Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

CAT24C01B

1K-Bit Serial EEPROM

FEATURES

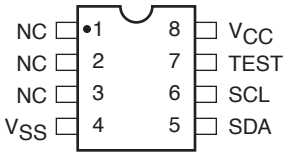
- 2-Wire Serial Interface
- 1.8 to 6.0Volt Operation
- Low Power CMOS Technology
- 4-Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin DIP, 8-pin SOIC, 8 pin TSSOP or 8-pin MSOP
- Commercial, Industrial and Automotive Temperature Ranges
- "Green" Package Options Available

DESCRIPTION

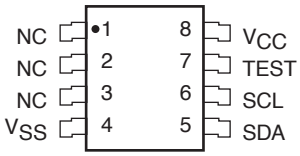
The CAT24C01B is a 1K-bit Serial CMOS EEPROM internally organized as 128 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C01B features a 4-byte page write buffer. The device operates via a 2-wire serial interface and is available in 8-pin DIP, 8-pin SOIC, 8-pin TSSOP or 8-pin MSOP.

PIN CONFIGURATION

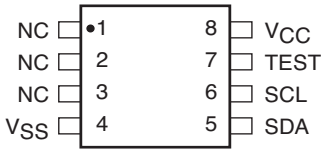
DIP Package (P, L)



SOIC Package (J, W)

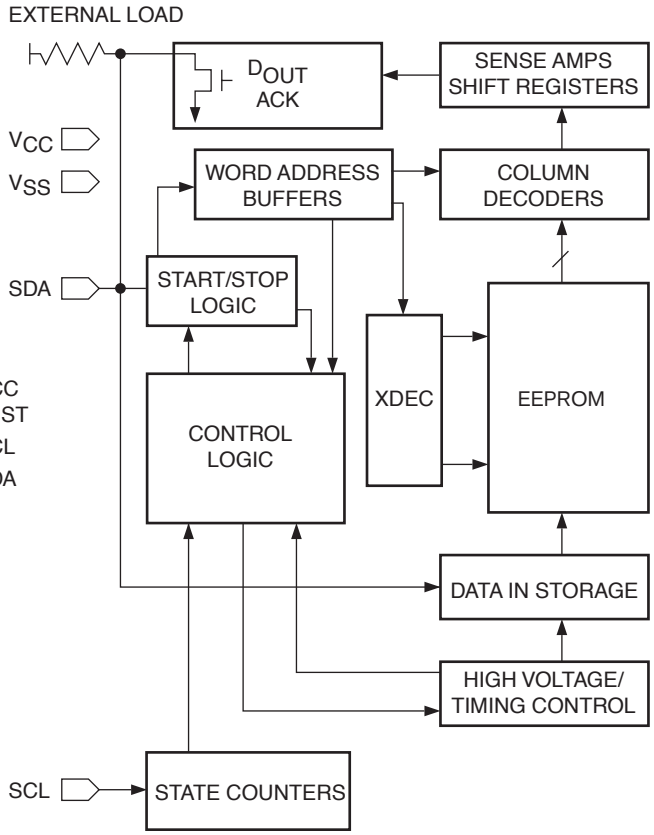


MSOP Package (R, Z)



TSSOP Package (U, Y)

BLOCK DIAGRAM



PIN FUNCTIONS

Pin Name	Function
NC	No Connect
SDA	Serial Data/Address
SCL	Serial Clock
V_{CC}	+1.8V to +6.0V Power Supply
V_{SS}	Ground
TEST	Test Input (GND, V_{CC} or Floating)

Doc. No. 1081, Rev. B

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Reference Test Method
N_{END}(3)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}(5)	Standby Current (V_{CC} = 5.0V)			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)			0.4	V	I_{OL} = 3 mA
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL, WP)	6	pF	V_{IN} = 0V

Note:

(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.

(2) Output shorted for no more than one second. No more than one output shorted at a time.

(3) This parameter is tested initially and after a design or process change that affects the parameter.

(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

(5) Standby Current (I_{SB}) = 0µA (<900nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, C_L=1TTL Gate and 100pF (unless otherwise specified).

Read & Write Cycle Limits

Symbol	Parameter	1.8V, 2.5V		4.5V-5.5V		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		100		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its input.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C01B uses a 2-wire data transmission protocol. The protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C01B operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24C01B serial clock input pin is used to clock all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address
The CAT24C01B bidirectional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs.

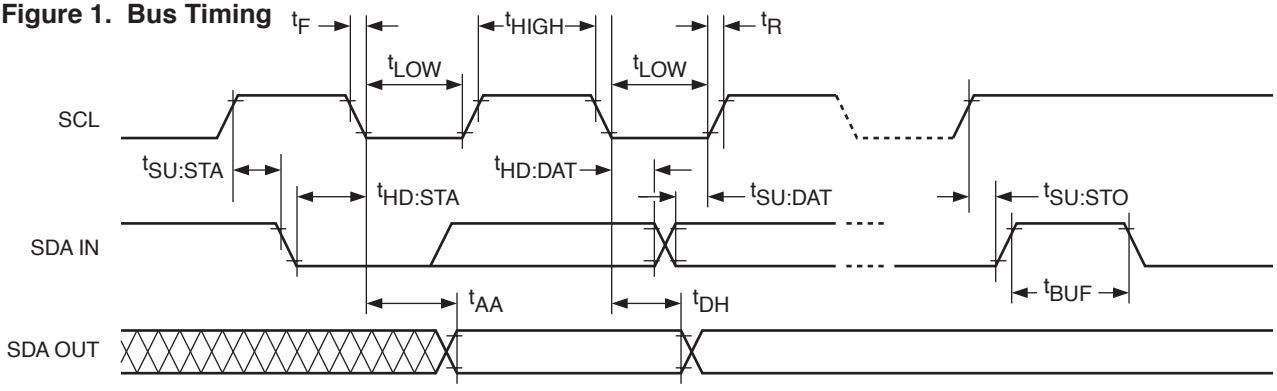
2-WIRE BUS PROTOCOL

The following defines the features of the 2-wire bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

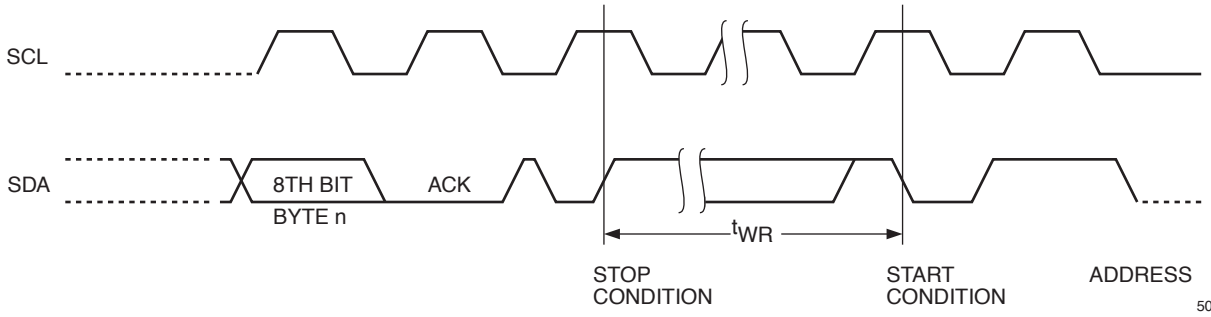
(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

Figure 1. Bus Timing



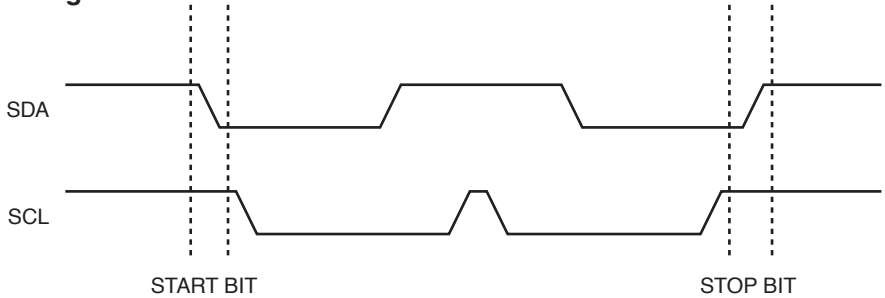
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C01B monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24C01B responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24C01B is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C01B will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C01B. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C01B acknowledge once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

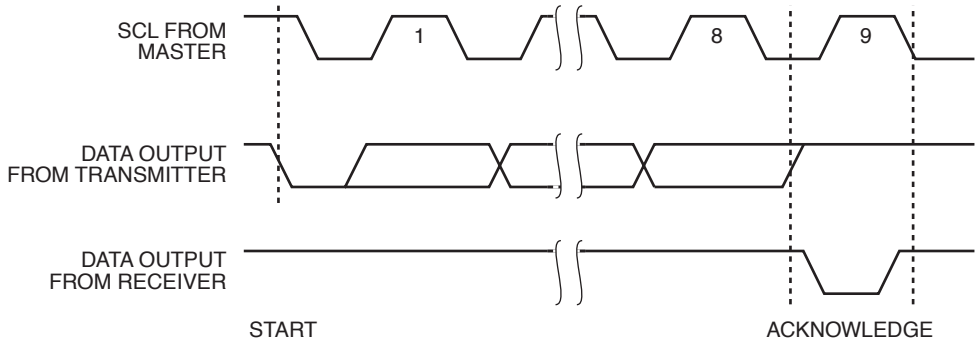
The CAT24C01B writes up to 4 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 3 additional bytes. After each byte has been transmitted the CAT24C01B will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 4 bytes prior to sending the STOP condition, the address counter 'wraps around,' and previously transmitted data will be overwritten.

Once all 4 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C01B in a single write cycle.

Note: Catalyst Semiconductor does program all "1" data into the entire memory array prior to shipping our EEPROM products.

Figure 4. Acknowledge Timing



5020 FHD F06

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C01B initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the byte address for a write operation. If the CAT24C01B is still busy with the write operation, no ACK will be returned. If the CAT24C01B has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

The READ operation for the CAT24C01B is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Two different READ operations are possible: Byte READ and Sequential READ.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issure a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Byte Read

To initiate a read operation, the master sends a start condition followed by a seven bit word address and a read bit. The CAT24C01B responds with an acknowledge and then transmits the eight bits of data. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the start word address, read bit, acknowledge and data transfer sequence.

Sequential Read

The Sequential READ operation can be initiated after the 24C01B sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C01B will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation is terminated when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24C01B is output sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C01B address bits so that the entire memory array can be read during one operation. If more than bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure5. Byte Write Timing

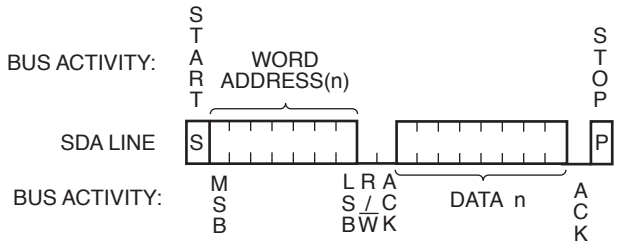


Figure 6. Page Write Timing

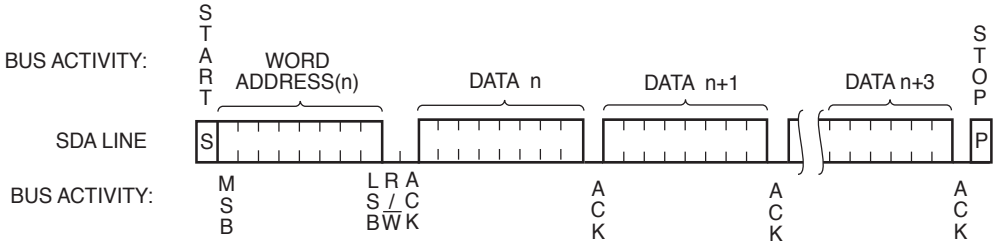


Figure 7. Byte Read Timing

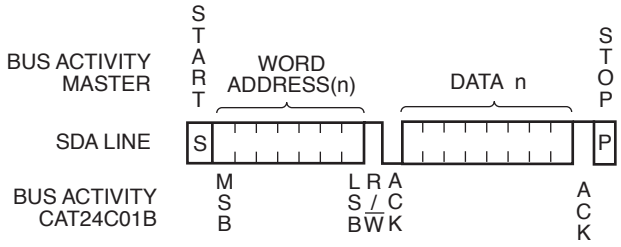
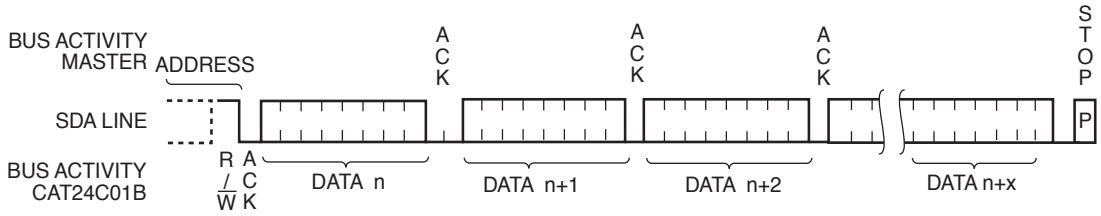
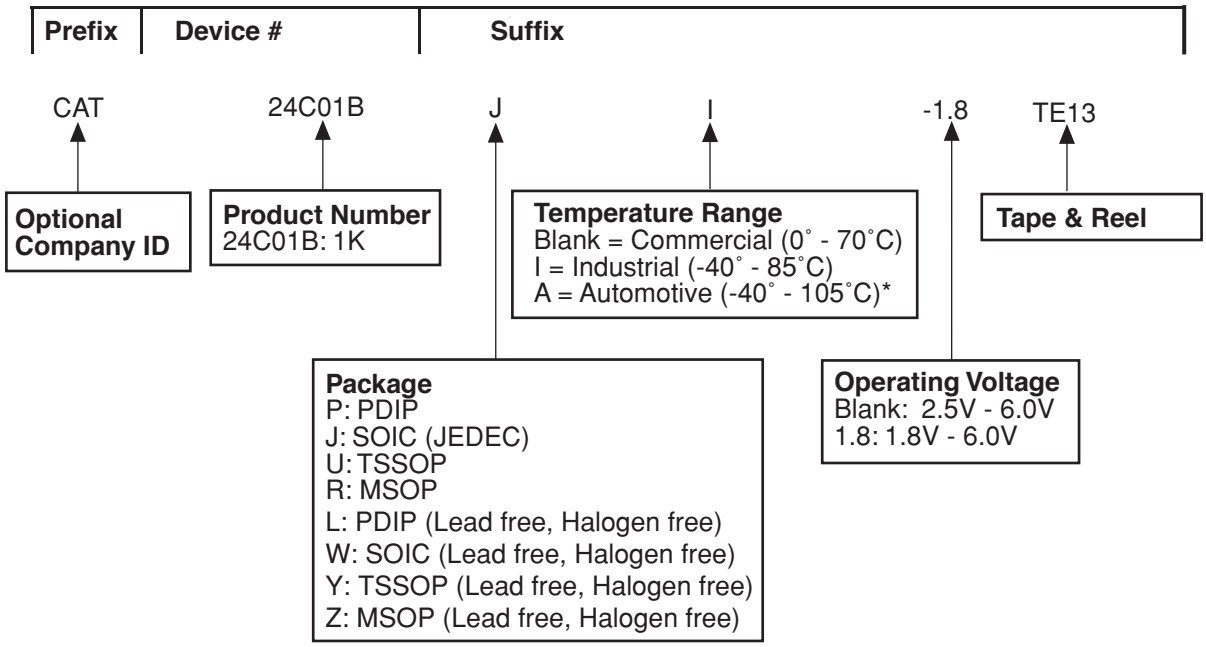


Figure 8. Sequential Read Timing



ORDERING INFORMATION



* -40˚ to +125˚C is available upon request

Notes:
(1) The device used in the above example is a 24C01BJI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)

REVISION HISTORY

Date	Revision	Comments
04/17/2004	B	Update Ordering Information Update Rev. Number

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