



Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT54/74FCT399T/AT/CT

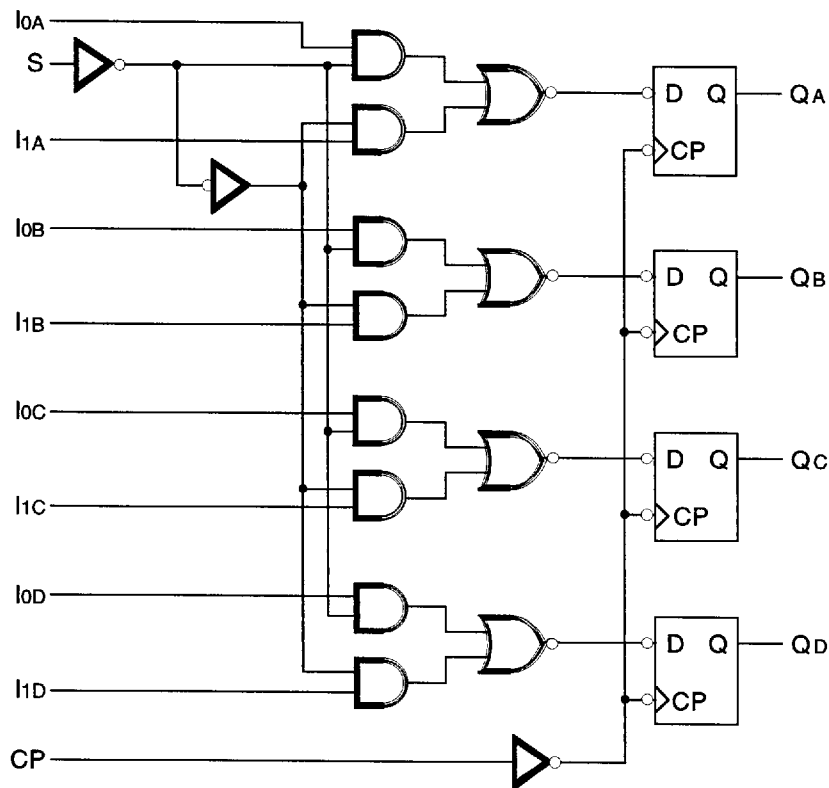
FEATURES:

- Std., A, and C speed grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT399T/AT/CT are high-speed quad dual-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X} , I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

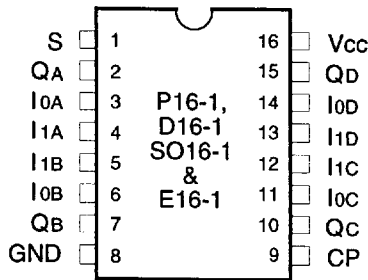


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MILITARY AND COMMERCIAL TEMPERATURE RANGES

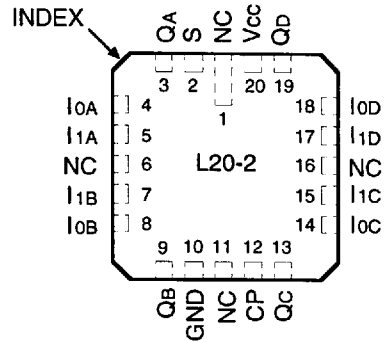
APRIL 1995

PIN CONFIGURATIONS



**DIP/SOIC/CERPACK
TOP VIEW**

2633 drw 03



**LCC
TOP VIEW**

2633 drw 02

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
I0A – I0D	Data Inputs from Source 0
I1A – I1D	Data Inputs from Source 1
QA – QD	Register True Outputs

2633 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
S	I0	I1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

2633 tbl 02

NOTE:

- H = HIGH Voltage Level
 L = LOW Voltage Level
 h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
 l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
 X = Immaterial

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V _{IN} = 0V	6	10	pF
COU	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE: 2633 Ink 04
1. This parameter is measured at characterization but not tested.

NOTES: 2633 Ink 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: TA = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max. V _I = 2.7V	—	—	±1	µA
I _{IL}	Input LOW Current ⁽⁴⁾	V _{CC} = Max. V _I = 0.5V	—	—	±1	µA
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., V _I = V _{CC} (Max.)	—	—	±1	µA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max ⁽³⁾ , V _O = GND	-60	-120	-225	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
		I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±1	µA
V _H	Input Hysteresis	—	—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.01	1	mA

NOTES: 2633 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at TA = -55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10MHz	V _{IN} = V _{CC} V _{IN} = GND	—	1.5	3.5	mA
		One Bit Toggling f _i = 5MHz 50% Duty Cycle	V _{IN} = 3.4V V _{IN} = GND	—	2.0	5.5	
		V _{CC} = Max., Outputs Open f _{CP} = 10MHz	V _{IN} = V _{CC} V _{IN} = GND	—	3.8	7.3 ⁽⁵⁾	
		Four Bits Toggling f _i = 5MHz 50% Duty Cycle	V _{IN} = 3.4V V _{IN} = GND	—	5.0	12.3 ⁽⁵⁾	

NOTES:

2633 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT399T				IDT54/74FCT399AT				IDT54/74FCT399CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Q _n	CL = 50pF RL = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	2.5	6.1	2.5	6.6	ns
tsu	Set-up Time HIGH or LOW In to CP		4.0	—	4.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
th	Hold Time HIGH or LOW In to CP		1.0	—	1.5	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tsu	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	8.5	—	9.0	—	ns
th	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
tw	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

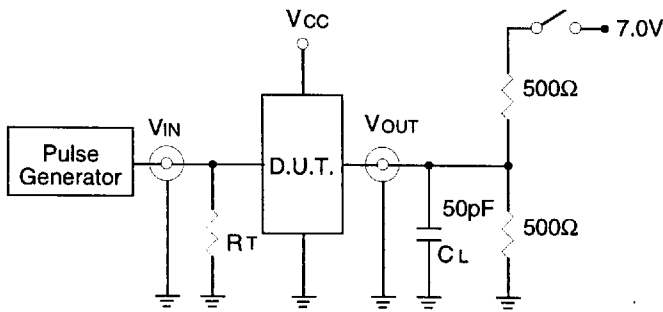
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2633 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2633 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

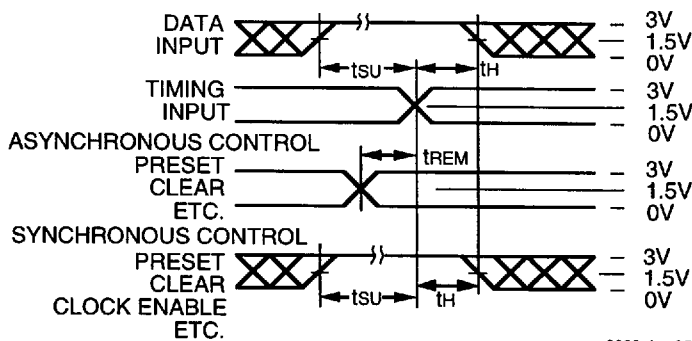
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to Zout of the Pulse Generator.

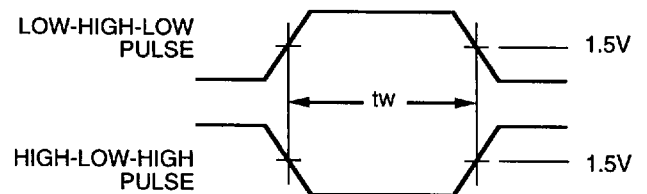
2633 Ink 08

SET-UP, HOLD AND RELEASE TIMES



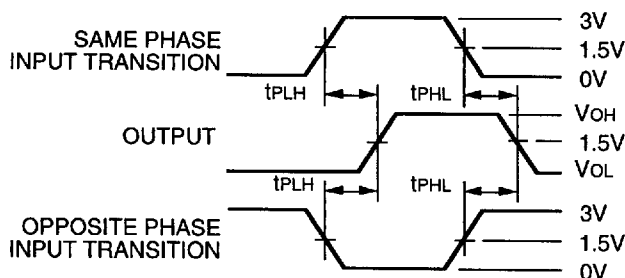
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PULSE WIDTH



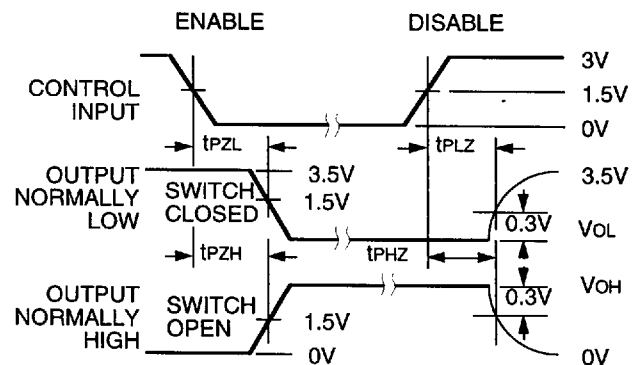
2633 drw 06

PROPAGATION DELAY



2633 drw 07

ENABLE AND DISABLE TIMES

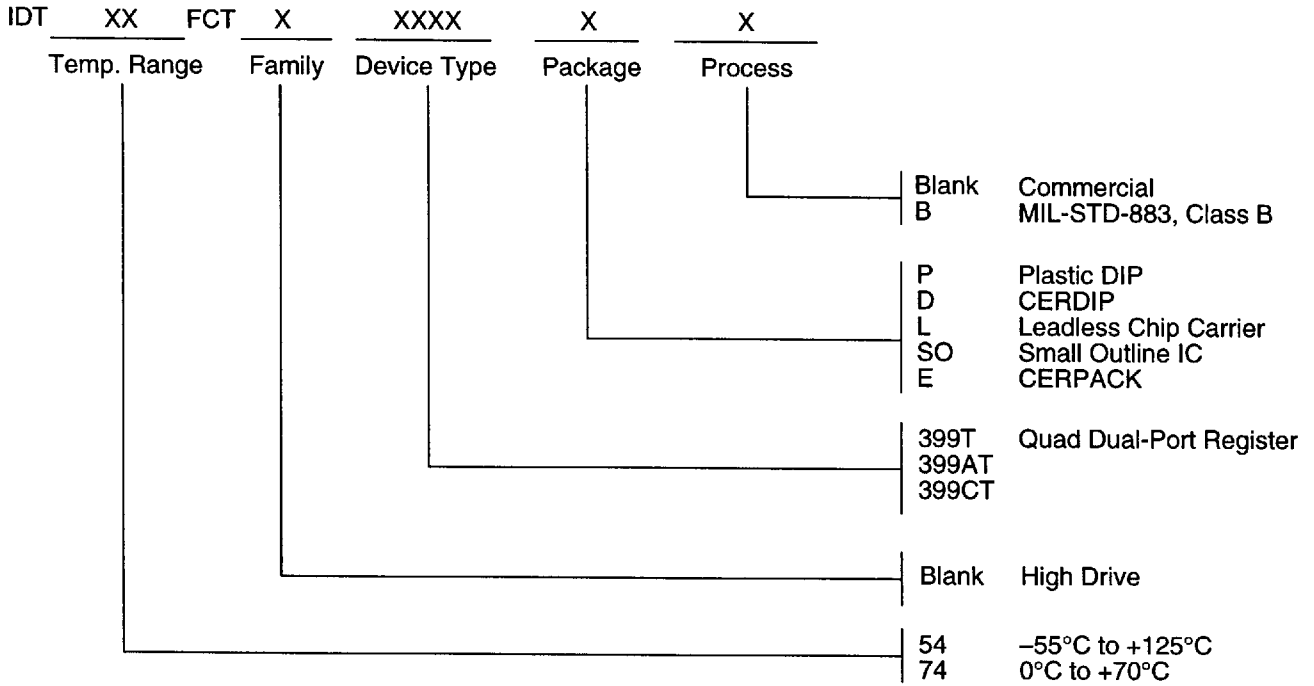


2633 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



2633 drw 09