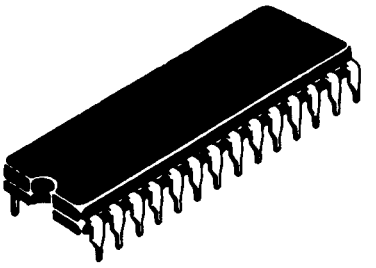
AKM6264A Series

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

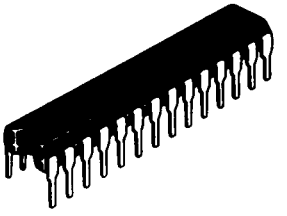
- Low Power Standby — Standby: 0.1mW (typ.) 10μW (typ.) L-/LL-version
  Low Power Operation — Operating: 15mW/MHz (typ.)
- Fast access Time — 100ns/120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/LL-version)

AKM6264AP Series



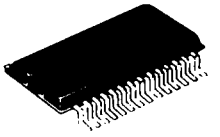
(DP-28)

AKM6264ASP Series



(DP-28N)

AKM6264AFP Series



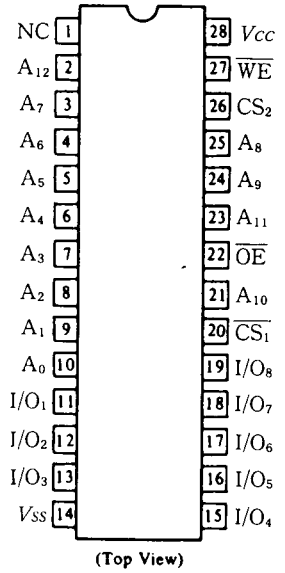
(FP-28D/DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
AKM6264AP-10 AKM6264AP-12 AKM6264AP-15	100ns 120ns 150ns	600 mil 28 pin Plastic DIP
AKM6264ALP-10 AKM6264ALP-12 AKM6264ALP-15	100ns 120ns 150ns	
AKM6264ALP-10L AKM6264ALP-12L AKM6264ALP-15L	100ns 120ns 150ns	
AKM6264ASP-10 AKM6264ASP-12 AKM6264ASP-15	100ns 120ns 150ns	300 mil 28 pin Plastic DIP
AKM6264ALSP-10 AKM6264ALSP-12 AKM6264ALSP-15	100ns 120ns 150ns	
AKM6264ALSP-10L AKM6264ALSP-12L AKM6264ALSP-15L	100ns 120ns 150ns	
AKM6264AFP-10 AKM5264AFP-12 AKM6264AFP-15	100ns 120ns 150ns	28 pin Plastic SOP (Note)
AKM6264ALFP-10 AKM6264ALFP-12 AKM6264ALFP-15	100ns 120ns 150ns	
AKM6264ALFP-10L AKM6264ALFP-12L AKM6264ALFP-15L	100ns 120ns 150ns	

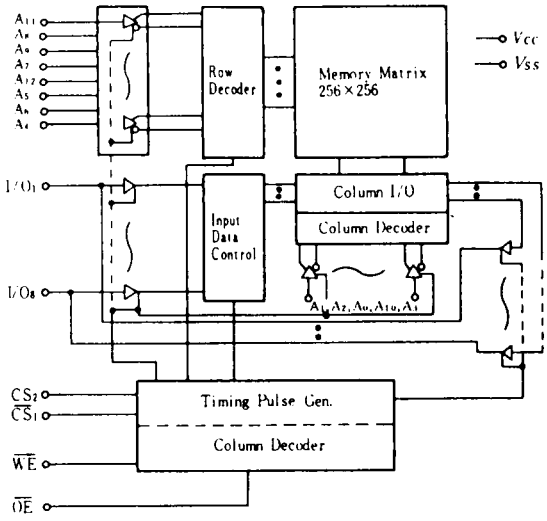
Note) T is added to the end of the type no. for a SOP of 3.00 mm (max.) thickness.

■ PIN CONFIGURATION



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage*1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}.
*2. −3.0V for pulse half-width ≦ 50ns

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB},I_{SB1}	
X	X	L	X		High Z	I_{SB},I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read Cycle
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*1	–	0.8	V

Note) *1. −3.0V for pulse half-width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}$=V_{IL}, CS2=V_{IH} $I_{I/O}$=0mA	–	30	45*5	mA
				30	55*6	
	I_{CC2}	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0mA, $\overline{CS1}$ ≦ 0.2V, CS2 ≧ V_{CC} –0.2V V_{IH} ≧ V_{CC} –0.2V, V_{IL} ≦ 0.2V	–	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ =V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1}$≧V_{CC}–0.2V, CS2≧V_{CC}–0.2V or 0V ≦ OS2 ≦ 0.2V, 0V ≦ V_{in}	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=–0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This characteristics is guaranteed only for LL-version.
*5. For 120ns/150ns version.
*6. For 100ns version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

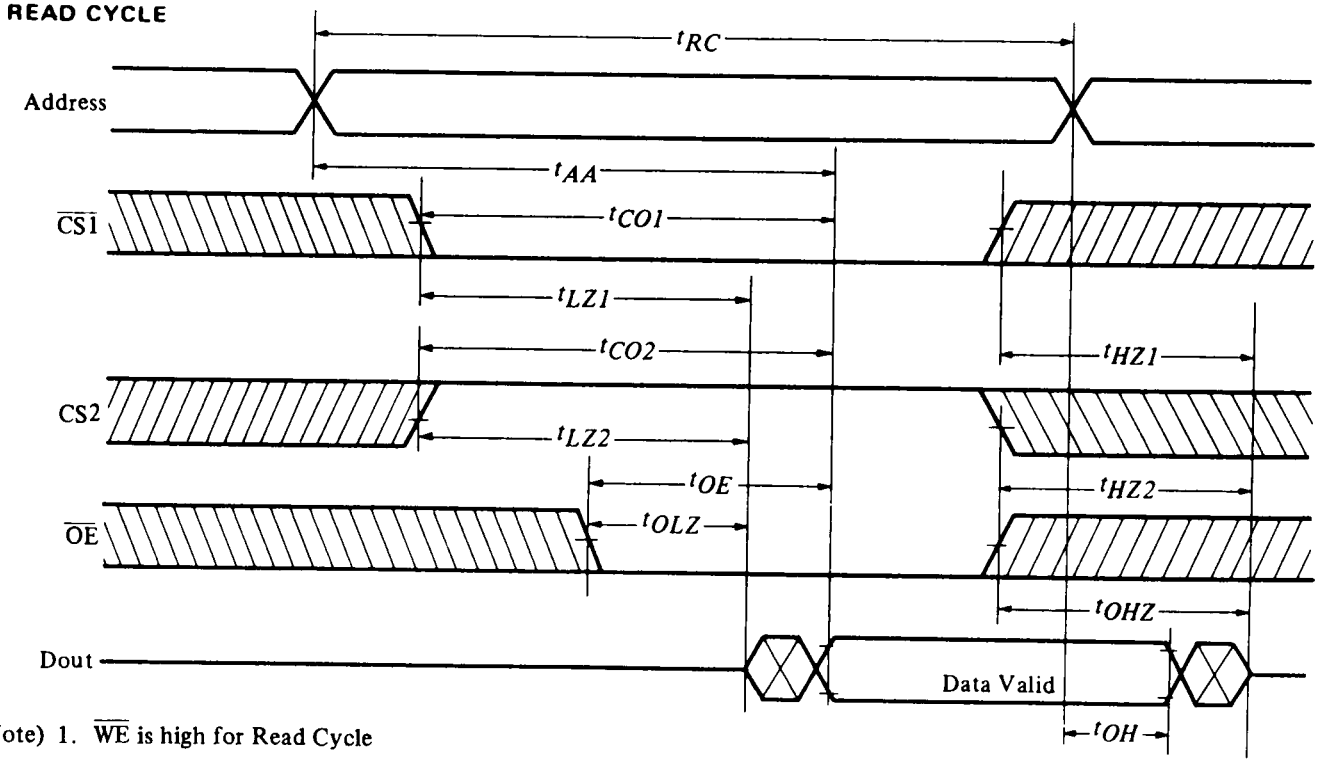
Input Pulse Levels: 0.8V/2.4V
Input Rise and Fall Time: 10ns
Input Timing Reference Level: 1.5V
Output Timing Reference Level: 0.8V/2.0V
Output Timing Reference Level: AKM6264A-10 1.5V
AKM6264A-12/15 0.8V/2.0V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

• READ CYCLE

Item		Symbol	AKM6264A-10		AKM6264A-12		AKM6264A-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	10	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from d device to device.

• READ CYCLE

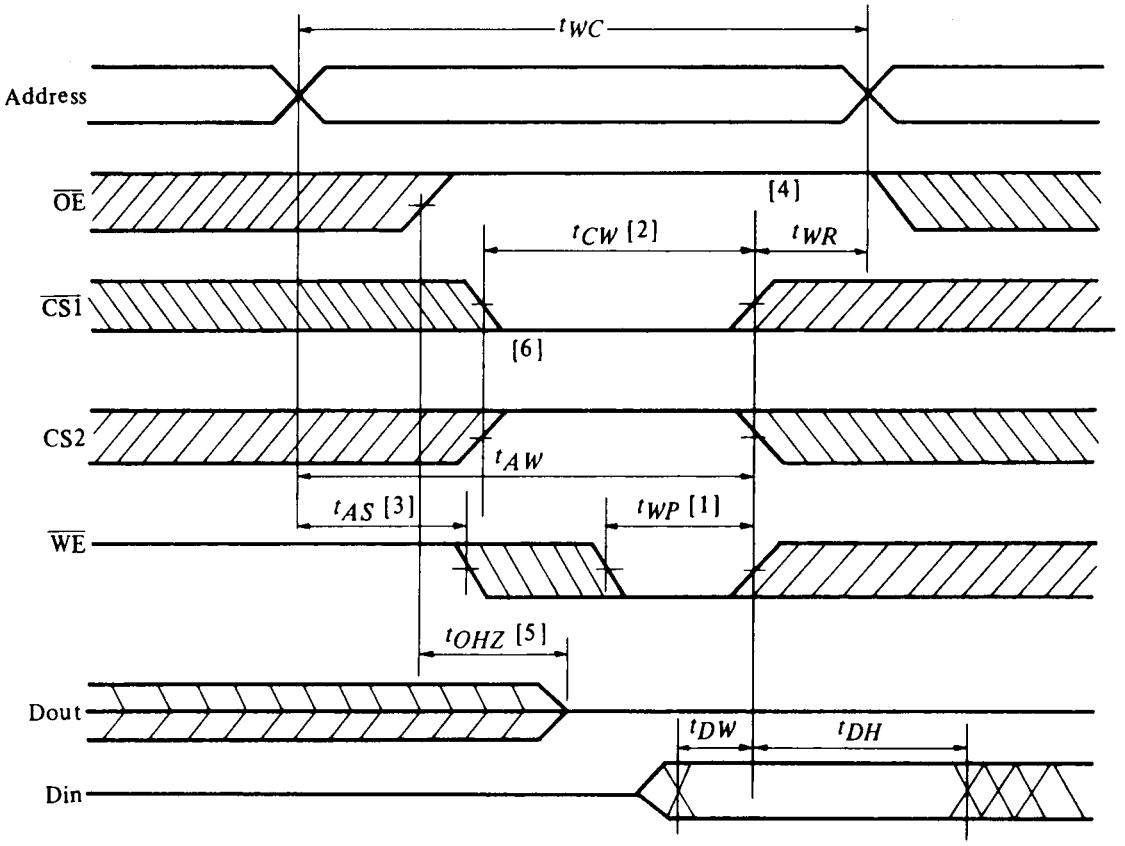


Note) 1. $\overline{WE}$ is high for Read Cycle

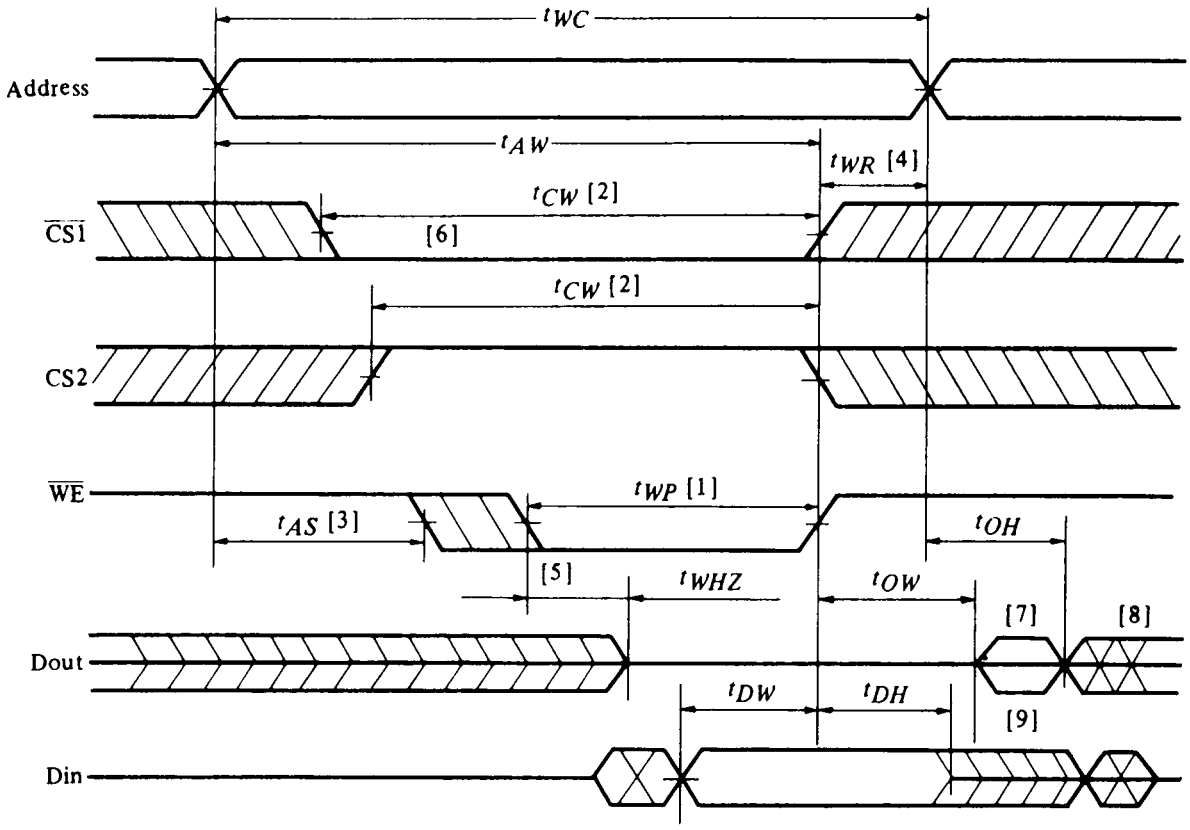
• **WRITE CYCLE**

Item	Symbol	AKM6264A-10		AKM6264A-12		AKM6264A-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	80	–	85	–	100	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width	t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Enable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

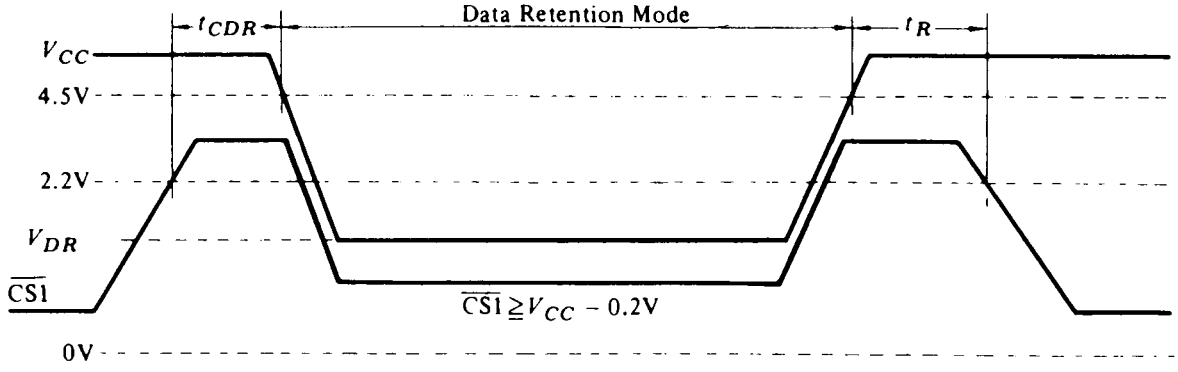
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

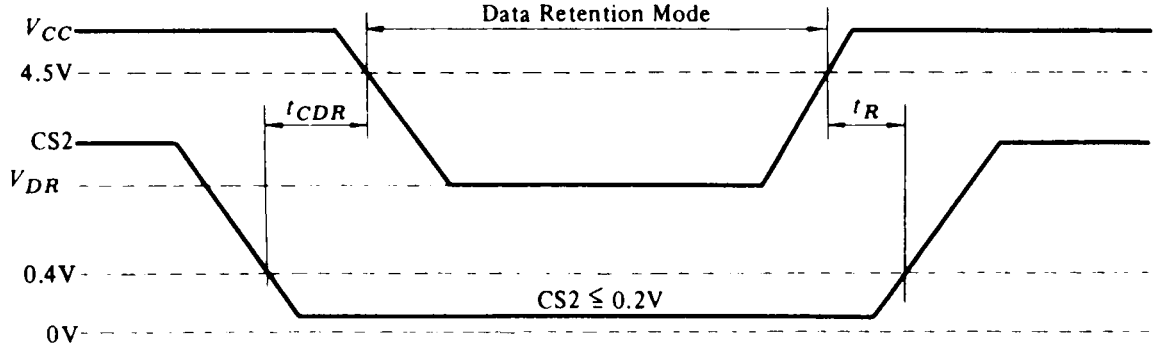
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
Data RetentionCurrent	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $0V \leqq CS2 \leqq 0.2V, 0V \leqq V_{in}$	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = −0.3V, 20μA max at T_a=0 to 40°C, This characteristics is guaranteed only for L-version.
*2. V_{IL} min = −0.3V, 10μA max at T_a = 0 to 40°C, This characteristics is guarnteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



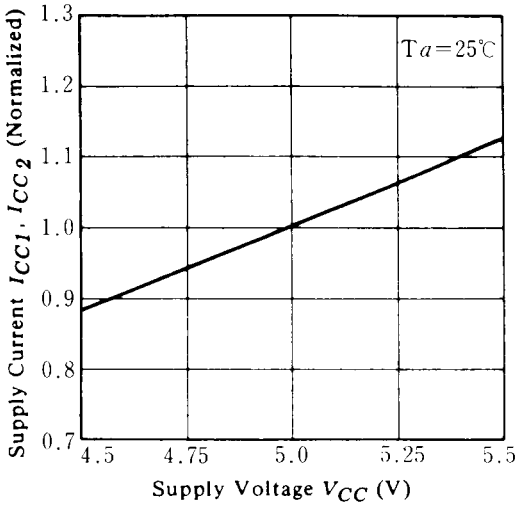
• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



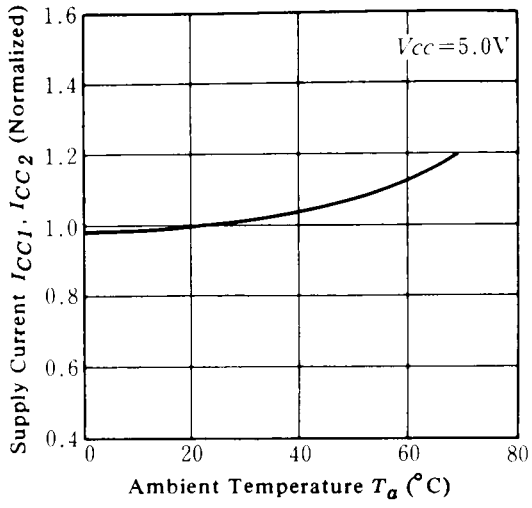
Note) In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

■ TYPICAL PERFORMANCE CHARACTERISTICS

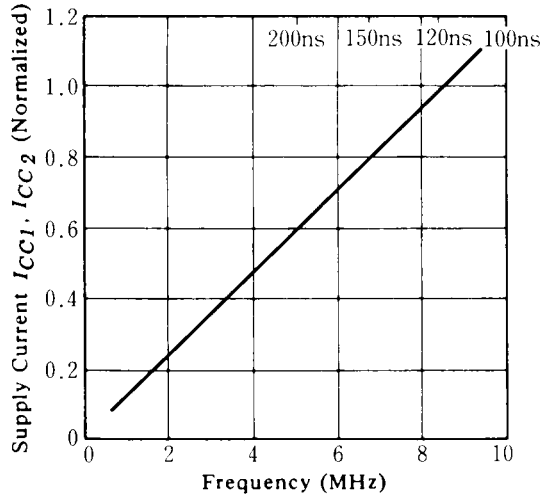
SUPPLY CURRENT vs. SUPPLY VOLTAGE



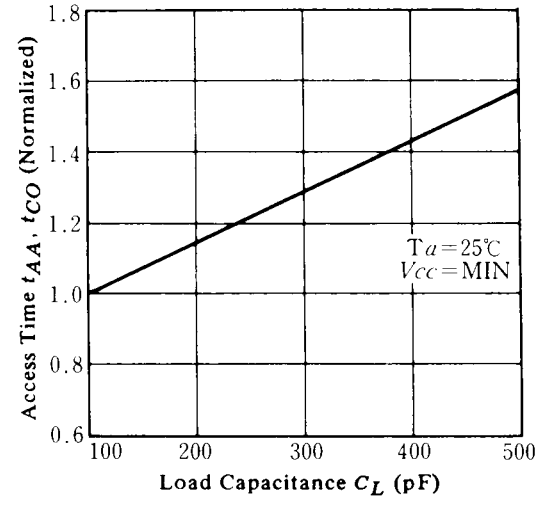
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



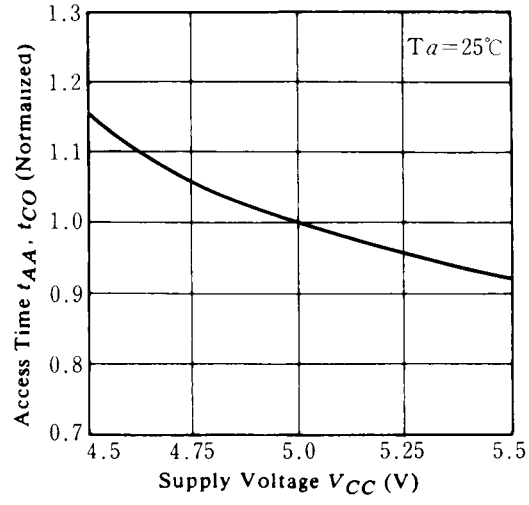
SUPPLY CURRENT vs. FREQUENCY



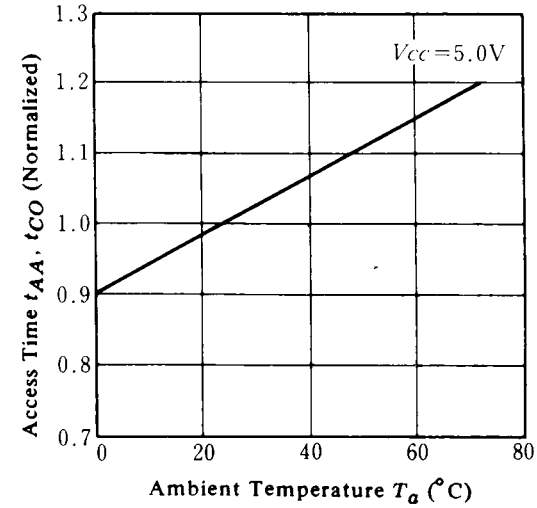
ACCESS TIME vs. LOAD CAPACITANCE



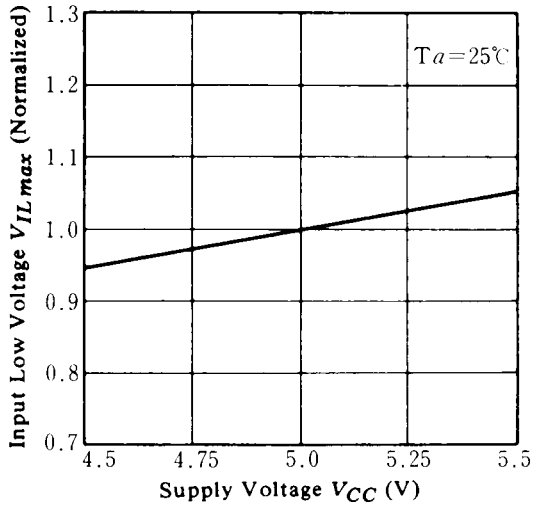
ACCESS TIME vs. SUPPLY VOLTAGE



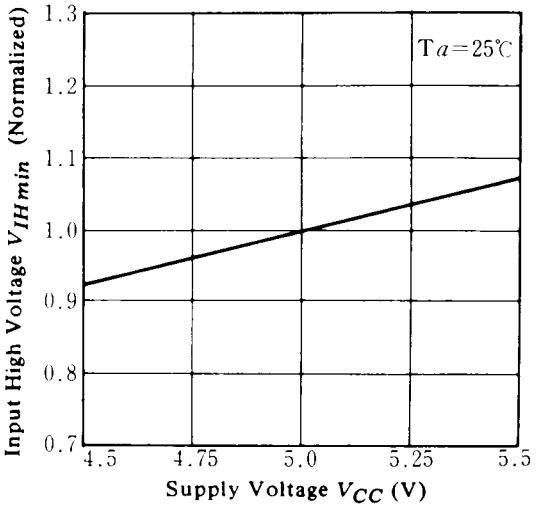
ACCESS TIME vs. AMBIENT TEMPERATURE



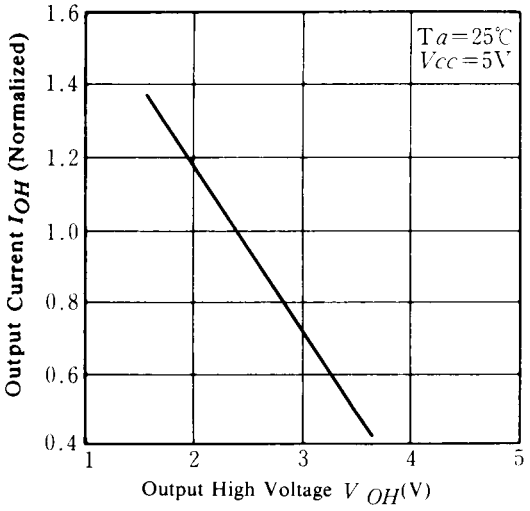
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



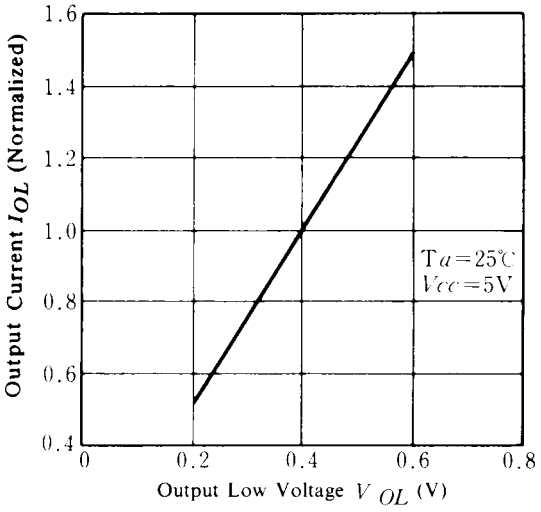
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



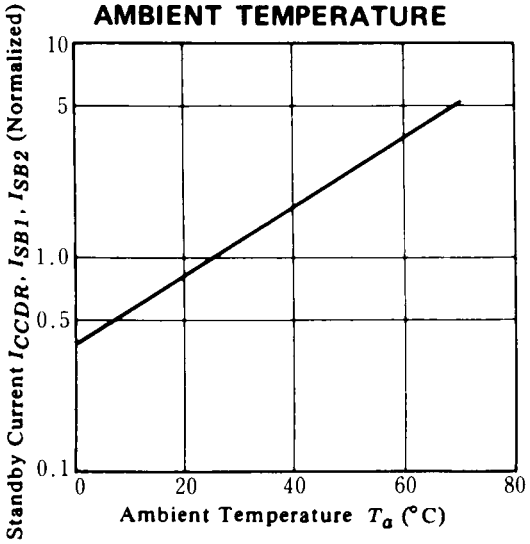
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE