Integrated Device Technology, Inc.

# LOW SKEW PLL-BASED CMOS CLOCK DRIVER (WITH 3-STATE)

**IDT74FCT88915TT**
**55/70/100/133**

## FEATURES:

- 0.5 MICRON CMOS Technology
- Input frequency range: 10MHz – f2Q Max. spec (FREQ_SEL = HIGH)
- Max. output frequency: 133MHz
- Pin and function compatible with MC88915T
- 5 non-inverting outputs, one inverting output, one 2x output, one ÷2 output; all outputs are TTL-compatible
- 3-State outputs
- Duty cycle distortion < 800ps (max.)
- TTL level output voltage swing
- 64/–15mA drive at TTL output voltage levels
- Available in 28 pin PLCC and SSOP packages

## DESCRIPTION:

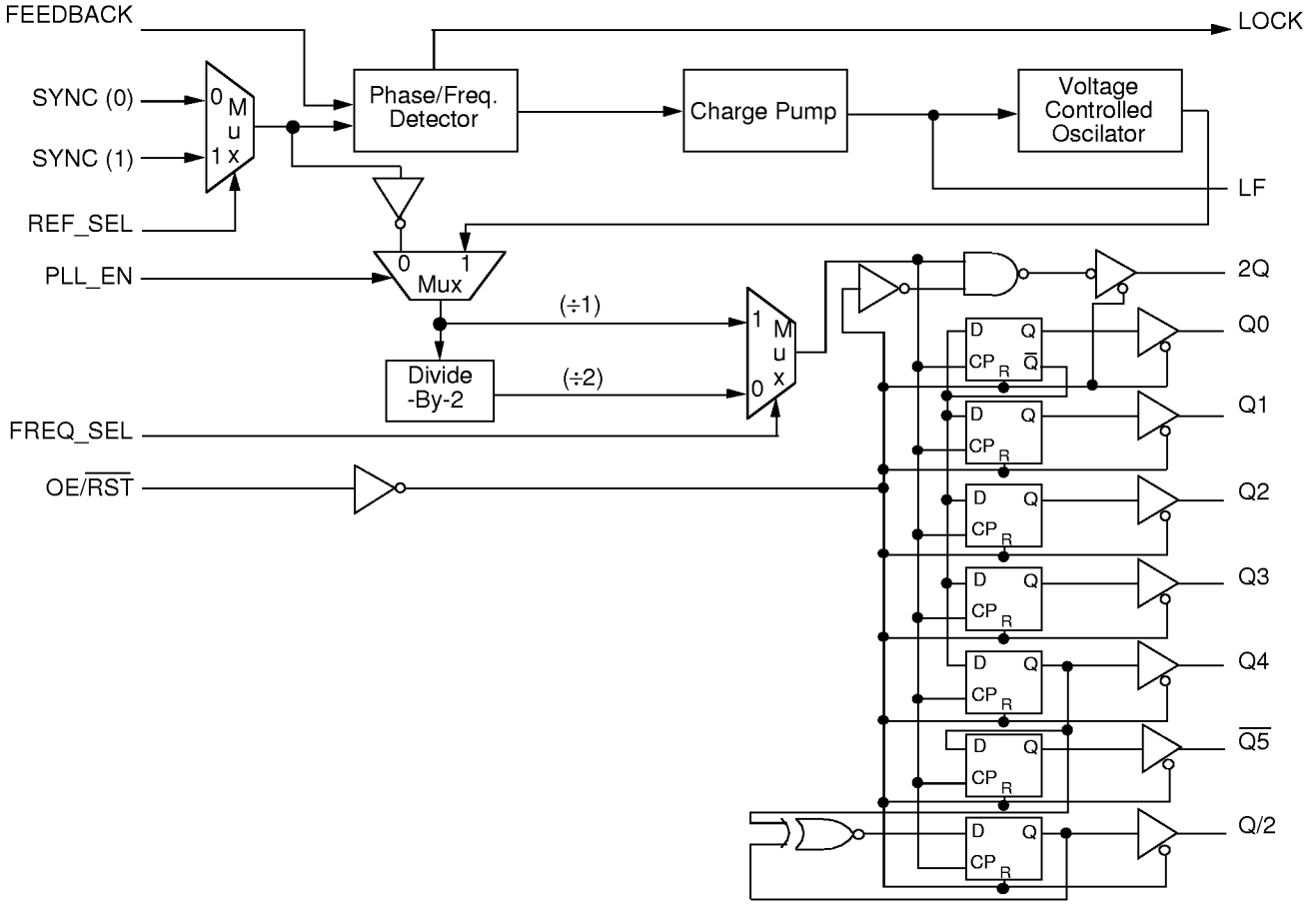
The FCT88915TT uses phase-lock loop technology to lock the frequency and phase of outputs to the input reference clock. It provides low skew clock distribution for high performance PCs and workstations. One of the outputs is fed back to the PLL at the FEEDBACK input resulting in essentially delay across the device. The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The VCO is designed for a 2Q operating frequency range of 40MHz to f2Q Max.

The FCT88915TT provides 8 outputs, the $\overline{Q5}$ output is inverted from the Q outputs. The 2Q runs at twice the Q frequency and Q/2 runs at half the Q frequency.

The FREQ_SEL control provides an additional ÷2 option in the output path. PLL _EN allows bypassing of the PLL, which is useful in static test modes. When PLL_EN is low, SYNC input may be used as a test clock. In this test mode, the input frequency is not limited to the specified range and the polarity of outputs is complementary to that in normal operation (PLL_EN = 1). The LOCK output attains logic HIGH when the PLL is in steady-state phase and frequency lock. When OE/$\overline{RST}$ is low, all the outputs are put in high impedance state and registers at Q, $\overline{Q}$ and Q/2 outputs are reset.

The FCT88915TT requires one external loop filter component as recommended in Figure 1.

## FUNCTIONAL BLOCK DIAGRAM

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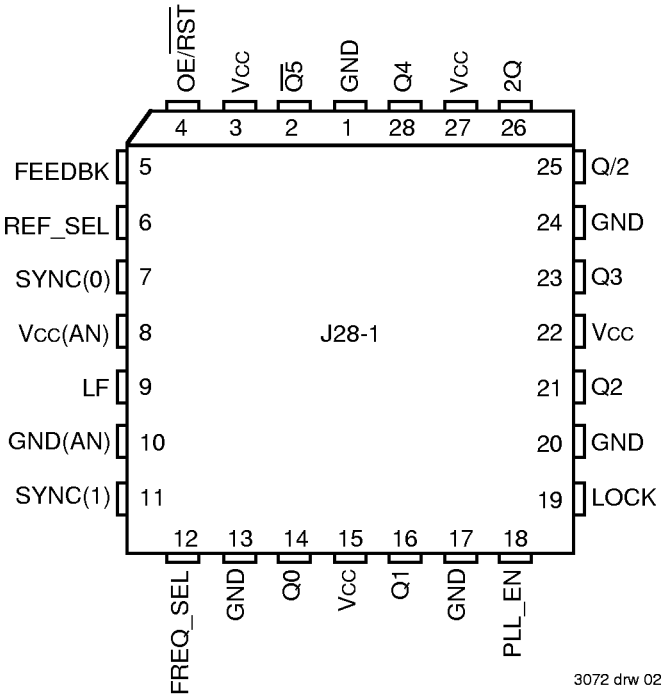
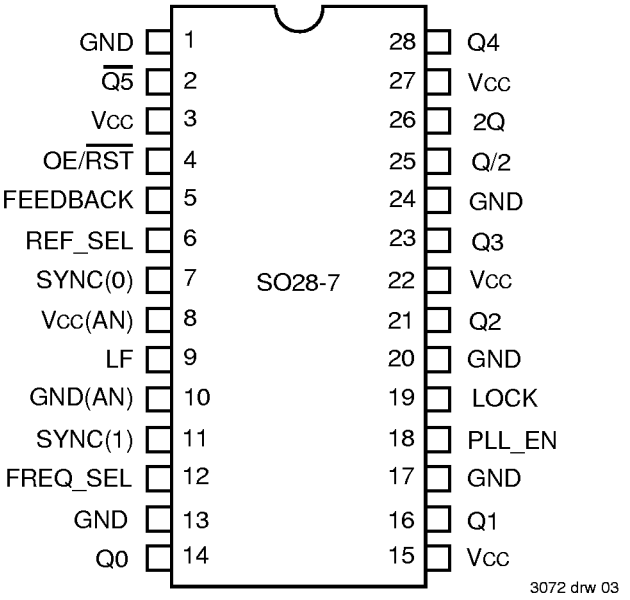
## PIN CONFIGURATIONS




**PLCC**
**TOP VIEW**




**SSOP**
**TOP VIEW**

## PIN DESCRIPTION

| Pin Name | I/O | Description |
|---|---|---|
| SYNC(0) | I | Reference clock input. |
| SYNC(1) | I | Reference clock input. |
| REF_SEL | I | Chooses reference between SYNC (0) & SYNC (1). (Refer to functional block diagram). |
| FREQ_SEL | I | Selects between ÷ 1 and ÷ 2 frequency options. (Refer to functional block diagram). |
| FEEDBACK | I | Feedback input to phase detector. |
| LF | I | Input for external loop filter connection. |
| Q0-Q4 | O | Clock output. |
| $\overline{Q5}$ | O | Inverted clock output. |
| 2Q | O | Clock output (2 x Q frequency). |
| Q/2 | O | Clock output (Q frequency ÷ 2). |
| LOCK | O | Indicates phase lock has been achieved (HIGH when locked). |
| OE/$\overline{RST}$ | I | Asynchronous reset (active LOW) and output enable (active HIGH). When HIGH, outputs are enabled. When LOW, outputs are in HIGH impedance. |
| PLL_EN | I | Disables phase-lock for low frequency testing. (Refer to functional block diagram). |

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## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +120 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed $V_{CC}$ by +0.5V unless otherwise noted.
2. Input and $V_{CC}$ terminals.
3. Output and I/O terminals.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 5.5 | 8 | pF |

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**NOTE:**
1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ± 5%

| Symbol | Parameter | Test Conditions(1) | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Current | | $V_I$ = GND | — | — | ±1 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | | | $V_O$ = 0.5V | — | — | ±1 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | — | | — | 100 | — | mV |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –3mA | 2.5 | 3.5 | — | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –15mA | 2.4 | 3.5 | — | V |
| | | | $I_{OH}$ = –32mA(3) | 2 | 3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 64mA | — | 0.2 | 0.55 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| $I_{CCL}$ $I_{CCH}$ $I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ (Test mode) | | — | 2 | 6 | mA |

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**NOTES:**
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Duration of the condition can not exceed one second.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC}$ = Max. $V_{IN}$ = $V_{CC}$ –2.1V[3] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max. All Outputs Open | $V_{IN}$ = $V_{CC}$ $V_{IN}$ = GND | — | 0.25 | 0.4 | mA/ MHz |
| $C_{PD}$ | Power Dissipation Capacitance | 50% Duty Cycle | | — | 15 | 40 | pF |
| $I_C$ | Total Power Supply Current[5,6] | $V_{CC}$ = Max. PLL_EN = 1, LOCK = 1, FEEDBACK = Q/2 SYNC frequency = 20MHz. Q/2 loaded with 50pF All other outputs open | | — | 25 | 40 | mA |
| | | $V_{CC}$ = Max. PLL_EN = 1, LOCK = 1, FEEDBACK = Q/2 SYNC frequency = 20MHz. Q/2 loaded with 50Ω Thevenin termination. All other outputs open | | — | 42 | 60 | mA |

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**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input; all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f) + I_{LOAD}$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f = 2Q frequency
   $I_{LOAD}$ = Dynamic Current due to load.

## SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{RISE/FALL}$ | Rise/Fall Times, SYNC inputs (0.8V to 2.0V) | — | 3 | ns |
| Frequency | Input Frequency, SYNC Inputs | 10.0[1] | 2Q fmax | MHz |
| Duty Cycle | Input Duty Cycle, SYNC Inputs | 25% | 75% | — |

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## OUTPUT FREQUENCY SPECIFICATIONS

| Symbol | Parameter | Min. | Max. [2] | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 55 | 70 | 100 | 133 | |
| f2Q | Operating frequency 2Q Output | 40 | 55 | 70 | 100 | 133 | MHz |
| fQ | Operating frequency Q0-Q4, $\overline{Q5}$ Outputs | 20 | 27.5 | 35 | 50 | 66.7 | MHz |
| fQ/2 | Operating frequency Q/2 Output | 10 | 13.75 | 17.5 | 25 | 33.3 | MHz |

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**NOTES:**

1. Note 8 in "General AC Specification Notes" and Figure 2 describes this specification and its actual limits depending on the feedback connection.
2. Maximum operating frequency is guaranteed with the part in a phase locked condition and all outputs loaded.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ All Outputs | Rise/Fall Time (between 0.8V and 2.0V) | Load = 50Ω to $V_{CC}/2$, $C_L$ = 20pF | 0.2[2] | 1.4 | ns |
| $t_{PULSE\ WIDTH}$[3] All outputs[3] | Output Pulse Width Q0-Q4, $\overline{Q}$5, Q/2, 2Q @ 1.5V | | $0.5t_{CYCLE} - 0.8$[5] | $0.5t_{CYCLE} + 0.8$[5] | ns |
| $t_{PD}$ SYNC-FEEDBACK[3] | SYNC input to FEEDBACK delay (measured at SYNC0 or 1 and FEEDBACK input pins) | Load = 50Ω to $V_{CC}/2$, $C_L$ = 20pF 0.1µF from LF to Analog GND[5] | –0.2 | +1.2 | ns |
| $t_{SKEWr}$ (rising)[3,4] | Output to Output Skew between outputs 2Q, Q0-Q4, Q/2 (rising edges only) | Load = 50Ω to $V_{CC}/2$, $C_L$ = 20pF | — | 600 | ps |
| $t_{SKEWf}$ (falling)[3,4] | Output to Output Skew between outputs Q0-Q4 (falling edges only) | | — | 350 | ps |
| $t_{SKEWall}$ [3,4] | Output to Output Skew 2Q, Q/2, Q0-Q4 rising, $\overline{Q}$5 falling | | — | 600 | ps |
| $t_{LOCK}$[6] | Time required to acquire Phase-Lock from time SYNC input signal is received | | 1[2] | 10 | ms |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time OE/$\overline{RST}$ (LOW-to-HIGH) to Q, 2Q, Q/2, $\overline{Q}$ | | 3[2] | 14 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time OE/$\overline{RST}$ (HIGH-to-LOW) to Q, 2Q, Q/2, $\overline{Q}$ | | 3[2] | 14 | ns |

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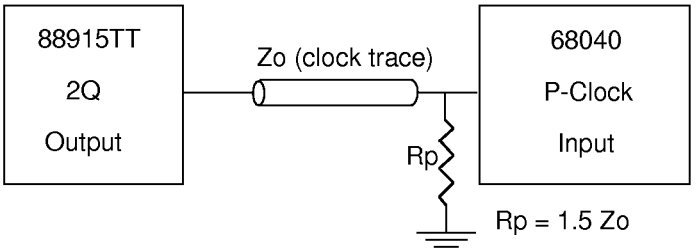
**GENERAL AC SPECIFICATION NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions, and at a fixed temperature and voltage.
5. $t_{CYCLE}$ = 1/frequency at which each output (Q, $\overline{Q}$, Q/2 or 2Q) is expected to run.
6. With $V_{CC}$ fully powered-on and an output properly connected to the FEEDBACK pin. $t_{LOCK}$ Max. is with C1 = 0.1µF, $t_{LOCK}$ Min. is with C1 = 0.01µF. (Where C1 is loop filter capacitor shown in Figure 1).

**NOTES:**

7. These two specs ( $t_{RISE/FALL}$ and $t_{PULSE\ WIDTH}$ 2Q output) guarantee that the FCT88915TT meets 68040 P-Clock input specification.

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8. The wiring diagrams and written explanations of Figure 4 demonstrate the input and output frequency relationships for various possible feedback configurations. The allowable SYNC input range to stay in the phase-locked condition is also indicated. There are two allowable SYNC frequency ranges, depending on whether FREQ_SEL is HIGH or LOW. Also it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the Q outputs. The table below summarizes the allowable SYNC frequency range for each possible configuration.

| FREQ_SEL Level | Feedback Output | Allowable SYNC Input Frequency Range (MHz) | Corresponding 2Q output Frequency Range | Phase Relationship of the Q Outputs to Rising SYNC Edge |
|---|---|---|---|---|
| HIGH | Q/2 | 10 to (2Q $f_{MAX}$ Spec)/4 | 40 to (2Q $f_{MAX}$ Spec) | 0° |
| HIGH | Any Q (Q0-Q4) | 20 to (2Q $f_{MAX}$ Spec)/2 | 40 to (2Q $f_{MAX}$ Spec) | 0° |
| HIGH | $\overline{Q5}$ | 20 to (2Q $f_{MAX}$ Spec)/2 | 40 to (2Q $f_{MAX}$ Spec) | 180° |
| HIGH | 2Q | 40 to (2Q $f_{MAX}$ Spec) | 40 to (2Q $f_{MAX}$ Spec) | 0° |
| LOW | Q/2 | 5 to (2Q $f_{MAX}$ Spec)/8 | 20 to (2Q $f_{MAX}$ Spec)/2 | 0° |
| LOW | Any Q (Q0-Q4) | 10 to (2Q $f_{MAX}$ Spec)/4 | 20 to (2Q $f_{MAX}$ Spec)/2 | 0° |
| LOW | $\overline{Q5}$ | 10 to (2Q $f_{MAX}$ Spec)/4 | 20 to (2Q $f_{MAX}$ Spec)/2 | 180° |
| LOW | 2Q | 20 to (2Q $f_{MAX}$ Spec)/2 | 20 to (2Q $f_{MAX}$ Spec)/2 | 0° |

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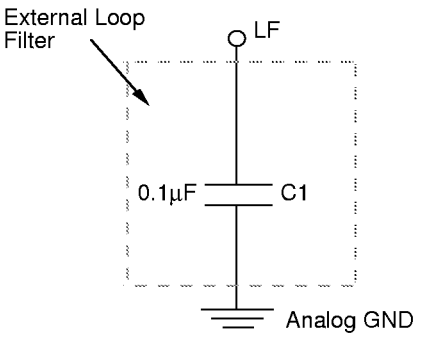
9. The tPD spec describes how the phase offset between the SYNC input and the output connected to the FEEDBACK input, varies with process, temperature and voltage. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to $V_{CC}$ and 100Ω to ground. tPD measurements were made with the loop filter connection shown below:

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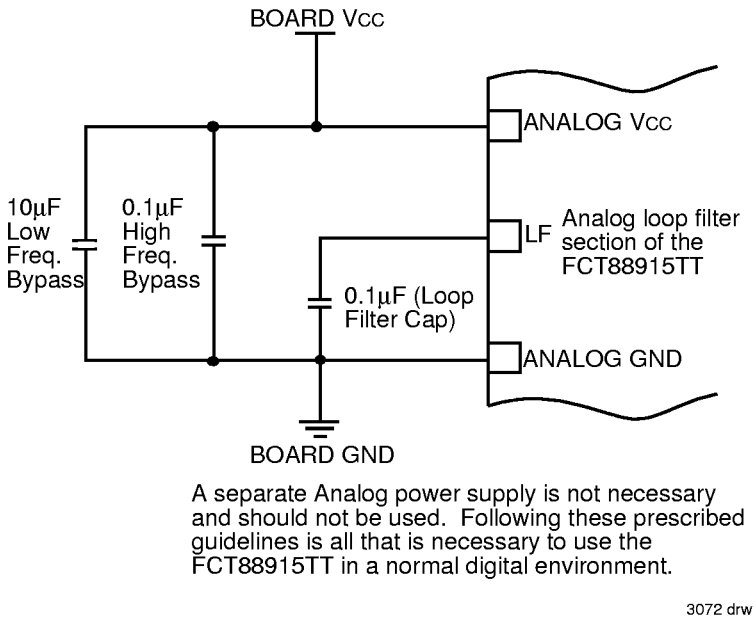



**Figure 1. Recommended Loop Filter and Analog Isolation Scheme for the FCT88915TT**

**NOTES:**

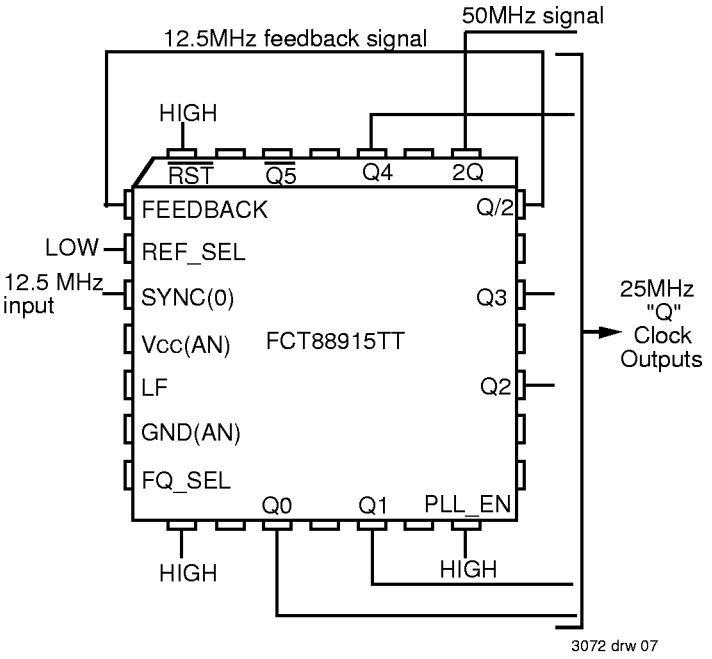
1. Figure 1 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

   a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the LF pin.
   b. The 10µF low frequency bypass capacitor and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915TT's sensitivity to voltage transients from the system digital Vcc supply and ground planes.
   If good bypass techniques are used on a board design near components which may cause digital Vcc and ground noise, Vcc step deviations should not occur at the 88915TT's digital Vcc supply. The purpose of the bypass filtering scheme shown in figure 1 is to give the 88915TT additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.
   c. The loop filter capacitor (0.1µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
2. In addition to the bypass capacitors used in the analog filter of figure 1 there should be a 0.1µF bypass capacitor between each of the other (digital) four Vcc pins and the board ground plane. This will reduce output switching noise caused by the 88915TT outputs, in addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the 88915TT package as possible.

The frequency relationship shown here is applicable to all Q outputs (Q0, Q1, Q2, Q3 and Q4).

## 1:2 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The Q outputs (Q0-Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2Q output will run at 4X the Q/2 frequency.

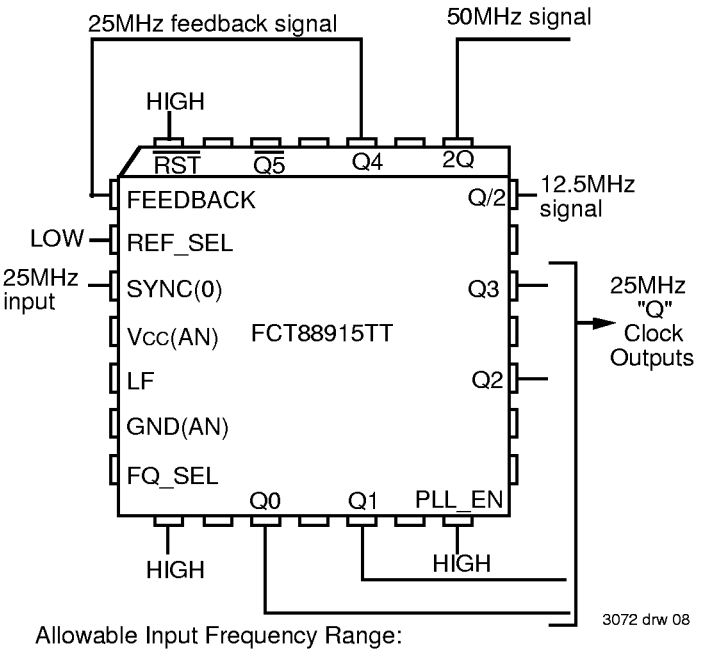



Allowable Input Frequency Range:
10MHz to (f2Q FMAX Spec /4 (for FREQ_SEL HIGH)
5MHz to (f2Q FMAX Spec /8 (for FREQ_SEL LOW)

**Figure 2a. Wiring Diagram and Frequency Relationships With Q/2 Output Feedback**

## 1:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the Q frequency, and the 2Q output will run at 2X the Q frequency.

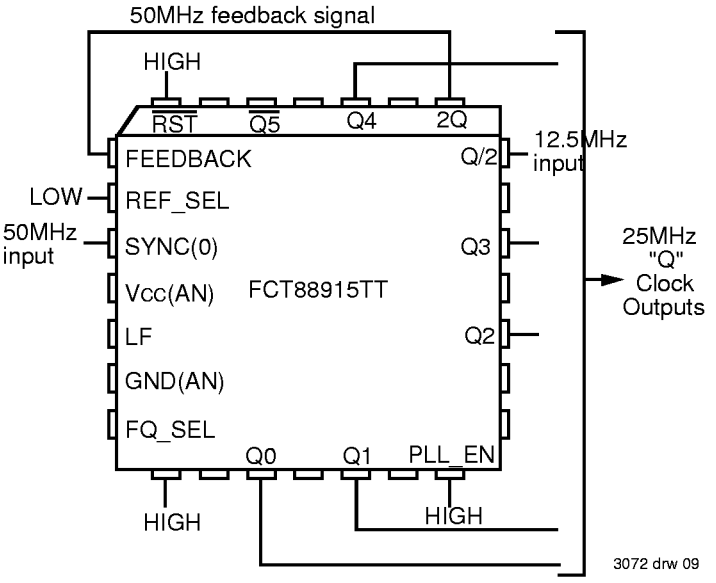



Allowable Input Frequency Range:
20MHz to (f2Q FMAX Spec)/2 (for FREQ_SEL HIGH)
10MHz to (f2Q FMAX Spec)/4 (for FREQ_SEL LOW)

**Figure 2b. Wiring Diagram and Frequency Relationships With Q4 Output Feedback**

## 2:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the 2Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2Q and SYNC, thus the 2Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2Q frequency, and the Q output will run at 1/2 the 2Q frequency.




Allowable Input Frequency Range:
40MHz to (f2Q FMAX Spec) (for FREQ_SEL HIGH)
20MHz to (f2Q FMAX Spec)/2 (for FREQ_SEL LOW)

**Figure 2c. Wiring Diagram and Frequency Relationships With 2Q Output Feedback**

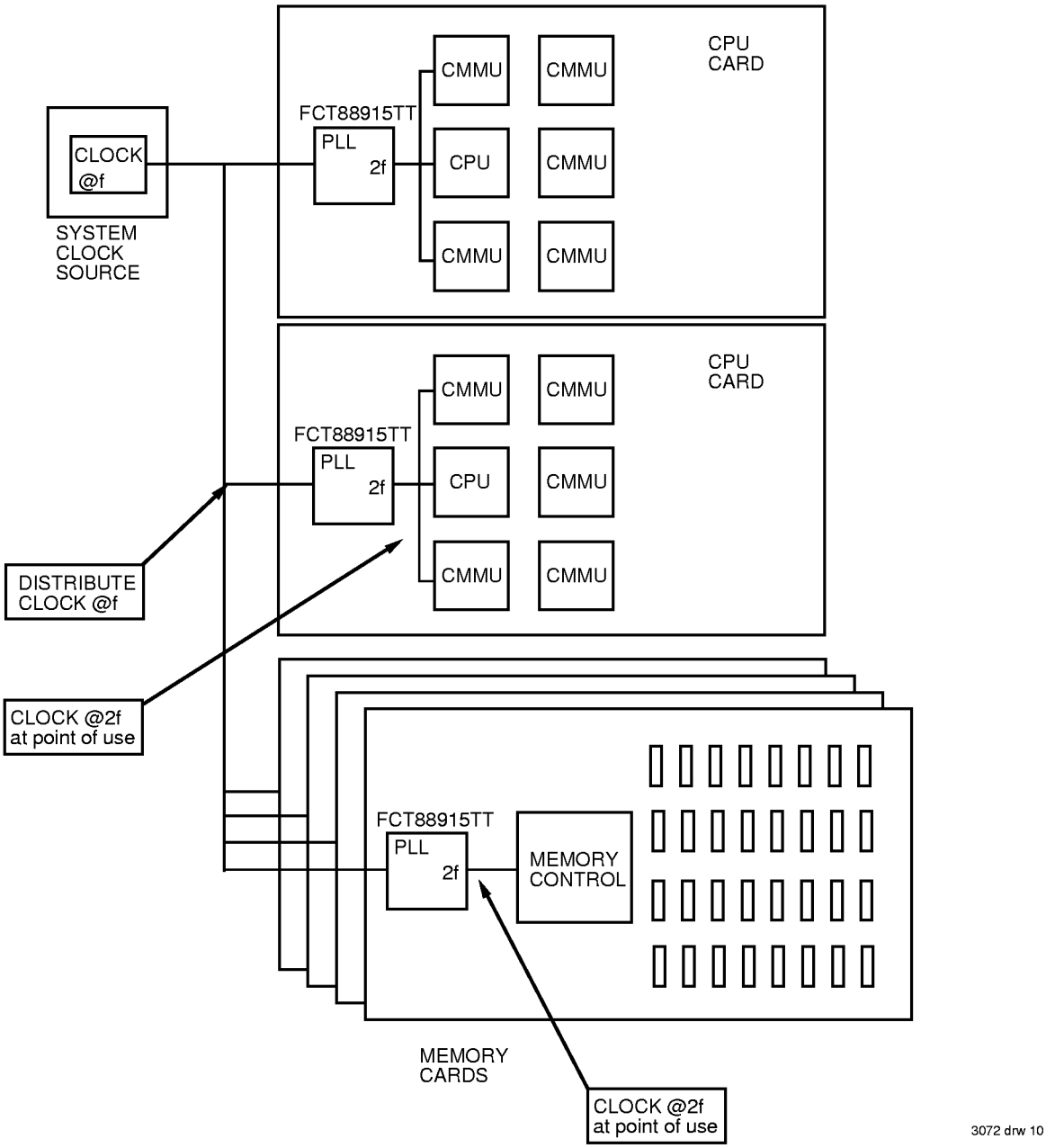



**Figure 3. Multiprocessing Application Using the FCT88915TT for Frequency Multiplication and Low Board-to-Board skew**

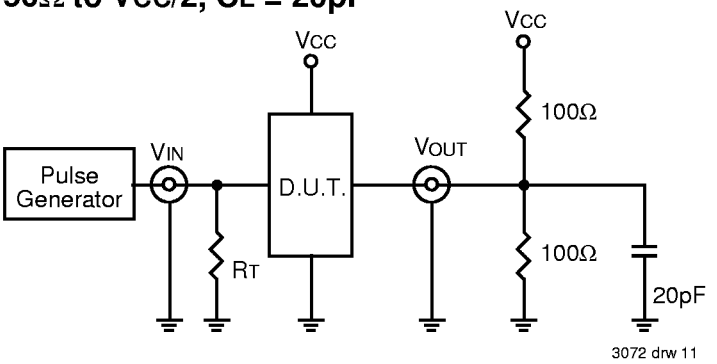
## FCT88915TT System Level Testing Functionality

When the PLL_EN pin is LOW, the PLL is bypassed and the FCT88915TT is in low frequency "test mode". In test mode (with FREQ_SEL HIGH), the 2Q output is inverted from the selected SYNC input, and the Q outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4 (negative edge triggered). With FREQ_SEL LOW the 2Q output is divide-by-2 of the SYNC, the Q outputs divide-by-4, and the Q/2 output divide-by-8. These relationships can be seen in the block diagram. A recommended test configuration would be to use SYNC0 or SYNC1 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic.

This functionality is needed since most board-level testers run at 1 MHz or below, and theFCT 88915TT cannot lock onto that low of an input frequency. In the test mode described above, any test frequency test can be used.

## TEST CIRCUITS AND WAVEFORM

### 50Ω to VCC/2, CL = 20pF

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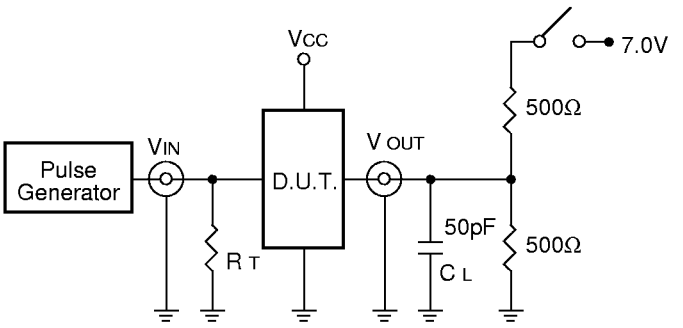
### ENABLE AND DISABLE TEST CIRCUIT

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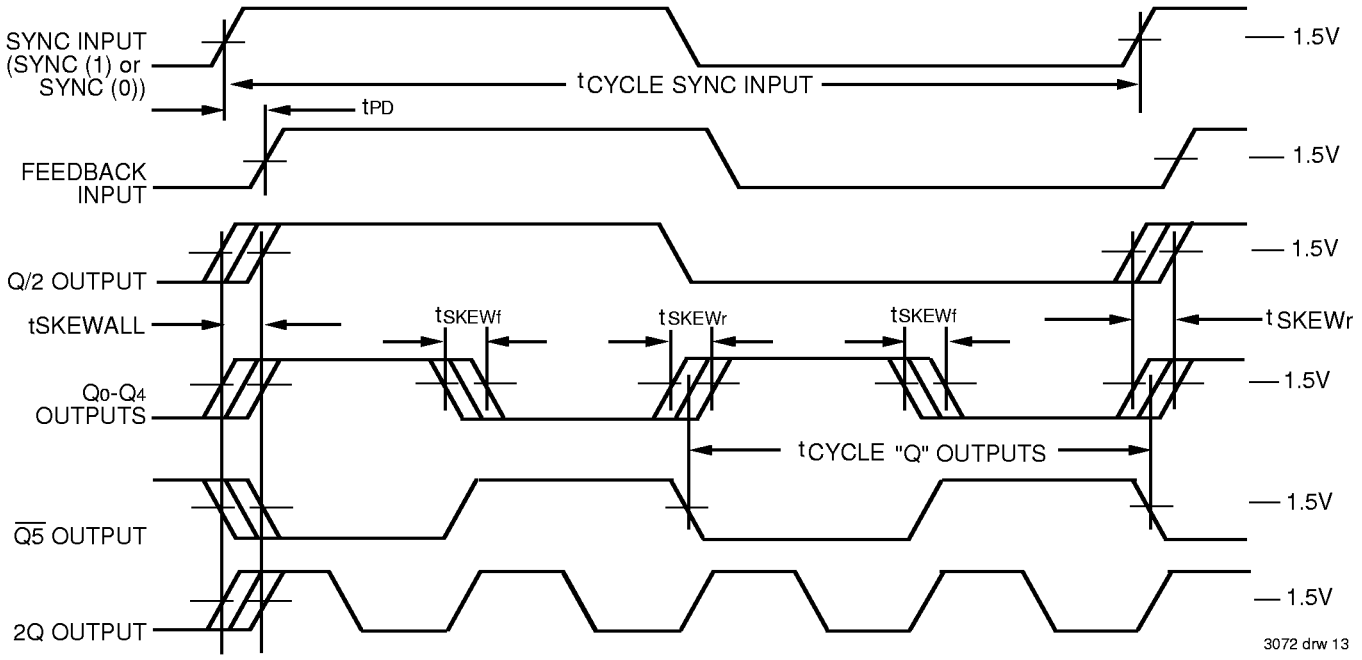
## PROPAGATION DELAY, OUTPUT SKEW

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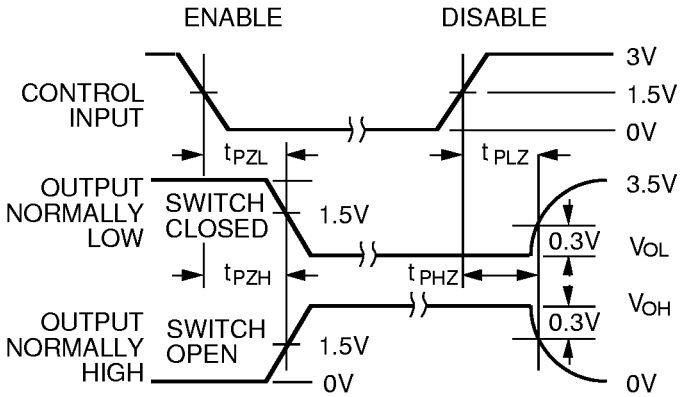
**(These waveforms represent the hookup of Figure 2a)**

**NOTES:**

1. The FCT88915TT aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the 1.5V crossing point of the appropriate output edges. All skews are specified as "windows", not as ± deviation around a center point.
3. If a Q output is connected to the FEEDBACK input (this situation is not shown), the Q output frequency would match the SYNC input frequency, the 2Q output would run at twice the SYNC frequency and the Q/2 output would run at half the SYNC frequency.

## ENABLE AND DISABLE TIMES

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**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: tF ≤ 2.5ns; tR ≤ 2.5ns

## SWITCH POSITION

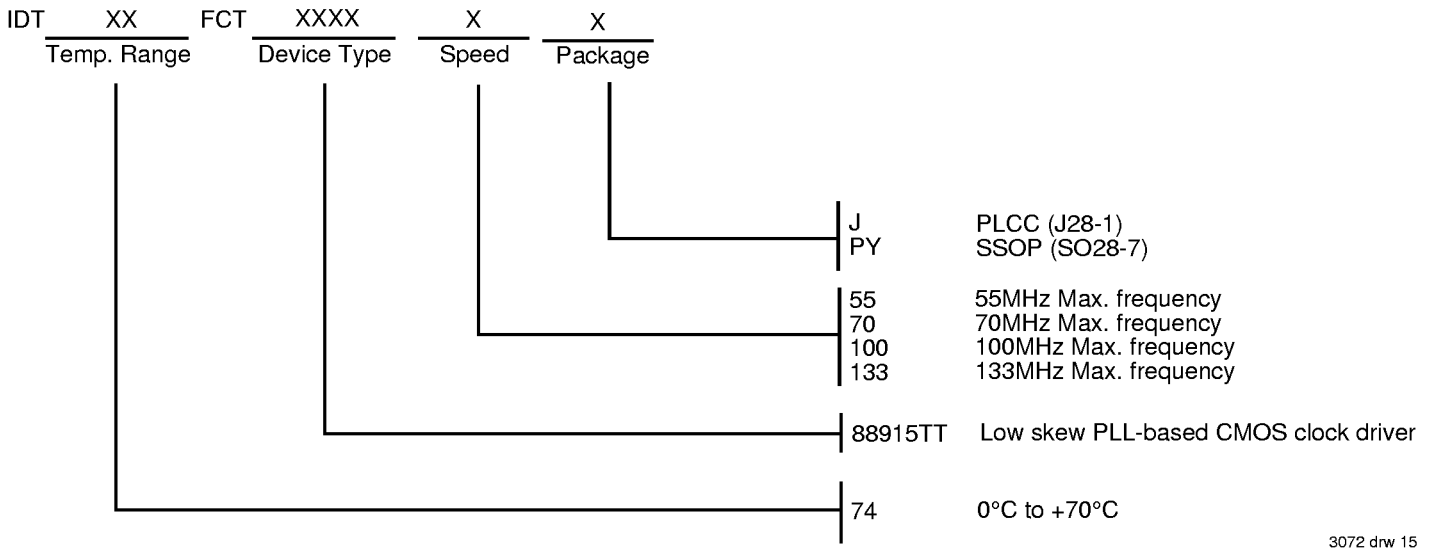
| Test | Switch |
|---|---|
| Disable Low<br>Enable Low | Closed |
| Disable High<br>Enable High | Open |

3072 tbl 10

**DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

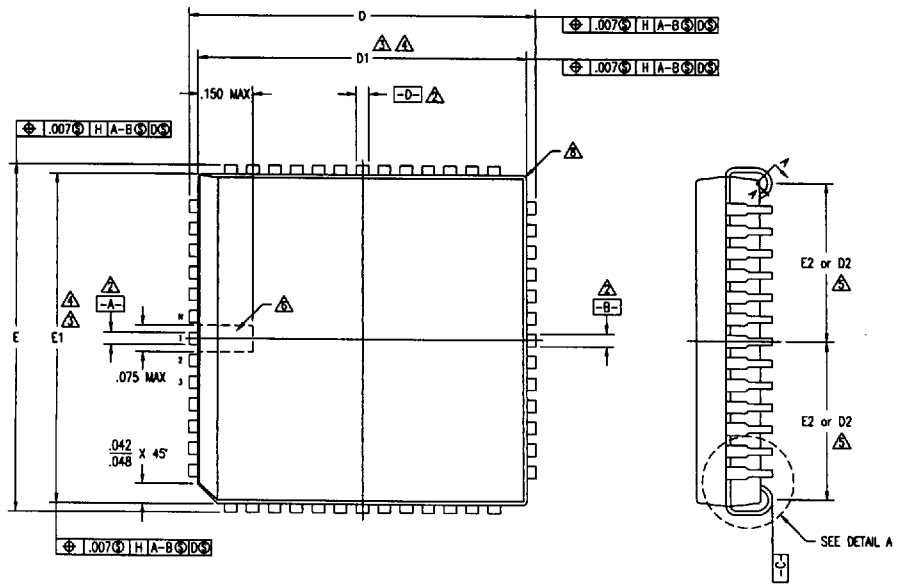
## ORDERING INFORMATION

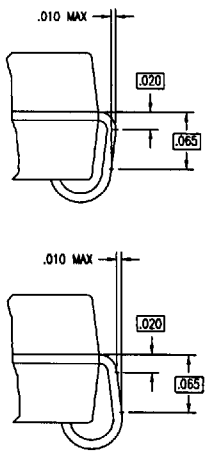



3072 drw 15

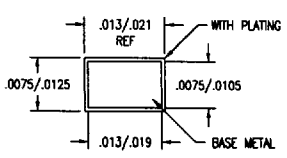
## PLCC

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 27647 | 06 | REDRAW TO JEDEC FORMAT | 03/15/95 | |




DETAIL A ⚠




SECTION A-A ⚠

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 |
|---|---|---|
| DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | |
| APPROVALS | DATE | TITLE PL PACKAGE OUTLINE<br>SQUARE PLCC<br>.050 PITCH |
| DRAWN dd | 08/15/88 | |
| CHECKED | | SIZE C DRAWING No. PSC-4008 REV 06 |
| | | DO NOT SCALE DRAWING |



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## PLCC (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 27647 | 06 | REDRAW TO JEDEC FORMAT | 03/15/95 | |

| DWG # | J28-1 | | | |
|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION AB | | | NOTE |
| | MIN | NOM | MAX | |
| A | .165 | .172 | .180 | |
| A1 | .095 | .105 | .115 | |
| A2 | .062 | – | .083 | |
| D | .485 | .490 | .495 | |
| D1 | .450 | .453 | .456 | 3,4 |
| D2 | .195 | .205 | .215 | 5 |
| E | .485 | .490 | .495 | |
| E1 | .450 | .453 | .456 | 3,4 |
| E2 | .191 | .205 | .219 | 5 |
| N | 28 | | | |

| DWG # | J44-1 | | | |
|---|---|---|---|---|
| JEDEC VARIATION AC | | | | NOTE |
| MIN | NOM | MAX | | |
| .165 | .172 | .180 | | |
| .095 | .105 | .115 | | |
| .062 | – | .083 | | |
| .685 | .690 | .695 | | |
| .650 | .653 | .656 | 3,4 | |
| .295 | .305 | .315 | 5 | |
| .685 | .690 | .695 | | |
| .650 | .653 | .656 | 3,4 | |
| .291 | .305 | .319 | 5 | |
| 44 | | | | |

| DWG # | J52-1 | | | |
|---|---|---|---|---|
| JEDEC VARIATION AD | | | | NOTE |
| MIN | NOM | MAX | | |
| .165 | .172 | .180 | | |
| .095 | .105 | .115 | | |
| .062 | – | .083 | | |
| .785 | .790 | .795 | | |
| .750 | .753 | .756 | 3,4 | |
| .345 | .355 | .365 | 5 | |
| .785 | .790 | .795 | | |
| .750 | .753 | .756 | 3,4 | |
| .341 | .355 | .369 | 5 | |
| 52 | | | | |

| DWG # | J68-1 | | | |
|---|---|---|---|---|
| JEDEC VARIATION AE | | | | NOTE |
| MIN | NOM | MAX | | |
| .165 | .172 | .180 | | |
| .095 | .105 | .115 | | |
| .062 | – | .083 | | |
| .985 | .990 | .995 | | |
| .950 | .953 | .956 | 3,4 | |
| .445 | .455 | .465 | 5 | |
| .985 | .990 | .995 | | |
| .950 | .953 | .956 | 3,4 | |
| .441 | .455 | .469 | 5 | |
| 68 | | | | |

| DWG # | J84-1 | | | |
|---|---|---|---|---|
| JEDEC VARIATION AF | | | | NOTE |
| MIN | NOM | MAX | | |
| .165 | .172 | .180 | | |
| .095 | .105 | .115 | | |
| .059 | – | .080 | | |
| 1.185 | 1.190 | 1.195 | | |
| 1.150 | 1.154 | 1.156 | 3,4 | |
| .545 | .555 | .565 | 5 | |
| 1.185 | 1.190 | 1.195 | | |
| 1.150 | 1.154 | 1.156 | 3,4 | |
| .541 | .555 | .569 | 5 | |
| 84 | | | | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

| TOLERANCES UNLESS SPECIFIED | | |
|---|---|---|
| DECIMAL | ANGULAR | |
| XX± | ± | |
| XXX± | | |
| XXXX± | | |

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

| APPROVALS | DATE |
|---|---|
| DRAWN AA | 06/15/95 |
| CHECKED | |

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

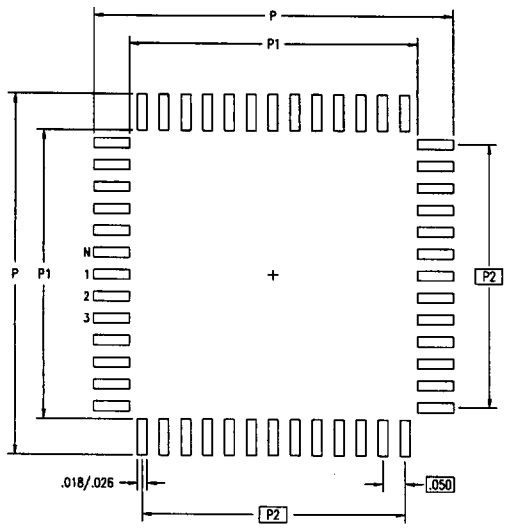
| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC-4008 | 06 |

DO NOT SCALE DRAWING

## PLCC (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 27647 | 08 | REDRAW TO JEDEC FORMAT | 03/15/95 | |

### LAND PATTERN DIMENSIONS

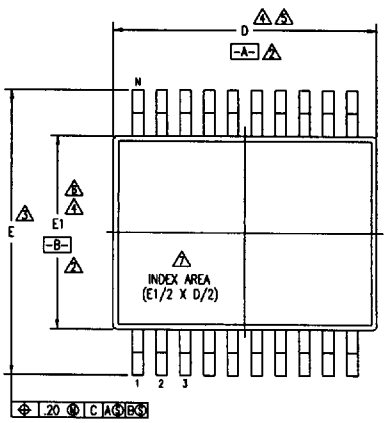


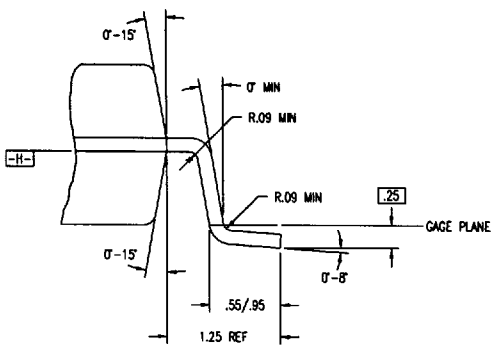

| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
|---|---|---|---|---|---|---|---|---|---|---|
| P | .520 | .528 | .720 | .728 | .820 | .828 | 1.020 | 1.028 | 1.220 | 1.228 |
| P1 | .354 | .362 | .554 | .562 | .654 | .662 | .854 | .862 | 1.054 | 1.062 |
| P2 | .300 BSC | | .500 BSC | | .600 BSC | | .800 BSC | | 1.000 BSC | |
| N | 28 | | 44 | | 52 | | 68 | | 84 | |

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | | |
| APPROVALS | DATE | TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH | |
| DRAWN dd | 08/15/89 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4008 REV 06 |
| | | DO NOT SCALE DRAWING | |

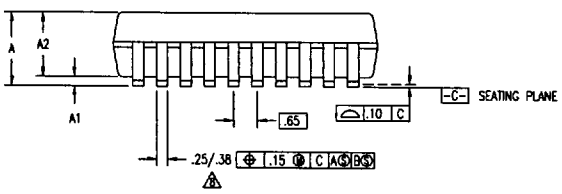
## SSOP (Continued)

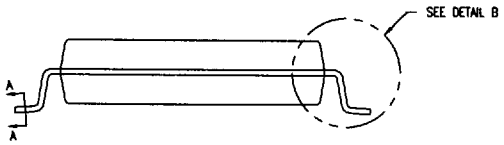
| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 20286 | 00 | INITIAL RELEASE | 04/15/91 | T. VU |
| 24536 | 01 | ADD 28 LD | 07/27/93 | T. VU |
| 27493 | 02 | REDRAW TO JEDEC FORMAT | 03/15/95 | |

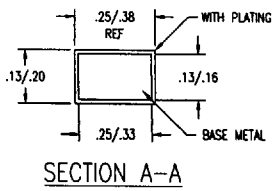



DETAIL B




SECTION A-A

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | | |
| APPROVALS | DATE | TITLE | PY PACKAGE OUTLINE 5.3 mm BODY WIDTH SSOP .65 mm PTICH |
| DRAWN AA | 04/15/91 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4032 REV 02 |
| | | DO NOT SCALE DRAWING | |



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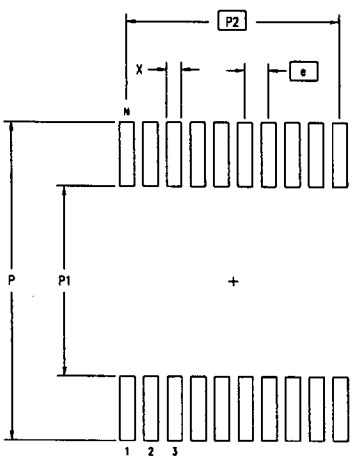
## SSOP (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 20288 | 00 | INITIAL RELEASE | 04/15/91 | T. VU |
| 24536 | 01 | ADD 28 LD | 07/27/93 | T. VU |
| 27493 | 02 | REDRAW TO JEDEC FORMAT | 03/15/95 | |

| DWG # | SO20-7 | | | | SO24-7 | | | | SO28-7 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION AE | | | NOTE | JEDEC VARIATION AG | | | NOTE | JEDEC VARIATION AH | | | NOTE |
| | MIN | NOM | MAX | | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | 1.73 | 1.86 | 1.99 | | 1.73 | 1.86 | 1.99 | | 1.73 | 1.86 | 1.99 | |
| A1 | .05 | .13 | .21 | | .05 | .13 | .21 | | .05 | .13 | .21 | |
| A2 | 1.68 | 1.73 | 1.78 | | 1.68 | 1.73 | 1.78 | | 1.68 | 1.73 | 1.78 | |
| D | 7.07 | 7.20 | 7.33 | 4,5 | 8.07 | 8.20 | 8.33 | 4,5 | 10.07 | 10.20 | 10.33 | 4,5 |
| E | 7.65 | 7.80 | 7.90 | 3 | 7.65 | 7.80 | 7.90 | 3 | 7.65 | 7.80 | 7.90 | 3 |
| E1 | 5.20 | 5.30 | 5.38 | 4,6 | 5.20 | 5.30 | 5.38 | 4,6 | 5.20 | 5.30 | 5.38 | 4,6 |
| N | 20 | | | | 24 | | | | 28 | | | |

### LAND PATTERN DIMENSIONS




| | MIN | MAX | MIN | MAX | MIN | MAX |
|---|---|---|---|---|---|---|
| P | 8.60 | 8.80 | 8.60 | 8.80 | 8.60 | 8.80 |
| P1 | 5.10 | 5.30 | 5.10 | 5.30 | 5.10 | 5.30 |
| P2 | 5.85 BSC | | 7.15 BSC | | 8.45 BSC | |
| X | .30 | .40 | .30 | .40 | .30 | .40 |
| e | .65 BSC | | .65 BSC | | .65 BSC | |
| N | 20 | | 24 | | 28 | |

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .20 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .20 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .13 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-150, VARIATION AE, AG & AH

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | | |
| APPROVALS | DATE | TITLE | PY PACKAGE OUTLINE 5.3 mm BODY WIDTH SSOP .65 mm PTICH |
| DRAWN dd | 04/15/91 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4032 REV 02 |
| | | DO NOT SCALE DRAWING | |



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