3.3V CMOS PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER WITH ASYNCHRONOUS RESET, 5 VOLT TOLERANT I/O

IDT74LVC161A

FEATURES:

- **0.5 MICRON CMOS Technology**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 3.3V ± 0.3V, Normal Range**
- **Vcc = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **All inputs, outputs, and I/Os are 5V tolerant**
- **Supports hot insertion**
- **Available in QSOP, SOIC, SSOP, and TSSOP packages**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Reduced system switching noise**

APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
- **Data communication and telecommunication systems**

DESCRIPTION:

The LVC161A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS-compatible TTL families.

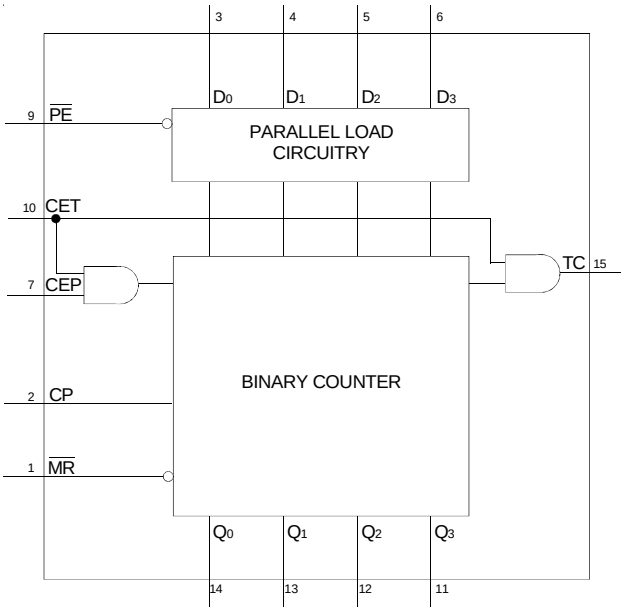
The LVC161A is a presettable synchronous binary counter which features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaniously on the positive-going edge of the clock (CP). Outputs (Q_0 to Q_3) of the counters may be preset to a high or low level. A low level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at the count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to low level regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be high to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a high output pulse of a duration approximately equal to a high level output of Q_0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

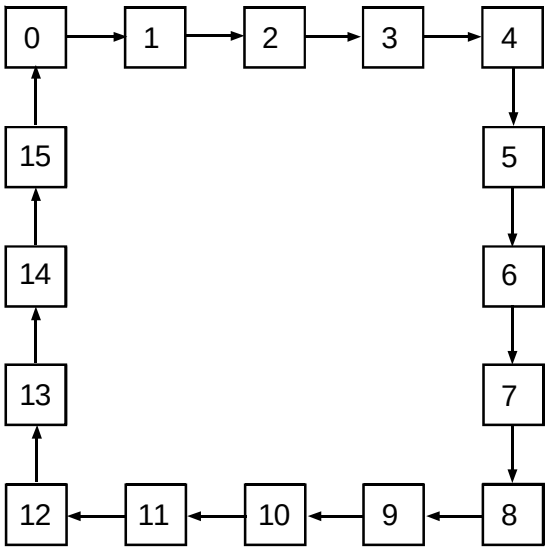
$$f_{max} = \frac{1}{tp_{(max)}\,(\text{CP to TC}) + t_{su}\,(\text{CEP to CP})}$$

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

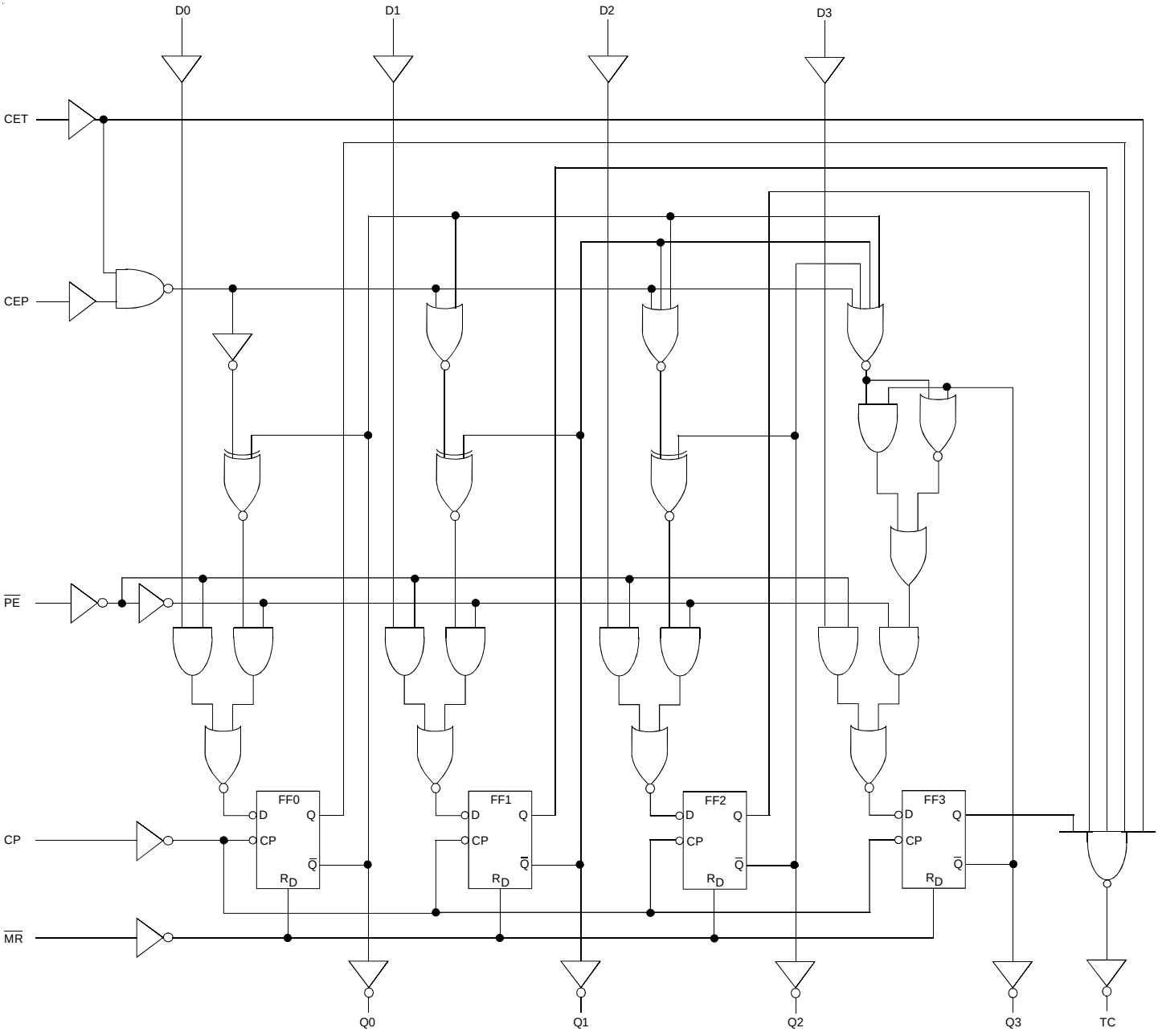
FUNCTIONAL DIAGRAM



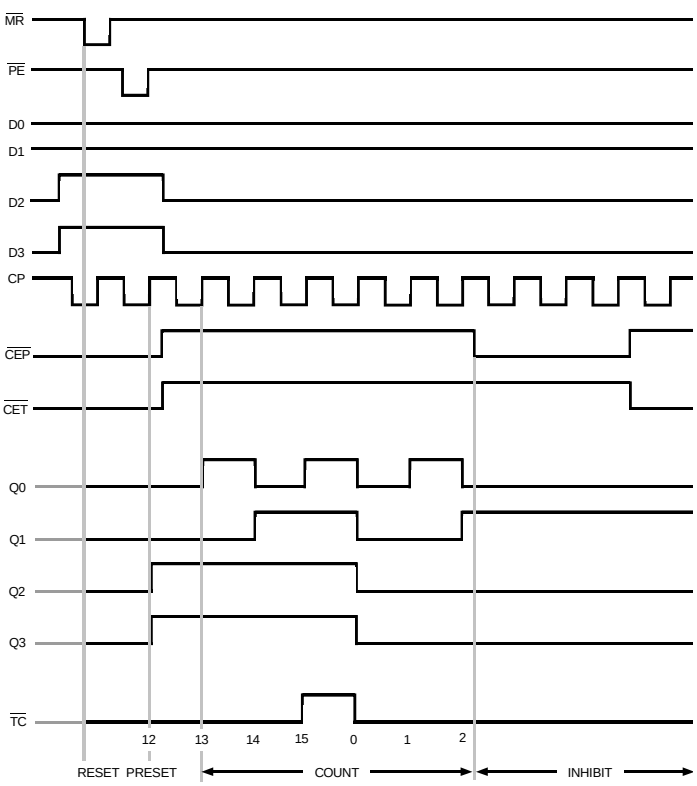
STATE DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



TYPICAL TIMING SEQUENCE



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

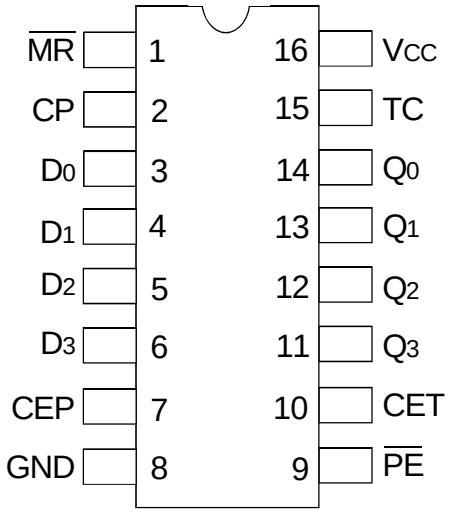
NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

NOTE:
1. As applicable to the device type.

PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{MR}$	Asynchronous Master Reset (Active LOW)
CP	Clock Input (LOW-to-HIGH, Edge-Triggered)
Dx	Data Inputs
CEP	Count Enable Inputs
GND	Ground (0V)
$\overline{PE}$	Parallel Enable Input (Active LOW)
CET	Count Enable Carry Input
Qx	Flip-Flop Outputs
TC	Terminal Count Output
Vcc	Positive Supply Voltage

FUNCTION TABLE (1)

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dx	Qx	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
Count	H	↑	h	h	h	X	count	*
Hold	H	X	l	X	h	X	Q(2)	*
(do nothing)	H	X	X	l	h	X	Q(2)	L

NOTE:

1. H = HIGH Voltage Level
   h = HIGH Voltage level one setup time prior to the LOW-to-HIGH clock transition.
   L = LOW Voltage Level
   l = LOW Voltage level one setup time prior to the LOW-to-HIGH clock transition.
   X = Don't care
   * = The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH).
   ↑ = LOW-to-HIGH clock transition
2. Indicates the state of the referenced output one set up time prior to the LOW-to-HIGH clock transition.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}(2)	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V, V_{IN} = GND or V_{CC}		—	—	10	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Clock Pin (CP) requires a minimum V_{IH} of 2.5V.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance	C_L = 0pF, f = 10Mhz	—	pF

SWITCHING CHARACTERISTICS[1]

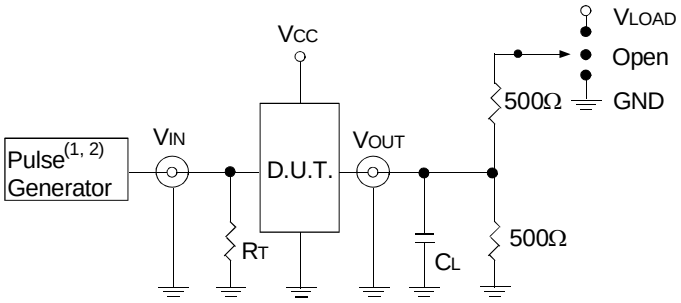
Symbol	Parameter	Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Qx	—	9	—	8	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC	—	11	—	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC	—	8.8	—	7.8	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to Qx	—	10	—	9	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	—	11	—	10	ns
t_W	Clock Pulse Width, HIGH or LOW	5	—	4	—	ns
t_W	Master Reset Width LOW	4	—	3	—	ns
t_{REM}	Removal Time, $\overline{MR}$ to CP	0.5	—	0.5	—	ns
t_{SU}	Set-Up Time, Dx to CP	3.5	—	3	—	ns
t_{SU}	Set-Up Time, $\overline{PE}$ to CP	3.5	—	3	—	ns
t_{SU}	Set-Up Time, CEP, CET to CP	5.5	—	5	—	ns
t_H	Hold Time, Dx, $\overline{PE}$, CEP, CET to CP	0	—	0	—	ns
$t_{SK}(o)$	Output Skew[2]	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2 Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 2.5V±0.2V	$V_{CC}^{(2)}$= 3.3V±0.3V & 2.7V	Unit
V_{LOAD}	2 x Vcc	6	V
V_{IH}	Vcc	2.7	V
V_T	Vcc / 2	1.5	V
V_{LZ}	150	300	mV
V_{HZ}	150	300	mV
C_L	30	50	pF



LVC QUAD Link

Test Circuit for All Outputs

DEFINITIONS:

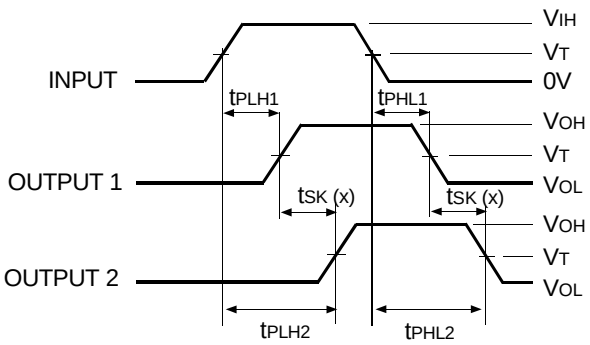
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open



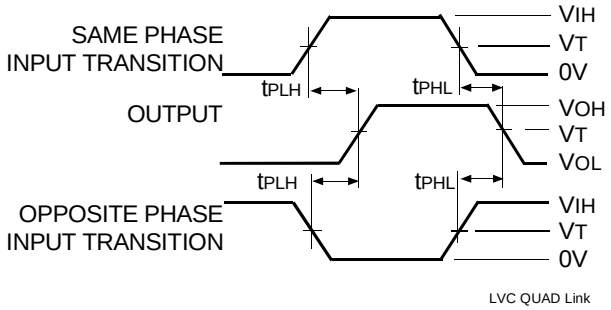
$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

LVC QUAD Link

Output Skew - $t_{SK(x)}$

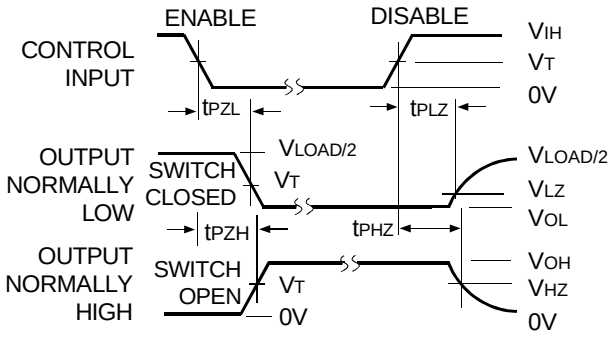
NOTES:

1. For $t_{SK(o)}$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK(b)}$ OUTPUT1 and OUTPUT2 are in the same bank.



LVC QUAD Link

Propagation Delay

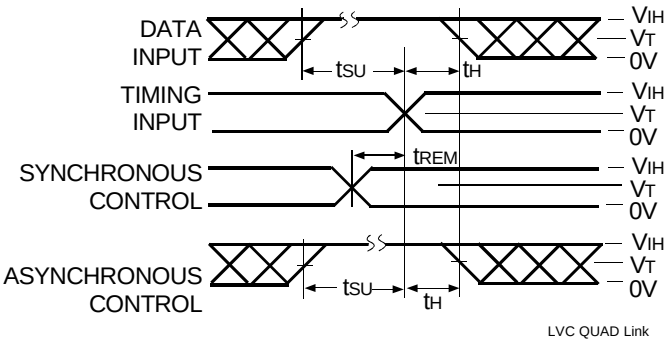


LVC QUAD Link

NOTE:

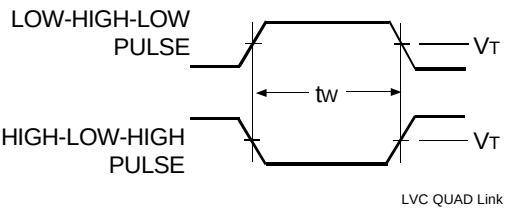
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



LVC QUAD Link

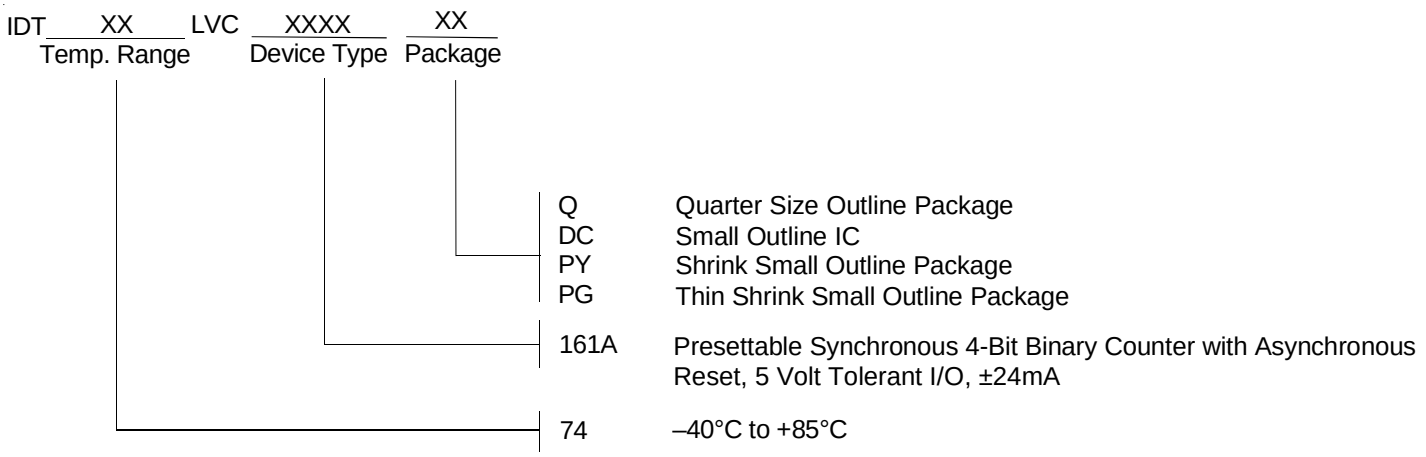
Set-up, Hold, and Release Times



LVC QUAD Link

Pulse Width

ORDERING INFORMATION



Q	Quarter Size Outline Package
DC	Small Outline IC
PY	Shrink Small Outline Package
PG	Thin Shrink Small Outline Package
161A	Presettable Synchronous 4-Bit Binary Counter with Asynchronous Reset, 5 Volt Tolerant I/O, ±24mA
74	–40°C to +85°C

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