REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. Editorial changes throughout. - gap	00-11-30	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	A																			
SHEET	15																			

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
90-03-27

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 16K X 4 SRAM WITH OE, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-89892**

SHEET 1 OF 15

DSCC FORM 2233
APR 97

5962-E016-01

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89892	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	4C198L-25	16K X 4 Static RAM with $\overline{OE}$	25 ns (data retention)
02	4C198-25		25 ns
03	4C198L-20		20 ns (data retention)
04	4C198-20		20 ns
05	4C198L-15		15 ns (data retention)
06	4C198-15		15 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
X	CQCC3-N28	28	leadless chip carrier package
Y	CQCC4-N28	28	leadless chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc 1/
DC output current	20 mA
Ambient storage temperature	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, X, and Y	See MIL-STD-1835
Power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc 1/
Ground voltage (V_{SS}) (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc to VCC +0.5 V dc
Input low voltage (V_{IL})	-0.5 V dc to 0.8 V dc 2/
Operating case temperature range (T_C)	-55°C to +125°C

1/ All voltages referenced to V_{SS}.
2/ V_{IL} negative undershoots to a minimum of -2.0 V dc are allowed with a maximum 20 ns pulse width.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity. Samples may be pulled anytime after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535,
appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{CC} = max, V_{IN} = GND to V_{CC}	1, 2, 3	All		±10	µA
Output leakage current	I_{LO}	V_{CC} = max, V_{OUT} = GND to V_{CC}, $\overline{CE} \ge V_{IH}$, $\overline{WE} \le V_{IL}$	1, 2, 3	All		±10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, outputs open, V_{CC} = max, f = $1/t_{AVAV}$	1, 2, 3	01, 03		120	mA
				02, 04		130	
				05, 06		150	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, outputs open, V_{CC} = max, f = 0 MHz	1, 2, 3	01, 03, 05		20	mA
				02, 04, 06		50	
Standby power supply current (CMOS)	I_{CC3}	V_{CC} +0.2 V ≥ $\overline{CE}$ ≥ V_{CC} -0.2 V, outputs open, V_{CC} +0.2 V ≥ $V_{IN} \ge V_{CC}$ -0.2 V or +0.2 V ≥ $V_{IN} \ge$ -0.2 V, f = 0 MHz	1, 2, 3	01, 03, 05		5	mA
				02, 04, 06		20	
Data retention current 1/	I_{CC4}	$V_{CC} = V_{DR}$ = 2.0 V	1, 2, 3	01, 03, 05		600	µA
Input capacitance 1/	C_{IN}	V_I = 0 V f = 1 MHz, T_A = +25°C, See 4.3.1c	4	All		10	pF
Output capacitance 1/	C_{OUT}	V_O = 0 V f = 1 MHz, T_A = +25°C, See 4.3.1c	4	All		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}		9, 10, 11	01, 02	25		ns
				03, 04	20		
				05, 06	15		
Address cycle time	t_{AVQV}		9, 10, 11	01, 02		25	ns
				03, 04		20	
				05, 06		15	
Chip enable access time	t_{ELQV}		9, 10, 11	01, 02		25	ns
				03, 04		20	
				05, 06		15	
Output hold from address change	t_{AVQX}		9, 10, 11	All	3		ns
Output enable to output valid	t_{OLQV}		9, 10, 11	01, 02	15		ns
				03, 04	12		
				05, 06	10		
Chip select to output in low Z 1/ 4/	t_{ELQX}		9, 10, 11	All	3		ns
Output enable to output in low Z 1/ 4/	t_{OLQX}		9, 10, 11	All	3		ns
Chip select to output in high Z 1/ 4/	t_{EHQZ}		9, 10, 11	01-04		15	ns
				05-06		10	
Output disable to output in high Z 1/ 4/	t_{OHQZ}		9, 10, 11	All		10	ns

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write enable to output in high Z 1/ 4/	t_{WLQZ}		9, 10, 11	01, 02		15	ns
				03, 04		12	
				05, 06		10	
Data valid to end of write	t_{DVWH}		9, 10, 11	01, 02	15		ns
				03, 04	12		
				05, 06	10		
Data hold time	t_{WHDX}		9, 10, 11	All	0		ns
Output active from end of write 1/ 4/	t_{WHQX}		9, 10, 11	All	3		ns
Write cycle time 1/	t_{AVAV}		9, 10, 11	01, 02	25		ns
				03, 04	20		
				05, 06	15		
Chip select to end of write	t_{ELWH}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	12		
Address valid to end of write	t_{AVWH}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	12		
Address setup time	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width	t_{WLWH}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	12		
Write recovery time	t_{EHAX}		9, 10, 11	01-06	0		ns
Chip deselect to data retention time	t_{CDR}		9, 10, 11	01, 03, 05	0		ns
Operation recovery time	t_R		9, 10, 11	01, 03, 05	t_{AVAV}		ns

1/ This parameter tested initially and after any design or process change which could affect this parameter, and is therefore guaranteed to the limits specified in table I.
2/ For timing waveforms, see figure 3.
3/ AC parameters are tested using input rise and fall times of 5 ns and input pulse levels of GND to 3.0 V. Both input and output timing reference levels are 1.5 V, and the output load is shown on figure 4.
4/ Transition is measured ±500 mV from steady state.

Device types	01 through 06	
Case outlines	K and L	X and Y
Terminal number	Terminal symbol	
1	A_0	NC
2	A_1	NC
3	A_2	A_0
4	A_3	A_1
5	A_4	A_2
6	A_5	A_3
7	A_6	A_4
8	A_7	A_5
9	A_8	A_6
10	$\overline{CE}$	A_7
11	$\overline{OE}$	A_8
12	GND	$\overline{CE}$
13	$\overline{WE}$	$\overline{OE}$
14	I/O_1	GND
15	I/O_2	NC
16	I/O_3	$\overline{WE}$
17	I/O_4	I/O_1
18	NC	I/O_2
19	A_9	I/O_3
20	A_{10}	I/O_4
21	A_{11}	A_9
22	A_{12}	A_{10}
23	A_{13}	A_{11}
24	V_{CC}	A_{12}
25	---	A_{13}
26	---	NC
27	---	NC
28	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

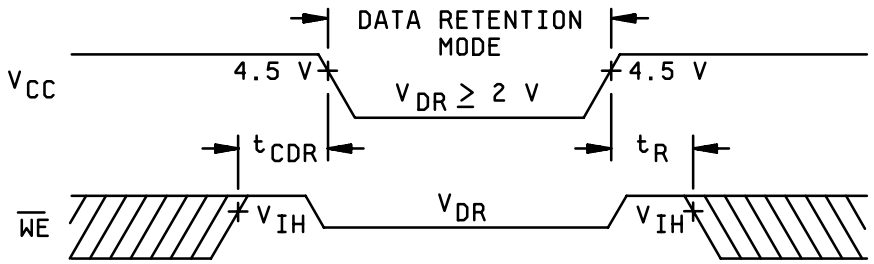
Device types 01 through 06

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Not selected	High Z	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 2. Truth table.

LOW V_{CC} DATA RETENTION WAVEFORM
(DEVICE TYPES 01,03,AND 05)



TIMING WAVEFORM OF READ CYCLE

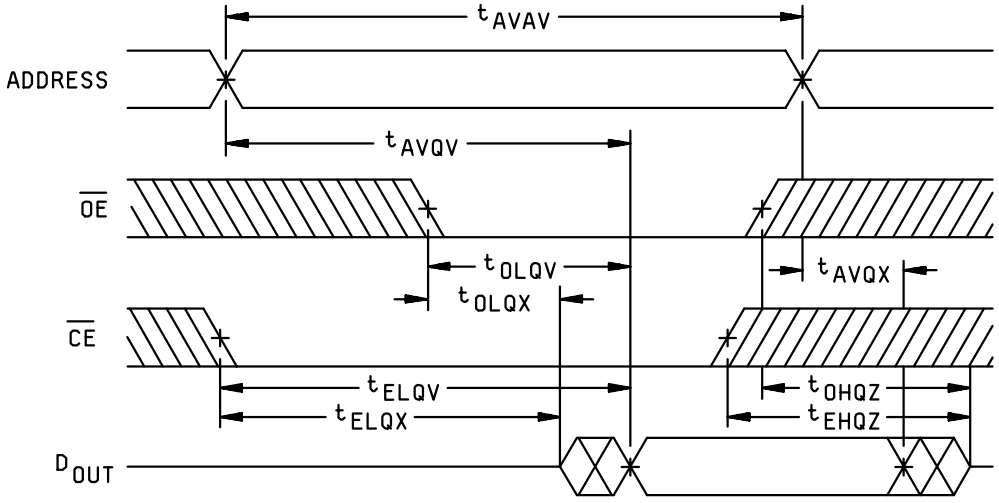


FIGURE 3. Switching time waveforms.

TIMING WAVEFORM OF WRITE CYCLE NO.1

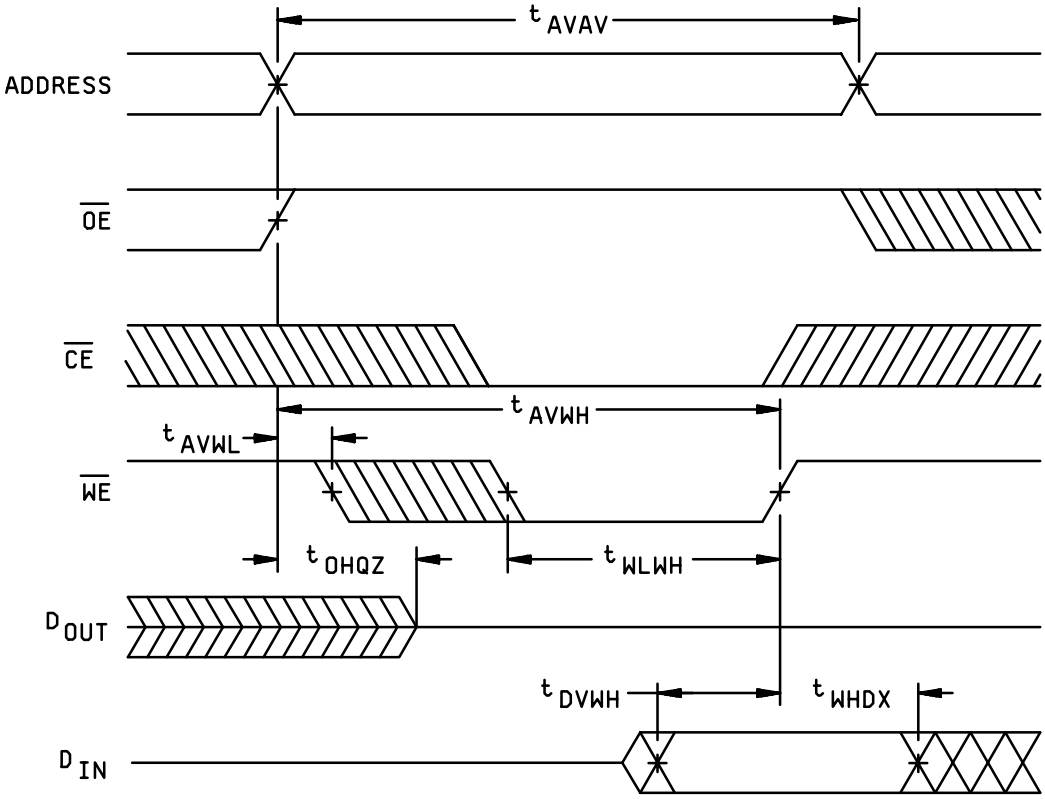


FIGURE 3. Switching time waveforms - Continued.

TIMING WAVEFORM OF WRITE CYCLE NO.2

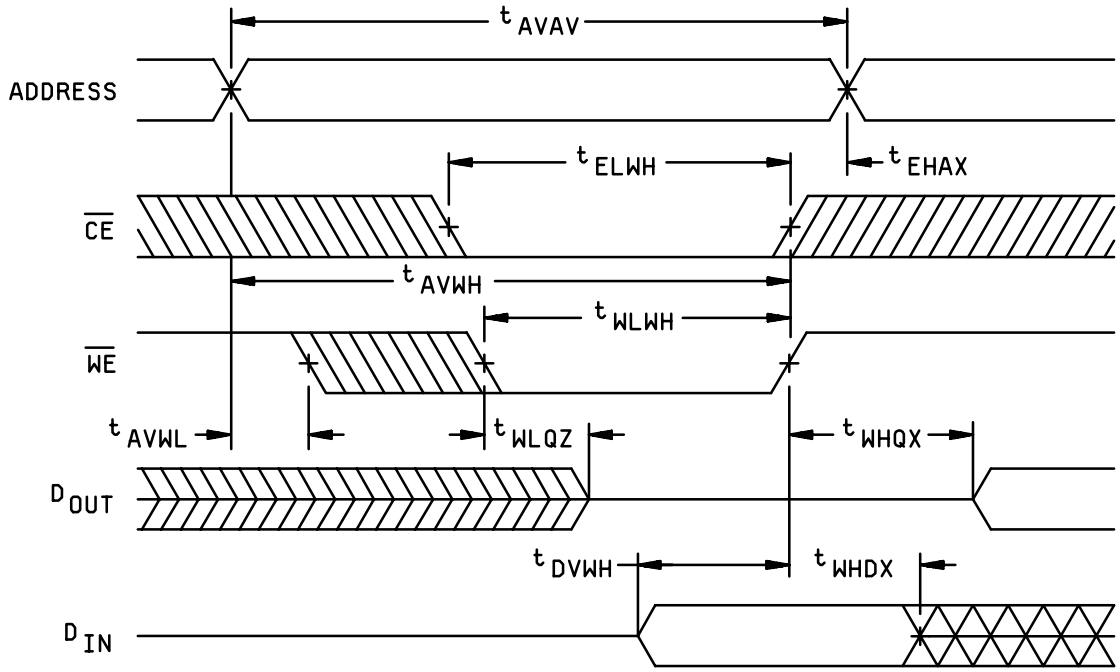
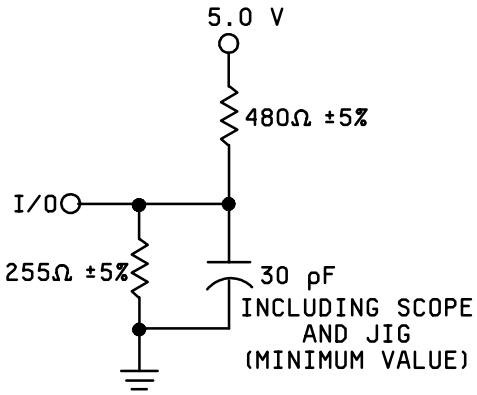
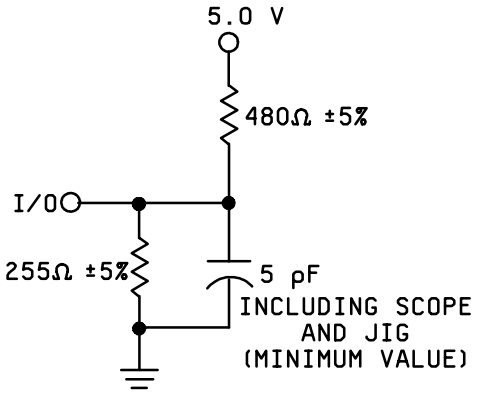


FIGURE 3. Switching time waveforms - Continued.



CIRCUIT A OR EQUIVALENT



CIRCUIT B OR EQUIVALENT

FOR (t_{ELQX}, t_{OLQX}, t_{EHQZ}, t_{OHQZ}, t_{WLQZ}, t_{WHQX})

FIGURE 4. Output loads circuits.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005,table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, (8A, 8B)***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.
*** See 4.3.1d.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-11-30

Approved sources of supply for SMD 5962-89892 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8989201KA	75569	P4C198L-25FMB
5962-8989201LA	75569	P4C198L-25DMB
	3/	6198L25CB
5962-8989201XA	75569	P4C198L-25LMB
	3/	6198L25L28B
5962-8989201YA	75569	P4C198L-25L1MB
5962-8989202KA	75569	P4C198-25FMB
	3/	CY7C166A-25KMB
5962-8989202LA	75569	P4C198-25DMB
	3/	6198S25CB
	3/	CY7C166A-25DMB
5962-8989202XA	75569	P4C198-25LMB
	3/	6198S25L28B
	3/	CY7C166A-25LMB
5962-8989202YA	75569	P4C198-25L1MB
	3/	CY7C166A-25LMB
5962-8989203KA	75569	P4C198L-20FMB
5962-8989203LA	75569	P4C198L-20DMB
	3/	6198L20CB
5962-8989203XA	75569	P4C198L-20LMB
	3/	6198L20L28B
5962-8989203YA	75569	P4C198L-20L1MB
5962-8989204KA	75569	P4C198-20FMB
	3/	CY7C166A-20KMB
5962-8989204LA	75569	P4C198-20DMB
	3/	6198S20CB
	3/	CY7C166A-20DMB
5962-8989204XA	75569	P4C198-20LMB
	3/	6198S20L28B
	3/	CY7C166A-20LMB
5962-8989204YA	75569	P4C198-20L1MB
	3/	CY7C166A-20LMB
5962-8989205KA	75569	P4C198L-15FMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8989205LA	75569	P4C198L-15DMB
	3/	6198L15CB
5962-8989205XA	75569	P4C198L-15LMB
	3/	6198L15L28B
5962-8989205YA	75569	P4C198L-15L1MB
5962-8989206KA	75569	P4C198-15FMB
5962-8989206LA	75569	P4C198-15DMB
	3/	6198S15CB
5962-8989206XA	75569	P4C198-15LMB
	3/	6198S15L28B
5962-8989206YA	75569	P4C198-15L1MB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
75569	Performance Semiconductor Corporation 630 East Weddell Drive Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.