T-46-07-09

MC54/74HC173

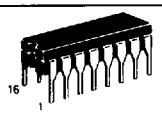
Quad 3-State D Flip-Flop with Common Clock and Reset

High-Performance Silicon-Gate CMOS

The MC54/74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip-flops with the rising edge of the common Clock. When either or both of the Output Enable Controls is high, the outputs are in a high-impedance state. This feature allows the HC173 to be used in bus-oriented systems. The Reset feature is asynchronous and active-high.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 208 FETs or 52 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-06

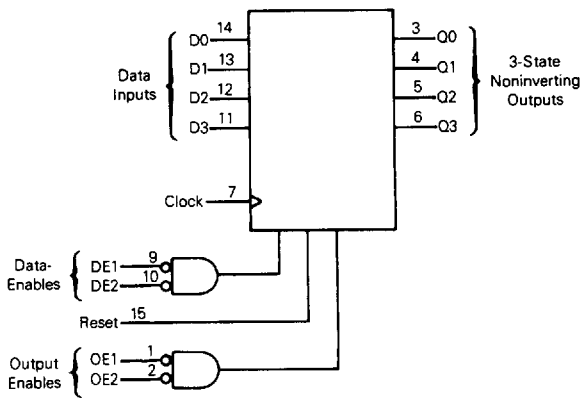
D SUFFIX
SOIC
CASE 751B-04

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

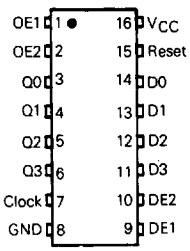
T_A = −55° to 125°C for all packages.
Dimensions in Chapter 6.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs							Output
Output Enables				Data Enables		Data	
OE1	OE2	Reset	Clock	DE1	DE2	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	no change
L	L	L	H	X	X	X	no change
L	L	L	↓	H	X	X	no change
L	L	L	↓	X	H	X	no change
L	L	L	↓	L	L	L	L
L	L	L	↓	L	L	H	H
L	L	L	↑	X	X	X	no change
L	H	X	X	X	X	X	high impedance
H	L	X	X	X	X	X	high impedance
H	H	X	X	X	X	X	high impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Figure 1)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\| \le 7.8$ mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 7.8$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 35	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input D or DE to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Clock to Input D or DE (Figure 4)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

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PIN DESCRIPTIONS

INPUTS

D0, D1, D2, D3 (PINS 14, 13, 12, 11) — 4-bit data inputs. Data on these pins, when enabled by the Data-Enable Controls, are entered into the flip-flops on the rising edge of the clock.

CLOCK (PIN 7) — Clock input.

OUTPUTS

Q0, Q1, Q2, Q3 (PINS 3, 4, 5, 6) — 3-state register outputs. During normal operation of the device, the outputs of the D flip-flops appear at these pins. During 3-state operation, these outputs assume a high-impedance state.

CONTROL INPUTS

RESET (PIN 15) — Asynchronous reset input. A high level on this pin resets all flip-flops and forces the Q outputs low, if they are not already in high-impedance state.

DE1, DE2 (Pins 9, 10) — Active-low Data Enable Control inputs. When both Data Enable Controls are low, data at the D inputs are loaded into the flip-flops with the rising edge of the Clock input. When either or both of these controls are high, there is no change in the state of the flip-flops, regardless of any changes at the D or Clock inputs.

OE1, OE2 (Pins 1, 2) — Output Enable Control inputs. When either or both of the Output Enable Controls are high, the Q outputs of the device are in the high-impedance state. When both controls are low, the device outputs display the data in the flip-flops.

SWITCHING WAVEFORMS

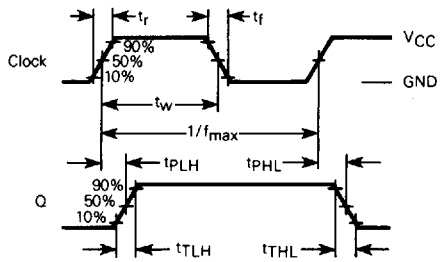


Figure 1.

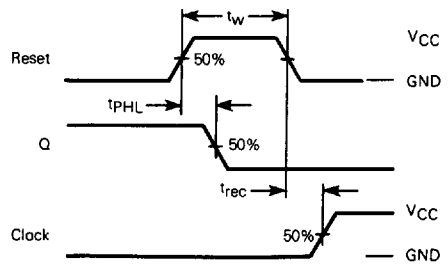


Figure 2.

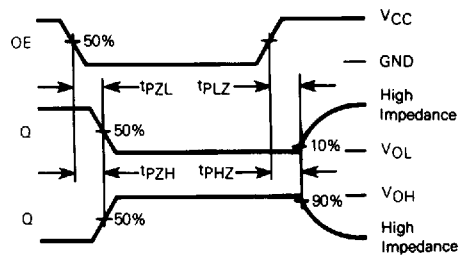


Figure 3.

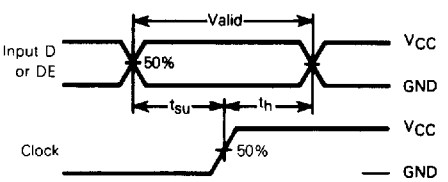
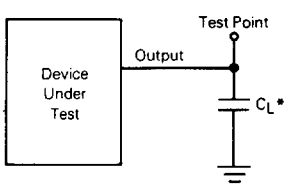


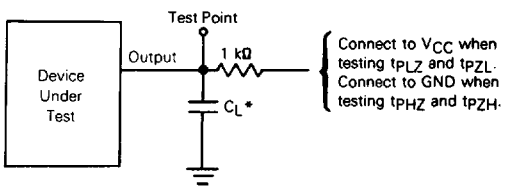
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance.

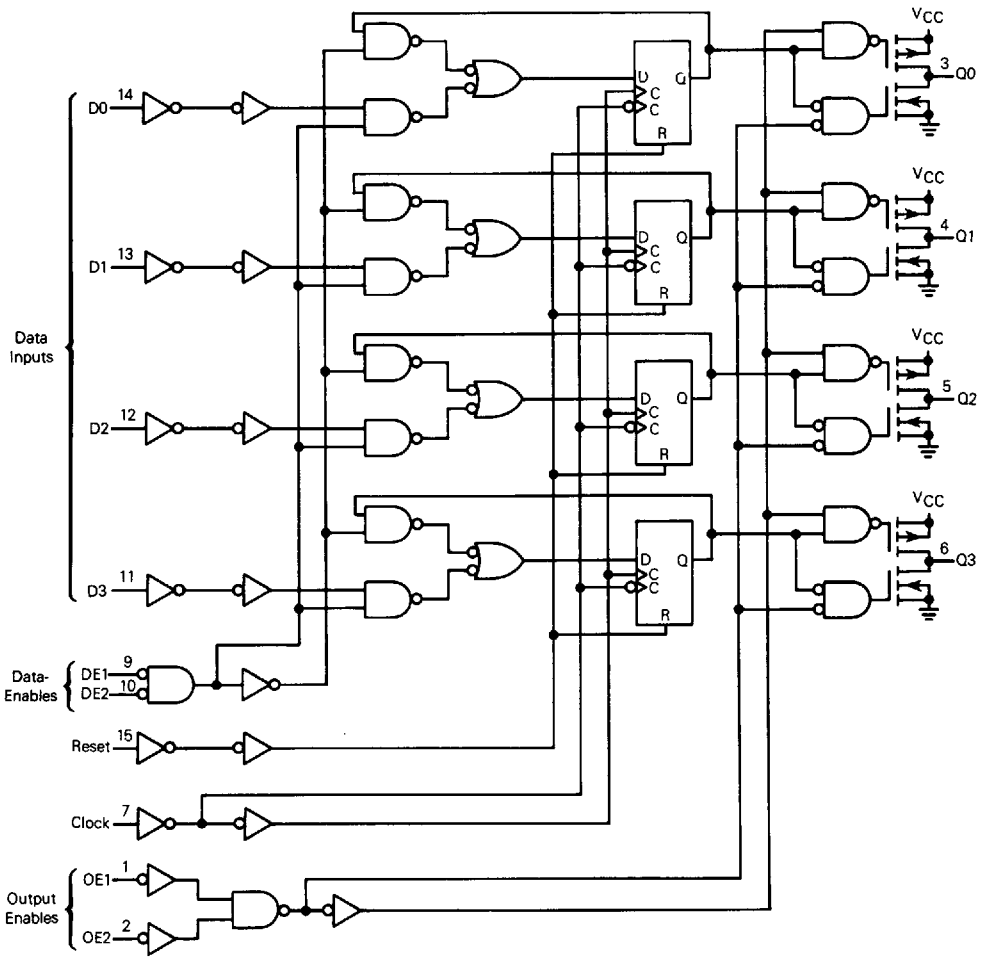
Figure 5.



* Includes all probe and jig capacitance.

Figure 6.

LOGIC DETAIL



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