MOTOROLA

Military 54F74

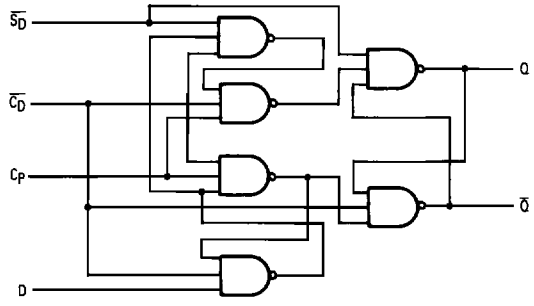
Quad D-Type Positive Edge-Triggered Flip-Flop

ELECTRICALLY TESTED PER: MIL-M-38510/34101

The 54F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the clock Pulse input.

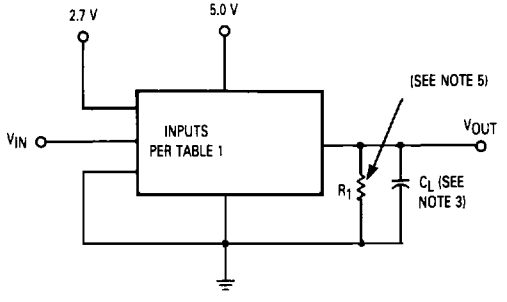
Asynchronous Inputs:
- LOW Input to $\overline{S_D}$ sets Q to HIGH level
- LOW Input to $\overline{C_D}$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C_D}$ and $\overline{S_D}$ makes both Q and $\overline{Q}$ HIGH

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC TEST CIRCUIT



AVAILABLE AS:

1) JAN: JM38510/34101BXA
2) SMD: *
3) 883C: 54F74/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
*Call Factory for latest update

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{CD}1$	1	1	2	GND
D1	2	2	3	V_{CC}
CP1	3	3	4	V_{CC}
$\overline{SD}1$	4	4	6	V_{CC}
Q1	5	5	8	OPEN
$\overline{Q}1$	6	6	9	OPEN
GND	7	7	10	GND
$\overline{Q}2$	8	8	12	OPEN
Q2	9	9	13	OPEN
$\overline{SD}2$	10	10	14	V_{CC}
CP2	11	11	16	V_{CC}
D2	12	12	18	V_{CC}
$\overline{CD}2$	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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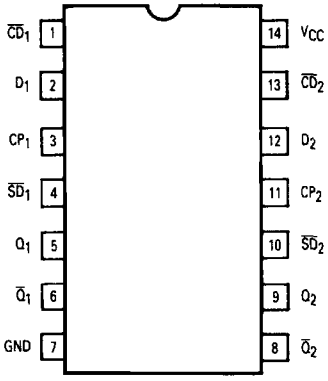
MODE SELECT — TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

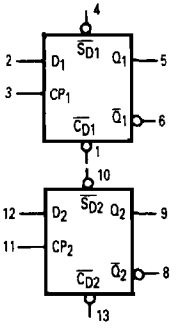
*Both outputs will be HIGH when both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

CONNECTION DIAGRAM

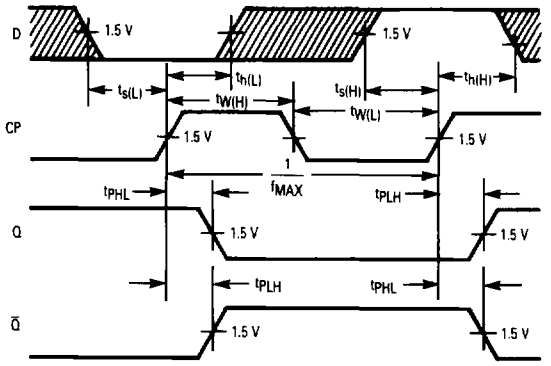


LOGIC SYMBOLS



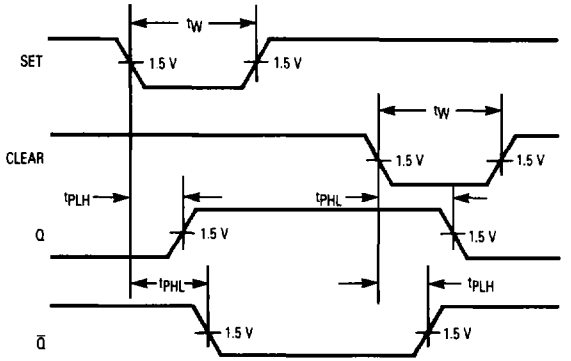
AC WAVEFORMS

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths



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Symbol	Parameter		Limits						Units	Test Condition (Unless Otherwise Specified)	
			+25°C		+125°C		−55°C				
	Static Parameters:		Subgroup 1		Subgroup 2		Subgroup 3				
			Min	Max	Min	Max	Min	Max			
V_{OH}	Logical "1" Output Voltage		2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 2.0 V, V_{IL} = 0.8 V.	
V_{OL}	Logical "0" Output Voltage			0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V.	
V_{IC}	Input Clamping Voltage			−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.	
I_{IH}	Logical "1" Input Current			20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 4.5 V, D & CP = 0 V, CD = 2.7 V.	
I_{IHH}	Logical "1" Input Current			100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, D & CP = 0 V, CD = 4.5 V.	
I_{IL}	Logical "0" Input Current	CP,D	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, SD = 0 V, CP = 4.5 V.	CD = 4.5 V.
		CD,SD	−0.09	−1.8	−0.09	−1.8	−0.09	−1.8			D = 4.5 V.
I_{OD}	Diode Current		60		60		60		mA	V_{CC} = 5.5 V, CD = 0 V, SD = 5.5 V, other inputs are open, V_{OUT} = 2.5 V.	
I_{OS}	Output Short Circuit Current		−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, SD = 0 V, other inputs are open, V_{OUT} = 0 V.	
I_{CC}	Power Supply Current			16		16		16	mA	V_{CC} = 5.5 V, CD = 5.5 V, other inputs = 0 V.	
V_{IH}	Logical "1" Input Voltage		2.0		2.0		2.0		V	V_{CC} = 4.5 V.	
V_{IL}	Logical "0" Input Voltage			0.8		0.8		0.8	V	V_{CC} = 4.5 V.	
			Subgroup 7		Subgroup 8A		Subgroup 8B				
	Functional Tests									per Truth Table with V_{CC} = 4.5 V, (Repeat at), V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.	

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q or $\overline{Q}$	4.4	8.0	3.8	10.5	3.8	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PLH1}	Propagation Delay /Data-Output CP to Q or $\overline{Q}$	3.8	6.8	3.8	8.5	3.8	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output CP to Q or $\overline{Q}$	4.4	8.0	3.8	10.5	3.8	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output CP to Q or $\overline{Q}$	3.8	6.8	3.8	8.5	3.8	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PHL3}	Propagation Delay /Data-Output $\overline{CD}$ to Q or $\overline{Q}$	3.5	9.0	3.2	11.5	3.2	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PLH3}	Propagation Delay /Data-Output $\overline{CD}$ to Q or $\overline{Q}$	3.2	6.1	3.2	8.0	3.2	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PHL4}	Propagation Delay /Data-Output $\overline{SD}$ to Q or $\overline{Q}$	3.5	9.0	3.5	11.5	3.5	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_{PLH4}	Propagation Delay /Data-Output $\overline{SD}$ to Q or $\overline{Q}$	3.2	6.1	3.2	8.0	3.2	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
f_{MAX}	Maximum Clock Frequency	100		80		80		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 499 Ω ± 5.0%.
t_s (H)	Set Up Time D High or Low to CP	3.0		3.0		3.0		ns	V_{CC} = 5.0 V, C_L = 50 pF. (Information only, No Testing Required).
t_s (L)		4.0		4.0		4.0			
t_h (H)	Hold Time D High or Low to CP	2.0		2.0		2.0		ns	V_{CC} = 5.0 V, C_L = 50 pF, (Information only, No Testing Required).
t_h (L)									
t_{rec}	Recovery Time SD or CD to CP	3.0		3.0		3.0		ns	V_{CC} = 5.0 V, C_L = 50 pF. (Information only, No Testing Required).

NOTES:
1. V_{IN} = Input pulse has the following characteristics:
   $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, or as specified in table 1, PRR (Subgroups 10 and 11) have a duty cycle 50 ± 15%, t_p = 5.0 ns (min).
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. R_1 = 499 Ω ± 5.0%.
6. When testing f_{MAX} the output frequency shall be 1/2 the input frequency, f_{MAX} minimum limit specified is the frequency of the input pulse.
7. Clock, Clear and Set inputs need to be in the proper configuration for specified output conditions.