TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

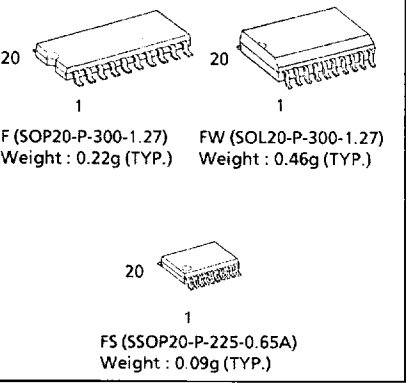
TC74VHCT540F, TC74VHCT540FW, TC74VHCT540FS
TC74VHCT541F, TC74VHCT541FW, TC74VHCT541FS

OCTAL BUS BUFFER
TC74VHCT540F/FW/FS INVERTED, 3-STATE OUTPUTS
TC74VHCT244F/FW/FS NON-INVERTED, 3-STATE OUTPUTS

The TC74VHCT540, 541 are advanced high speed CMOS OCTAL BUS BUFFFERs fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
The TC74VHCT540 is an inverting type and, The TC74VHCT541 is a non-inverting type.
When either $\overline{G}1$ or $\overline{G}2$ are high, the terminal outputs are in the high - impedance state.
The input voltage are compatible with TTL output voltage.
These devices may be used as a level converter for interfacing 3.3V to 5V system.
Input protection and output circuit ensure that 0 to 7V can be applied to the input and output pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

FEATURES:

- High Speed ..... t_{pd} = 5.4ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Low Noise ····· V_{OLP} = 1.6V (Max.)
- Pin and Function Compatible with 74ALS540/541



F (SOP20-P-300-1.27)
Weight : 0.22g (TYP.)

FW (SOL20-P-300-1.27)
Weight : 0.46g (TYP.)

FS (SSOP20-P-225-0.65A)
Weight : 0.09g (TYP.)

APPLICATION NOTE

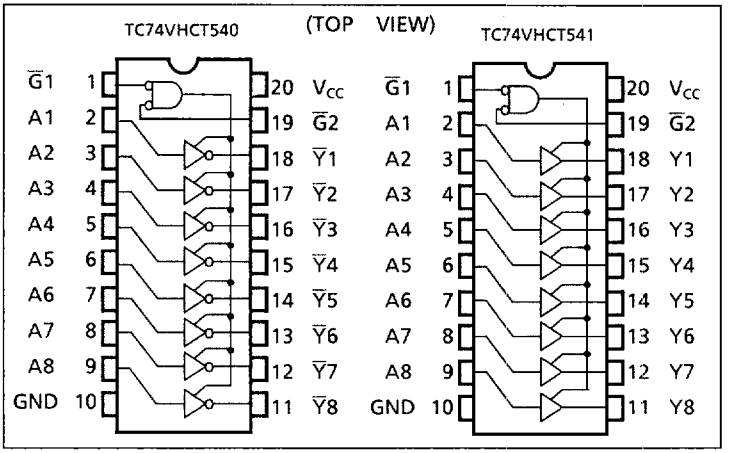
These devices can drive components with CMOS input level by adding a external pull up resistor to output terminal.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}1$	$\overline{G}2$	A_n	Y_n	$\overline{Y}_n$
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

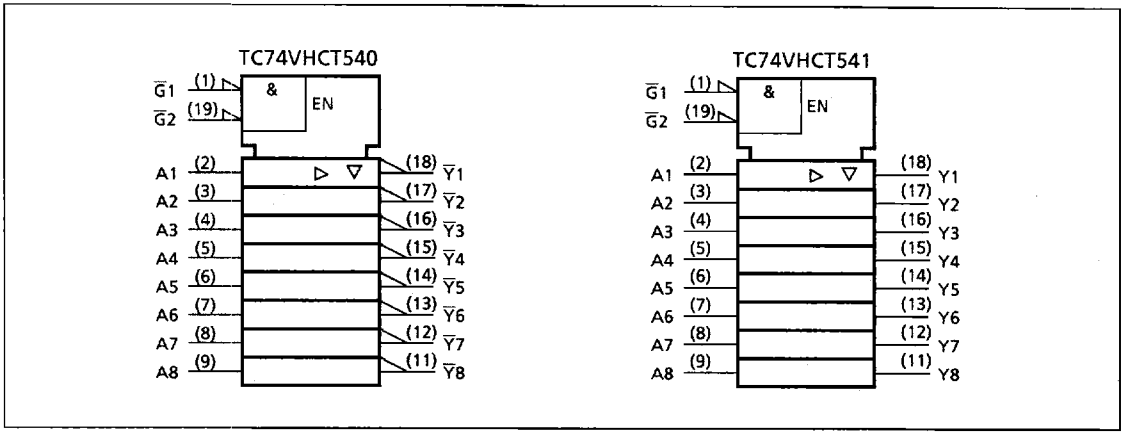
X : Don't Care
Z : High Impedance
Y_n : TC74VHCT541
$\overline{Y}_n$: TC74VHCT540

PIN ASSIGNMENT



961001EBA2

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	−20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~20	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	3.15	3.65	—	3.15	—	V
			I_{OH} = −8mA	4.5	2.50	—	—	2.40	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.10	—	0.10	V
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	
	I_{CCT}	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I_{OPD}	V_{OUT} = 5.5V		0	—	—	+0.5	—	+5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (TC74VHCT540)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	5.4	7.4	1.0	8.5	ns
				50	—	5.9	8.4	1.0	9.5	
Propagation Delay Time (TC74VHCT541)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	5.0	6.9	1.0	8.0	
				50	—	5.5	7.9	1.0	9.0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L = 1kΩ	5.0 ± 0.5	15	—	8.3	11.3	1.0	13.0	
				50	—	8.8	12.3	1.0	14.0	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	5.0 ± 0.5	50	—	9.4	11.9	1.0	13.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	9	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 2)			—	19	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

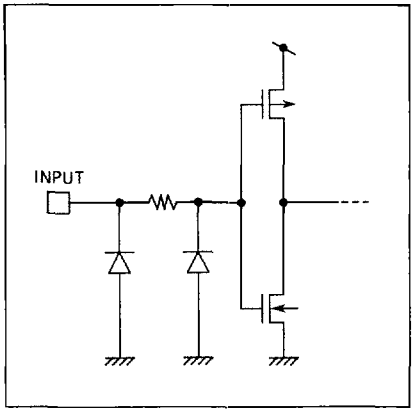
Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	1.2	1.6	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	−1.2	−1.6	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT