National Semiconductor

74F845
8-Bit Transparent Latch

General Description

The 'F845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The 'F845 is functionally- and pin-compatible with AMD's Am29845.

Features

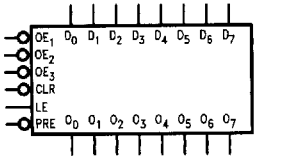
- TRI-STATE® outputs
- Direct replacement for AMD's Am29845

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F845SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F845SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbols



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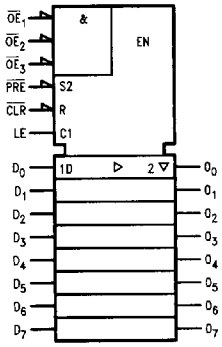
IEEE/IEC



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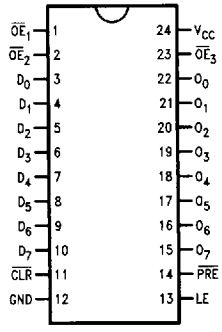
Connection Diagram

Pin Assignment for DIP, SOIC



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Unit Loading/Fan Out: See Section 2 for U.L. Definitions

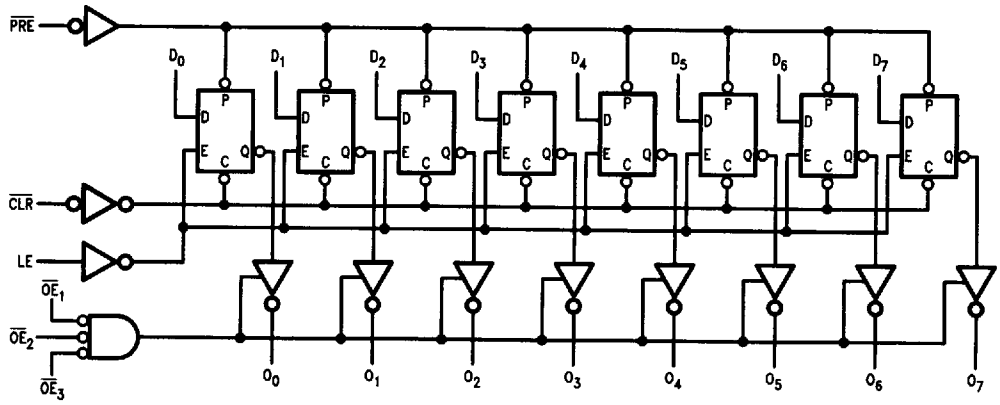
Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/−0.6 mA
O_0–O_7	Data Outputs	150/40	−3.0 μA/24 mA
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables	1.0/1.0	20 μA/−0.6 mA
LE	Latch Enable	1.0/1.0	20 μA/−0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 μA/−0.6 mA
$\overline{PRE}$	Preset	1.0/1.0	20 μA/−0.6 mA

Functional Description

The 'F845 consists of eight D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F Min	74F Typ	74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCZ}	Power Supply Current			63	85	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50\ pF$			74F T_A, V_{CC} = Com, $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	2.5 1.5	4.8 3.6	8.0 6.5	2.0 1.5	9.0 7.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	5.0 2.0	8.1 4.4	12.0 7.5	4.5 2.0	13.5 8.0	ns	2-3
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.0	5.9	10.0	2.5	11.0	ns	2-3
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.0	6.5	10.0	2.5	11.0	ns	2-3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.5 2.5	5.8 7.6	9.5 12.0	2.0 2.0	10.5 13.0	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	1.0 1.0	3.1 2.8	7.5 6.5	1.0 1.0	8.5 7.5	ns	2-5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0		2.5 2.5		ns	2-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to LE	2.5 3.0		3.0 3.5		ns	2-6
t_w (H)	LE Pulse Width, HIGH	4.0		4.0		ns	2-4
t_w (L)	$\overline{PRE}$ Pulse Width, LOW	5.0		5.0		ns	2-4
t_w (L)	$\overline{CLR}$ Pulse Width, LOW	5.0		5.0		ns	2-4
t_{rec}	$\overline{PRE}$ Recovery Time	10.0		10.0		ns	2-6
t_{rec}	$\overline{CLR}$ Recovery Time	12.0		13.0		ns	2-6