



# HIGH SPEED CMOS SRAM

## 256K-BIT(32K X 8)

PRELIMINARY  
**N341256L**  
 B12, B15

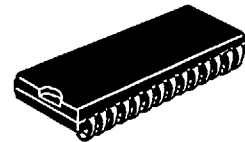
### ■ Features

- CMOS SRAM organized as 32,768 x 8bits
- Single +3.3V (± 0.3V) Power Supply
- High Speed Access time : 12/15ns
- Low power operation
  - Active : 75mA (Max.)
  - Standby : 0.5mA (Max.)

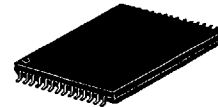
### ● Packages

- 28pin Plastic SOJ(300mil)
- 28pin Plastic TSOP(Type I)

This document contains preliminary information, and is subject to change without notice.



28pin Plastic SOJ(300mil)



28pin Plastic TSOP(Type I)

### ■ Description

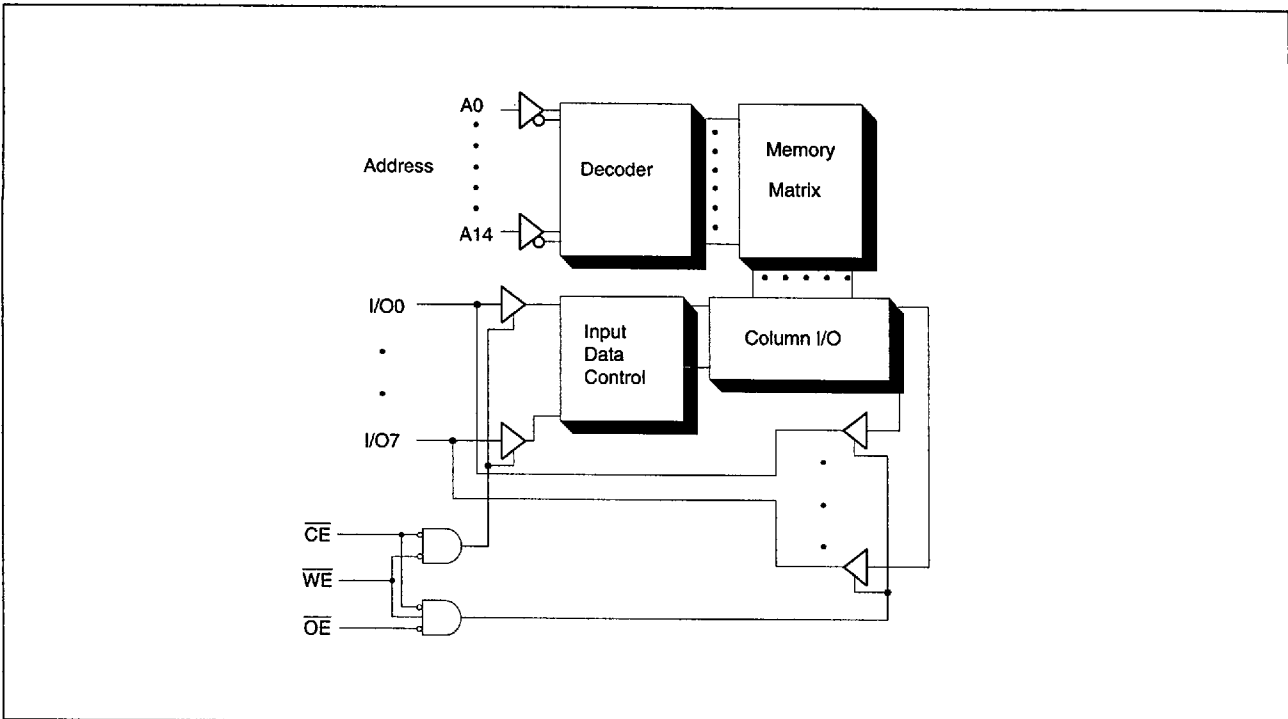
The N341256L is a high performance CMOS static RAM organized as 32,768 x 8bits.

Writing is accomplished when the  $\overline{WE}$  and  $\overline{CE}$  inputs are both Low.

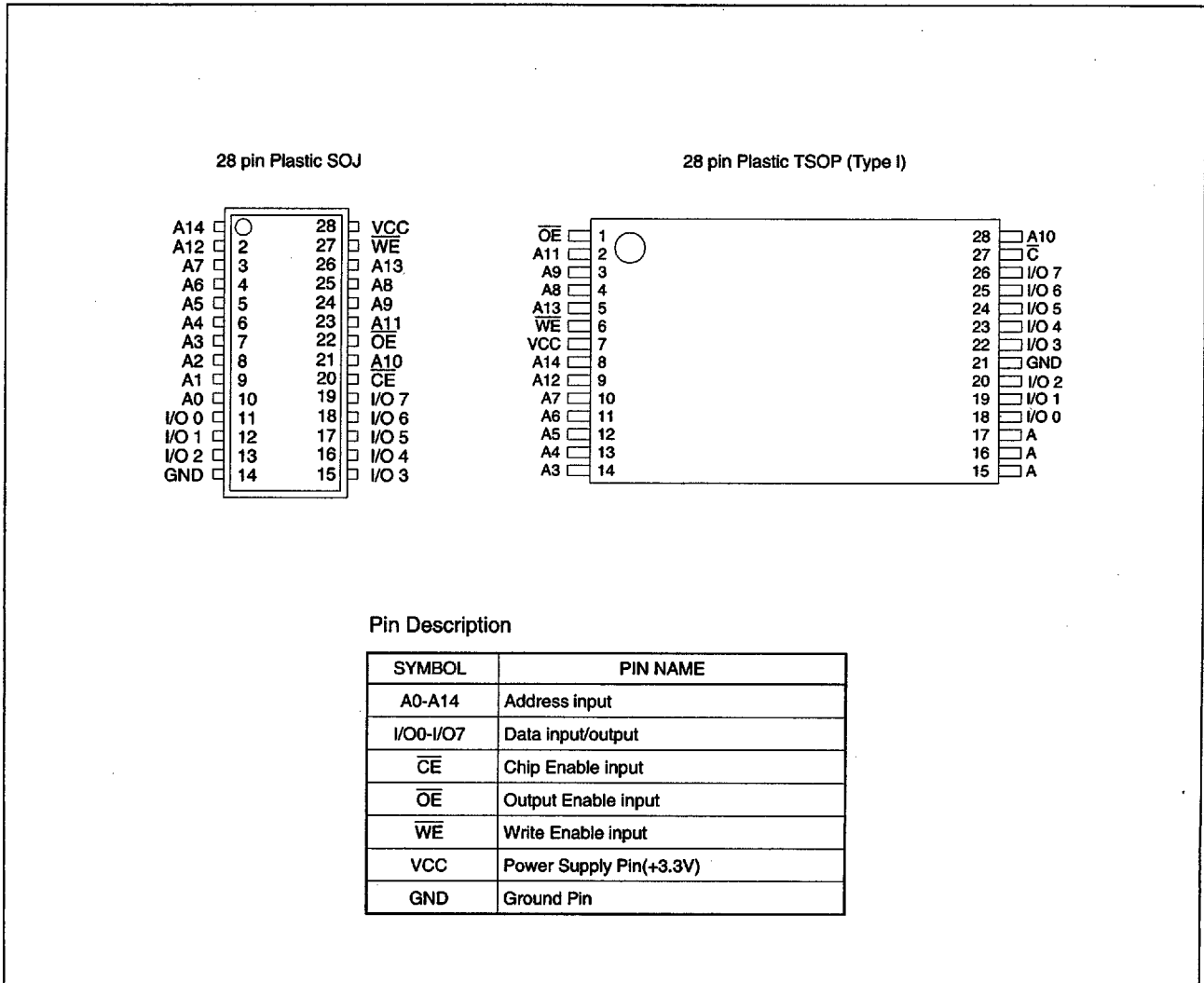
Reading is accomplished when the  $\overline{WE}$  input is High and the  $\overline{CE}$  and  $\overline{OE}$  inputs are both Low.

The N341256L operates from a single +3.3V power supply. All inputs are 2.5V and TTL compatible ( $V_{IH}=1.7V$ ), and all outputs are TTL compatible.

### ■ Functional Block Diagram



■ Pin Configuration



■ Mode Selection Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	High	High-Z	Standby
Low	High	Low	Data out	Read Cycle
X	Low	Low	Data in	Write Cycle
High	High	Low	High-Z	Output disable

Note : X = don't care.



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■ **Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	-0.5 to 4.6	V
VTERM	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5 (Max. 4.6)	V
TOPR	Operating Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
PD	Power Dissipation	1.0	W

**NOTICE**

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ **Recommended Operating Conditions**

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	VCC
0 to 70°C	0V	3.3V ± 0.3V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	1.7	-	VCC+0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

Note : VIL(min) = -2.0V for pulse width less than 10ns.

■ **Capacitance**

(TOPR=25°C, f=1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN=0V	6	pF
COU	Output Capacitance	VOUT=0V	8	pF

Note : These parameters are sampled and not 100% tested.

■ DC Electrical Characteristics

Power Supply Currents<sup>(1)</sup> (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Symbol	Parameter	N341256L B12	N341256L B15	Unit
I <sub>CC</sub>	Dynamic Operating Current $\overline{CE} \leq V_{IL}, V_{CC} = \text{max}, f = f_{\text{max}}, I_{\text{OUT}} = 0\text{mA}, V_{\text{IN}} \geq V_{\text{IH}} \text{ or } \leq V_{\text{IL}}$	75	70	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL level) $\overline{CE} \geq V_{\text{IH}}, V_{CC} = \text{max}, f = f_{\text{max}}^{(2)}, V_{\text{IN}} \geq V_{\text{IH}} \text{ or } \leq V_{\text{IL}}$	20	20	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS level) $\overline{CE} \geq V_{\text{CC}} - 0.2\text{V}, V_{CC} = \text{max}, f = 0, V_{\text{IN}} \leq 0.2\text{V} \text{ or } \geq V_{\text{CC}} - 0.2\text{V}$	0.5	0.5	mA

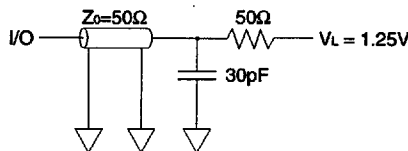
Note : (1) All values are the maximum guaranteed values.  
 (2) Only address inputs cycling at f<sub>max</sub>.

DC Characteristics (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Symbol	Parameter	Condition	N341256L		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = max, V <sub>IN</sub> = GND to V <sub>CC</sub>	-2	2	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = max, $\overline{CE} \geq V_{\text{IH}}, V_{\text{OUT}} = \text{GND to } V_{\text{CC}}$	-2	2	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4mA, V <sub>CC</sub> = min	-	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = min	2.4	-	V

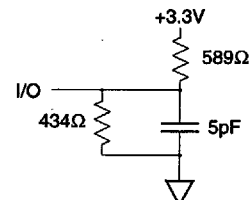
■ AC Test Conditions

Input pulse levels	GND to 2.5V
Input rise and fall times	2.5ns
Input timing reference levels	1.25V
Output timing reference levels	1.25V
Output load	See Figure 1 and 2



(Including scope and jig)

Figure 1. Output Load Equivalent



(Including scope and jig)

Figure 2. Output Load Equivalent  
 (for t<sub>LZCE</sub>, t<sub>HZCE</sub>, t<sub>LZWE</sub>, t<sub>HZWE</sub>, t<sub>LZOE</sub>, t<sub>HZOE</sub>)



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■ AC Electrical Characteristics

Read Cycle (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Description	Symbol	N341256LB12		N341256LB15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle time	t <sub>RC</sub>	12		15		ns
Address access time	t <sub>AA</sub>		12		15	ns
Chip enable access time	t <sub>ACE</sub>		12		15	ns
Output hold from address change	t <sub>OH</sub>	3		3		ns
Chip enable to output in Low-Z	t <sub>LZCE</sub>	3		3		ns
Chip disable to output in High-Z	t <sub>HZCE</sub>		5		5	ns
Chip enable to power up time	t <sub>PU</sub>	0		0		ns
Chip disable to power down time	t <sub>PD</sub>		12		15	ns
Output enable access time	t <sub>AOE</sub>		5		6	ns
Output enable to output in Low-Z	t <sub>LZOE</sub>	0		0		ns
Output disable to output in High-Z	t <sub>HZOE</sub>		5		5	ns

Note : t<sub>LZCE</sub>, t<sub>HZCE</sub>, t<sub>PU</sub>, t<sub>PD</sub>, t<sub>LZOE</sub>, and t<sub>HZOE</sub> are sampled and not 100% tested.

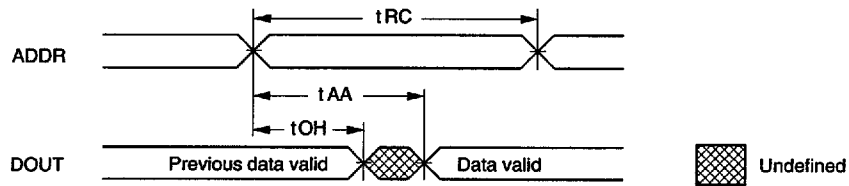
Write Cycle (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Description	Symbol	N341256LB12		N341256LB15		Unit
		Min.	Max.	Min.	Max.	
Write Cycle time	t <sub>WC</sub>	12		15		ns
Chip enable to end of write	t <sub>CW</sub>	8		10		ns
Address valid to end of write	t <sub>AW</sub>	8		10		ns
Address set-up time	t <sub>AS</sub>	0		0		ns
Address hold from end of write	t <sub>AH</sub>	0		0		ns
Write pulse width	t <sub>WP</sub>	8		10		ns
Data set-up time	t <sub>DS</sub>	6		8		ns
Data hold time	t <sub>DH</sub>	0		0		ns
Write disable to output in Low-Z	t <sub>LZWE</sub>	3		3		ns
Write enable to output in High-Z	t <sub>HZWE</sub>		3		3	ns

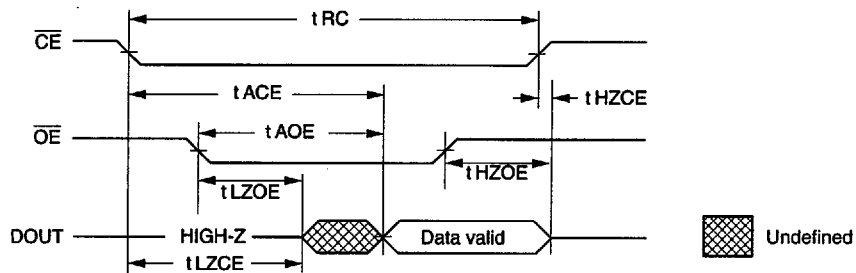
Note : t<sub>LZWE</sub> and t<sub>HZWE</sub> are sampled and not 100% tested.

■ AC Timing Waveform

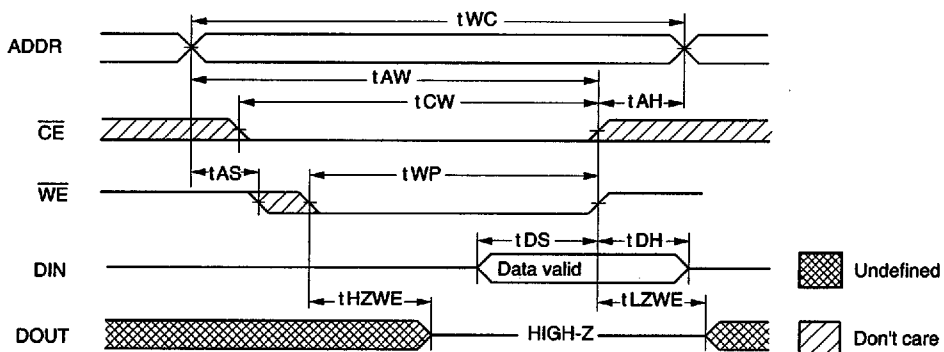
Read Cycle No.1



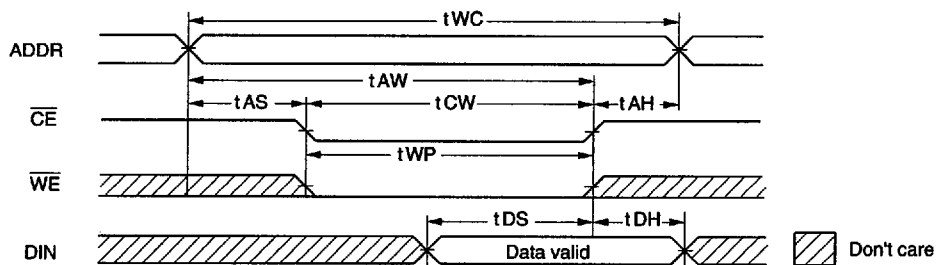
Read Cycle No.2



Write Cycle No.1(Write Enable Controlled)



Write Cycle No.2(Chip Enable Controlled)



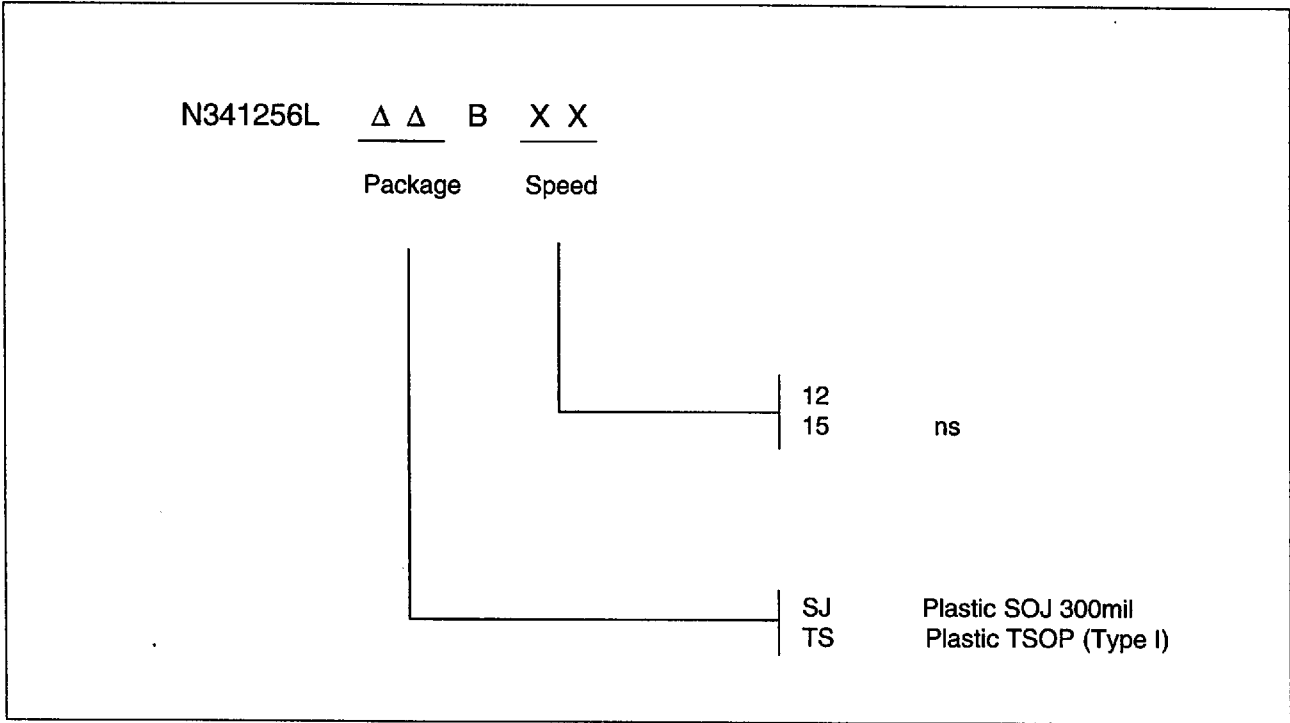


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■ Ordering Information



PART NO.	Access Time (ns)	Operating Current (mA)	Package
N341256LSJB12	12	75	28Pin Plastic SOJ
N341256LTSB12	12	75	28Pin Plastic TSOP
N341256LSJB15	15	70	28Pin Plastic SOJ
N341256LTSB15	15	70	28Pin Plastic TSOP