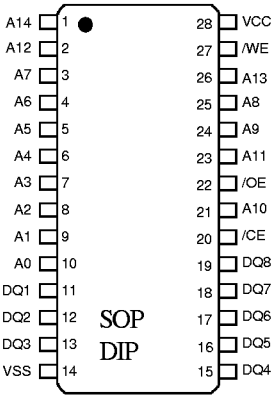
EK61256

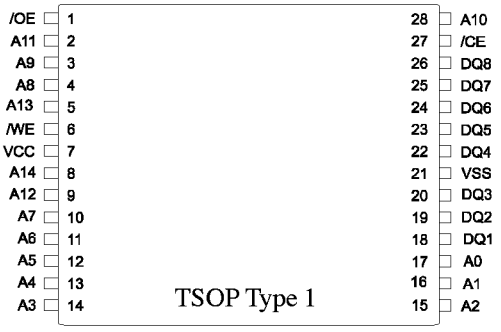
32K x 8 Bit CMOS SRAM
Low Power and Low Low Power

Features

- Low Low Power
  2 uA CMOS Standby 0 to 40^{0}C
- Low Operating Current 60 mA at Min Cycle
- Address Access Times
  35ns, 55ns, 70ns, 100ns
- Single 5V ±10% Power Supply
- Industry Standard Pin Assignment
- Package Options
  330 mil 28 pin SOP
  TSOP Type 1
  300 mil 28 pin PDIP (Skinny)
  600 mil 28 pin PDIP

Pin Configuration





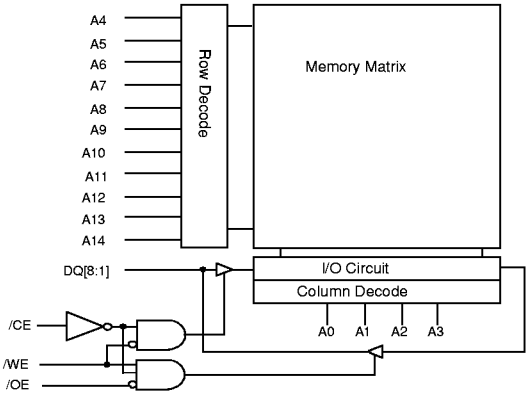
Description

The EK61256 from Eureka is a 256-kilobit density static random access memory organized as 32,768 words by 8 bits. The device is fabricated using high performance CMOS technology enabling low CMOS standby power. This device is ideal for battery backup application.

Pin Assignment

Symbol	Description
A0-A12	Address Inputs
DQ1-DQ8	Data Inputs/Outputs
/CE1, CE2	Chip Enables
/WE	Write Enable
/OE	Ouptut Enable
NC	No Connect
V_{CC}	Power Supply
V_{SS}	Ground

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to Vcc + 0.5	V
Output Voltage	V_{OUT}	-0.5 to Vcc +0.5	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

/CE	/OE	/WE	Mode	DQ Pin	Supply Current
H	X	X	Not Selected	High - Z	I_{SB}, I_{SB1}
X	X	X	Not Selected	High - Z	I_{SB}, I_{SB1}
L	H	H	Output Disabled	High - Z	I_{CCA}
L	L	H	Read	Data Out	I_{CCA}
L	X	L	Write	Data In	I_{CCA}

Electrical Characteristics and DC Operating Conditions

(T_A =0 to + 70^{0}C; V_{CC} = +5V ±10% unless otherwise noted; Note 1)

Description	Symbol	Conditions		Min	Typ	Max	Units
Power Supply Voltage	V_{CC}			4.5	-	5.5	V
Input Low Voltage	V_{IL}			-0.5	-	0.8	V
Input High Voltage	V_{IH}			2.2	-	Vcc+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		-1	-	1	µA
Output Leakage Current	I_{LO}	V_{IN}=V_{SS} to V_{CC}; /CE=V_{IH} or /OE=V_{IH} or /WE=V_{IL}		-1	-	1	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Power Supply Operating Current	I_{CCA}	/CE = V_{IH}; f=max, DQ=0mA		-	35	60	mA
Power Supply Standby Current	I_{SB}	/CE = V_{IL}, DQ=0mA			0.5	1	mA
Low Power CMOS Standby Current (EK61256x-yL)	I_{SB1} - L	V_{CC}=5.5V /CE≥5.3V f=0MHz DQ = 0mA	0 to +70 °C	-	-	100	µA
Low Low Power CMOS Standby Current (EK61256x-yLL)	I_{SB1} - LL		0 to +70 °C	-	4	10	µA
			0 to +40 °C	-	1.0	4	µA
			+25 °C	-	0.5	2	µA

Capacitance

Parameter	Symbol	Max	Units
Input Capacitance	C_{IN}	6	pF
Input/Output Capacitance	$C_{I/O}$	8	pF

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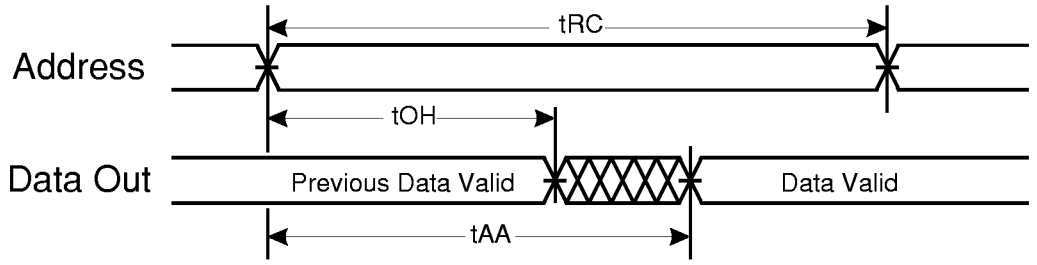
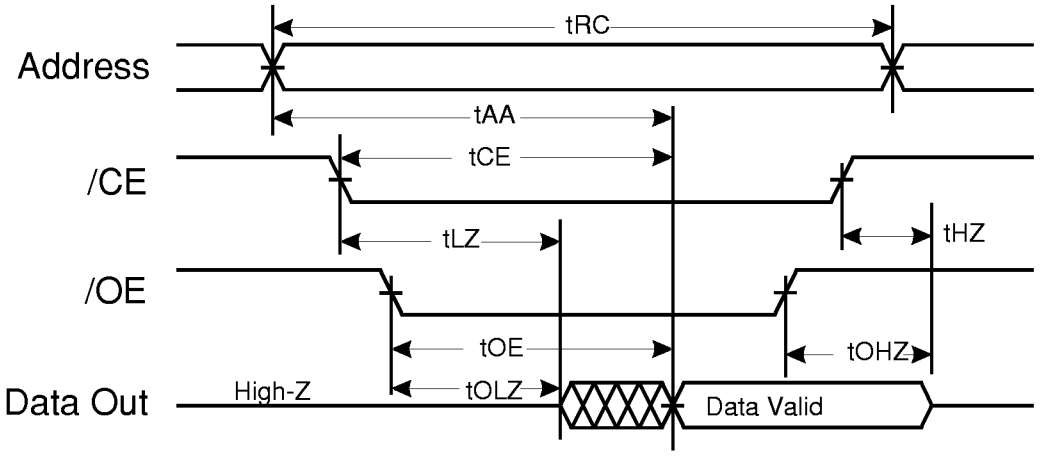
Read Cycle (Address Access)



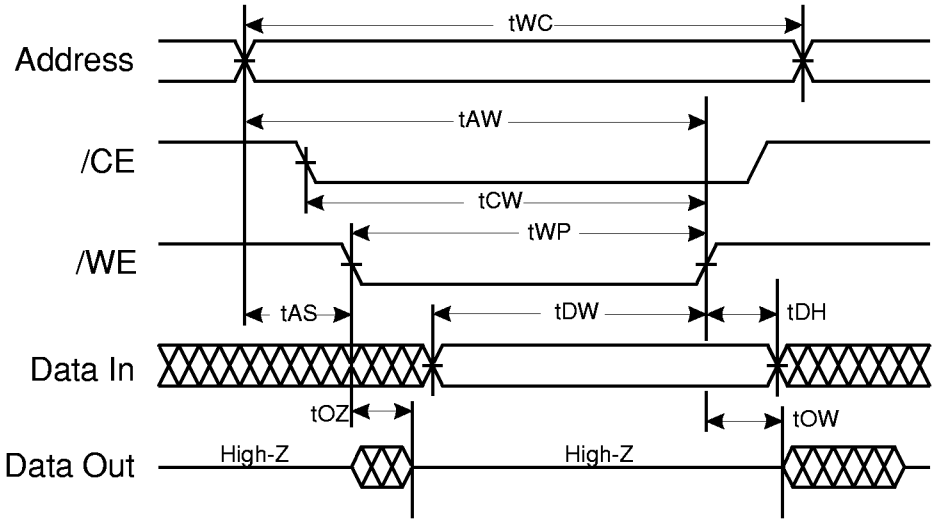
Read Cycle (Chip Enable Access)



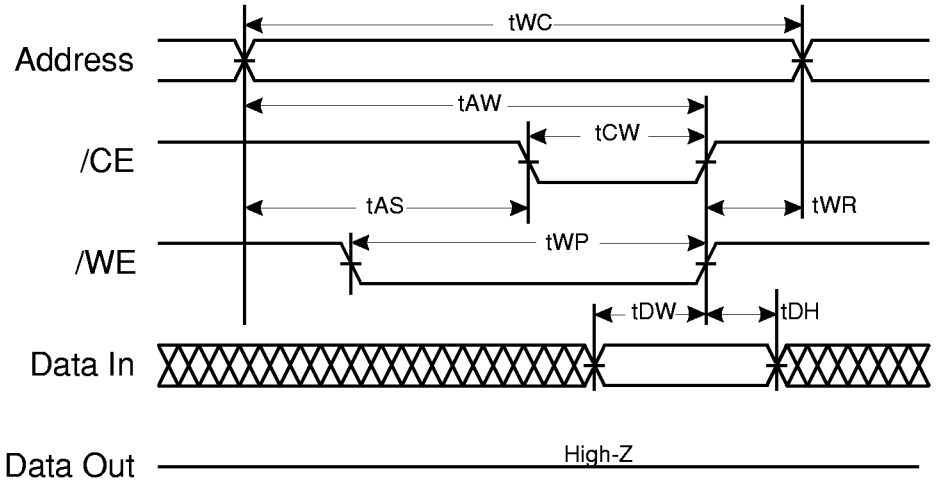
Read Cycle

DESCRIPTION		-35		-55		-70		-100			
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Read Cycle Time	tRC	35	-	55	-	70	-	100	-	ns	2,5
Address Access Time	tAA	-	35	-	55	-	70	-	100	ns	2
Chip Enable Access Time	tCE	-	35	-	55	-	70	-	100	ns	
Output Enable Access Time	tOE	-	15	-	25	-	35	-	50	ns	
Output Hold from Address Change	tOH	5	-	5	-	5	-	5	-	ns	
Chip Enable Active to Low-Z	tLZ	5	-	5	-	5	-	5	-	ns	2
Output Enable to Low-Z	tOLZ	5	-	5	-	5	-	5	-	ns	2
Chip Disable Active to High-Z	tHZ	0	10	0	20	0	25	0	35	ns	2,4
Output Disable to High-Z	tOHZ	0	10	0	20	0	25	0	35	ns	2,4

Write Cycle (/WE Controlled)



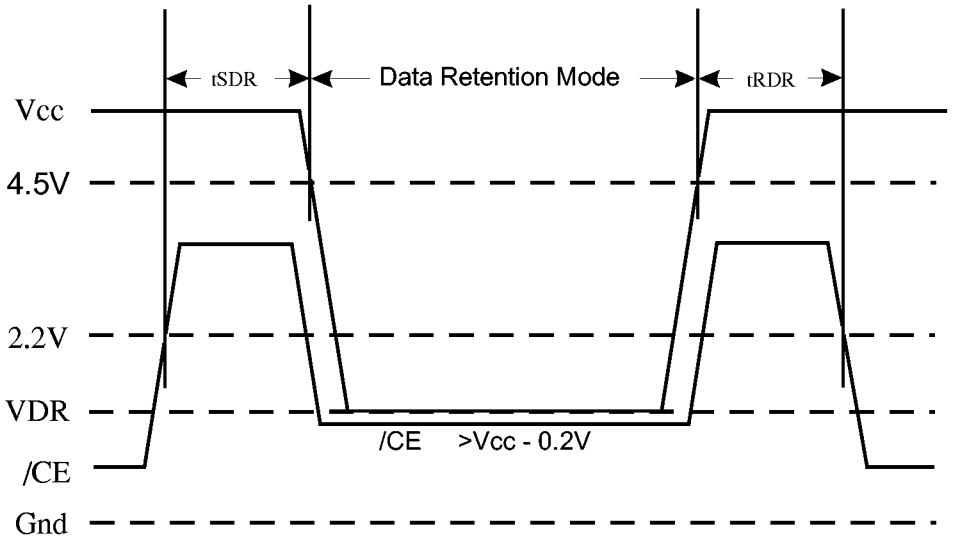
Write Cycle (/CE Controlled)



Write Cycle

DESCRIPTION		-35		-55		-70		-100			
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Write Cycle Time	tWC	35	-	55	-	70	-	100	-	ns	2,3,5
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns	2,3
Address Valid to End of Write	tAW	20	-	45	-	60	-	80	-	ns	2,3
Write Pulse Width	tWP	20	-	40	-	50	-	60	-	ns	2,3
Chip Enable to End of Write	tCW	30	-	40	-	50	-	60	-	ns	2,3
Data Valid to End of Write	tDW	15	-	25	-	30	-	40	-	ns	2,3
Data Hold from End of Write	tDH	0	-	0	-	0	-	0	-	ns	2,3
Write Low to Output High-Z	tOZ	0	10	0	10	0	10	0	10	ns	2,3,4
Write High to Output Low-Z	tOW	5	-	5	-	5	-	5	-	ns	2,3
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns	2,3

Data Retention (/CE Controlled)



Data Retention

Description	Symbol	Conditions		Min	Typ	Max	Units
Data Retention Supply Voltage	VDR	/CE1≥Vcc-0.2V or CE2≤Vss+0.2V		2.0	-	5.5	V
Data Retention Current (EK6264x-yL)	ICCDR1	VCC=3.0V	0 to +70 °C	-	-	90	µA
	ICCDR2	VCC=2.0V	0 to +70 °C	-	-	80	µA
Data Retention Current (EK6264x-yLL)	ICCDR1	VCC=3.0V	0 to +70 °C		1.5	4	µA
	ICCDR2	VCC=2.0V	0 to +70 °C	-	0.6	2	µA
			0 to +40 °C	-	0.4	0.7	µA
			+25 °C	-	0.3	0.5	µA
Data Retention Setup Time	tSDR			0	-	-	ns
Data Retention Recovery Time	tRDR			tRC	-	-	ns

AC Test Conditions

(TA = 0 to +70^{0}C, VCC = 5V ±10%)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	VIH	2.4	V
Input Pulse Low Level	VIL	0.8	V
Input Rise Time	TR	5.0	ns
Input Fall Time	TF	5.0	ns
Input and Output Timing Reference Level		1.5	V

AC Test Loads

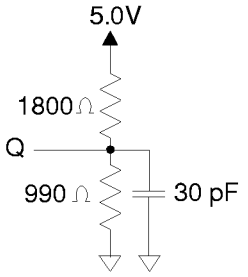


Figure 1A - AC Test Load

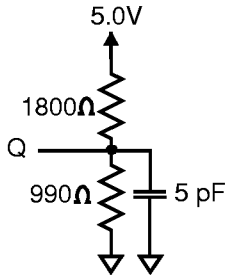


Figure 1B - Hi Z Test Load

Notes:

1. When /WE goes low, outputs are in a Hi-Z state and /OE is overridden.
2. /WE is high for a read cycle.
3. A write occurs during the overlap of /CE and /WE.
4. Measured at ±500mv from steady state with the Hi-Z load.
5. Referenced from the last valid address to the first transitioning address pin.

Ordering Information

(Order by Complete Part Number)

EK 61256 X - Y Z

- Eureka Prefix: EK
- Part Number: 61256
- Package Type: X
  - S = 330mil SOP
  - T = TSOP Type I
  - K = 300 mil PDIP(Skinny)
  - P = 600 mil PDIP
- 35=35ns, 55=55ns, 70=70ns, 100=100ns
- Y
- Z
  - L = Low Power Option
  - LL = Low Low Power Option

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