

KM23C32000G**CMOS MASK ROM****32M-Bit (4M × 8/2M × 16) CMOS MASK ROM****FEATURES**

- **Switchable organization**
4,194,304 × 8 (byte mode)
2,097,152 × 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
Operating: 60mA (max.)
Standby: 50 μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin, 800 mil, plastic SOP**

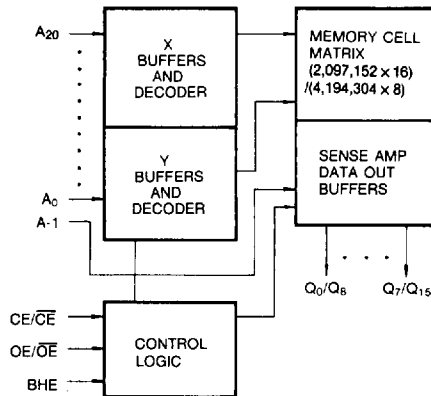
GENERAL DESCRIPTION

The KM23C32000G is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and its organization is either as 4,194,304 × 8 bit (byte mode) or as 2,097,152 × 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

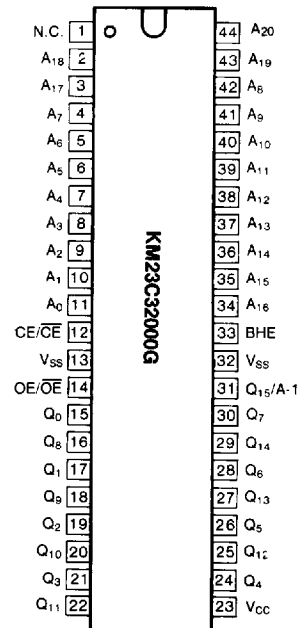
It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C32000G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM

Pin Name	Pin Function
A ₀ -A ₂₀	Address Inputs
Q ₀ -Q ₁₄	Data Outputs
Q ₁₅ /A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/ $\overline{\text{CE}}$ *	Chip Enable
OE/ $\overline{\text{OE}}$ *	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION

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ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN}	-0.3 to +7.0	V
Temperature Under Bias	T _{bias}	-10 to + 85	°C
Storage Temperature	T _{stg}	-55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I _{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I _{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I _{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I _I	V _{IN} = 0 to V _{CC}	—	10	μA
Output Leakage Current	I _{LO}	V _{OUT} = 0 to V _{CC}	—	10	μA
Input High Voltage, All Inputs	V _{IH}		2.2	V _{CC} + 0.3	V
Input Low Voltage, All Inputs	V _{IL}		-0.3	0.8	V
Output High Voltage Level	V _{OH}	I _{OH} = -400μA	2.4	—	V
Output Low Voltage Level	V _{OL}	I _{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C _{OUT}	V _{OUT} = 0V	—	12.0	pF
Input Capacitance	C _{IN}	V _{IN} = 0V	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/ \overline{CE}	OE/ \overline{OE}	BHE	Q ₁₅ /A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
		H	Output	Operating	Q ₀ -Q ₁₅ : Dout	Active
	H/L	L	Input	Operating	Q ₀ -Q ₇ : Dout Q ₈ -Q ₁₄ : High-Z	Active

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AC CHARACTERISTICS

(Ta=0° to +70°C, Vcc=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

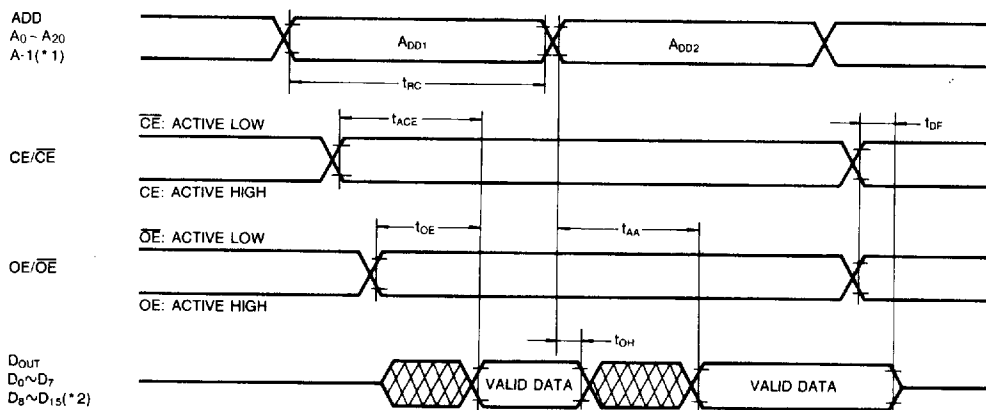
READ CYCLE

Parameter	Symbol	KM23C32000G-15		KM23C32000G-20		KM23C32000G-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	150		200		250		ns
Chip Enable Access Time	t _{ACE}		150		200		250	ns
Address Access Time	t _{AA}		150		200		250	ns
Output Enable Access Time	t _{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t _{DF}		30		40		50	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns

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TIMING DIAGRAM

READ



(* 1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
 (* 2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

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44 LEAD SMALL OUTLINE PACKAGE (KM23C32000G)

Unit: Inches (mm)

