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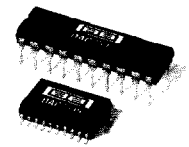


DAC7545

www.burr-brown.com/databook/DAC7545.html

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER Microprocessor Compatible

FEATURES

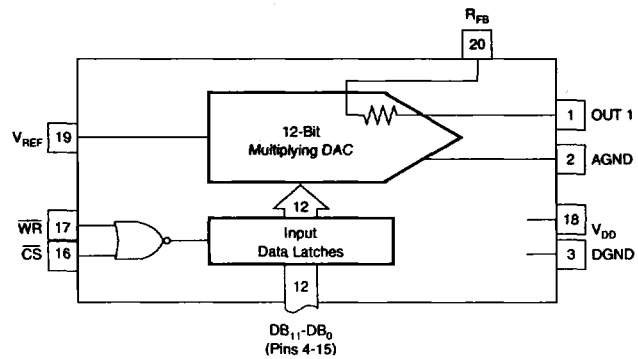
- **FOUR-QUADRANT MULTIPLICATION**
- **LOW GAIN TC: 2ppm/°C typ**
- **MONOTONICITY GUARANTEED OVER TEMPERATURE**
- **SINGLE 5V TO 15V SUPPLY**
- **TTL/CMOS LOGIC COMPATIBLE**
- **LOW OUTPUT LEAKAGE: 10nA max**
- **LOW OUTPUT CAPACITANCE: 70pF max**
- **DIRECT REPLACEMENT FOR AD7545, PM-7545**

DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin plastic DIP or 20-lead plastic SOIC packages. Devices are specified over the commercial.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and V_{DD} = +5V.



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SPECIFICATIONS

ELECTRICAL

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM, unless otherwise specified.

PARAMETER	GRADE	DAC7545 V_{DD} = +5V T_A = +25°C	DAC7545 V_{DD} = +5V T_{MAX}-T_{MIN}[1]	DAC7545 V_{DD} = +15V T_A = +25°C	DAC7545 V_{DD} = +15V T_{MAX}-T_{MIN}[1]	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Accuracy	J	±2	±2	±2	±2	LSB	
	K	±1	±1	±1	±1	LSB	
	L	±1/2	±1/2	±1/2	±1/2	LSB	
	GL	±1/2	±1/2	±1/2	±1/2	LSB	
Differential Nonlinearity	J	±4	±4	±4	±4	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	K	±1	±1	±1	±1	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	L	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
	GL	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
Gain Error (with internal R_{FB})[2]	J	±20	±20	±25	±25	LSB	D/A register loaded with FFF_H. Gain error is adjustable using the circuits in Figures 2 and 3.
	K	±10	±10	±15	±15	LSB	
	L	±5	±6	±10	±10	LSB	
	GL	±2	±3	±6	±7	LSB	
Gain Temperature Coefficient[3] (ΔGain/ΔTemperature)	All	±5	±5	±10	±10	ppm/°C for V_{DD} = +5	Typical value is 2ppm/°C
DC Supply Rejection[3] (ΔGain/ΔV_{DD})	All	0.015	0.03	0.01	0.02	%/%	ΔV_{DD} ±5%
Output Leakage Current at Out 1	J, K, L, GL	10	50	10	50	nA	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	µs	To 1/2LSB. Out_1 Load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V
Propagation Delay[3] (from digital input change to 90% of final analog output)	All	300		250		ns	Out_1 Load = 100Ω. C_{EXT} = 13pF[4]
Glitch Energy	All	400		250		nV-s[5]	V_{REF} = ACOM
AC Feedback at I_{OUT} 1	All	5	5	5	5	mVp-p[5]	V_{REF} = ±10V, 10kHz Sine Wave
REFERENCE INPUT							
Input Resistance (pin 19 to AGND)	All	7 25	7 25	7 25	7 25	kΩ[6] kΩ	Input resistance TC = 300ppm/°C[5]
AC OUTPUTS							
Output Capacitance[3]: $C_{OUT\,1}$	All	70	70	70	70	pF	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
$C_{OUT\,2}$	All	200	200	200	200	pF	DB_0-DB_{11} = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	13.5	13.5	V[6]	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	1.5	1.5	V	
I_{IN} (Input Current)[7]	All	±1	±10	±1	±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[3]: DB_0-DB_{11}	All	5	5	5	5	pF	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF	V_{IN} = 0V
SWITCHING CHARACTERISTICS[8]							
Chip Select to Write Setup Time, t_{CS}	All	280	380	180	200	ns[6]	See Timing Diagram
		200	270	120	150	ns[5]	
Chip Select to Write Hold Time, t_{CH}	All	0	0	0	0	ns[6]	
Write Pulse Width, t_{WR}	All	250	400	160	240	ns[6]	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns[5]	
Data Setup Time, t_{DS}	All	140	210	90	120	ns[6]	
		100	150	60	80	ns[5]	
Data Hold Time, t_{DH}	All	10	10	10	10	ns[6]	
POWER SUPPLY, I_{DD}							
	All	2	2	2	2	mA	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	µA	All Digital Inputs 0V or V_{DD}
	All	10	10	10	10	µA[5]	All Digital Inputs 0V or V_{DD}

NOTES: (1) Temperature ranges—J, K, L, GL: –40°C to +85°C. (2) This includes the effect of 5ppm max, gain TC. (3) Guaranteed but not tested. (4) DB_0-DB_{11} = 0V to V_{DD} or V_{DD} to 0V. (5) Typical. (6) Minimum. (7) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA. (8) Sample tested at +25°C to ensure compliance.

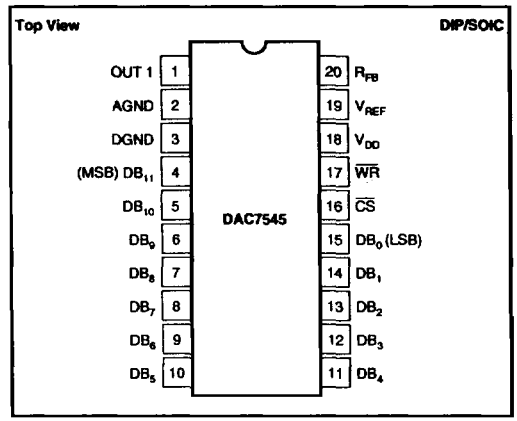
ABSOLUTE MAXIMUM RATINGS[1]

T_A = +25°C, unless otherwise noted.

V_{DD} to DGND	−0.3V, +17
Digital Input to DGND	−0.3V, V_{DD}
V_{RFB}, V_{REF}, to DGND	±25V
$V_{PIN\ 1}$ to DGND	−0.3V, V_{DD}
AGND to DGND	−0.3V, V_{DD}
Power Dissipation: Any Package to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature:	
Commercial J, K, L, GL	*−40°C to +85°C*
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB) V_{DD} = +5V	PACKAGE DRAWING NUMBER[1]
DAC7545JP	20-Pin Plastic PDIP	−40°C to +85°C	±2	±20	222
DAC7545KP	20-Pin Plastic PDIP	−40°C to +85°C	±1	±10	222
DAC7545LP	20-Pin Plastic PDIP	−40°C to +85°C	±1/2	±5	222
DAC7545GLP	20-Pin Plastic PDIP	−40°C to +85°C	±1/2	±2	222
DAC7545JU	20-Pin Plastic SOIC	−40°C to +85°C	±2	±20	221
DAC7545KU	20-Pin Plastic SOIC	−40°C to +85°C	±1	±10	221
DAC7545LU	20-Pin Plastic SOIC	−40°C to +85°C	±1/2	±5	221
DAC7545GLU	20-Pin Plastic SOIC	−40°C to +85°C	±1/2	±2	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.