Signetics

Military Logic Products

54F109
Flip-Flop

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

Product Specification

DESCRIPTION

The 54F109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs, and complementary $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock Input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.

The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

ORDERING INFORMATION

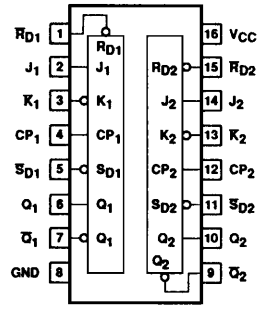
DESCRIPTION	ORDER CODE
Ceramic DIP	54F109/BEA
Ceramic Flat Pack	54F109/BFA
20-Pin Ceramic LLCC	54F109/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1 - J_2, $\overline{K}_1$ - $\overline{K}_2$	Data inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active Low)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active Low)	1.0/3.0	20μA/1.8mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

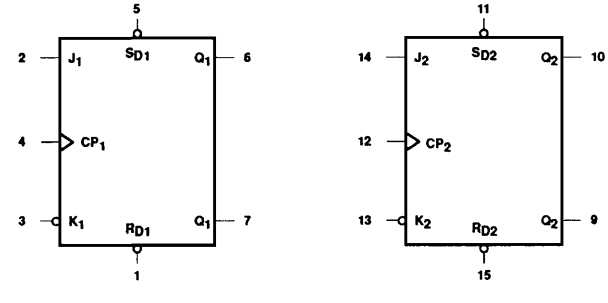
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



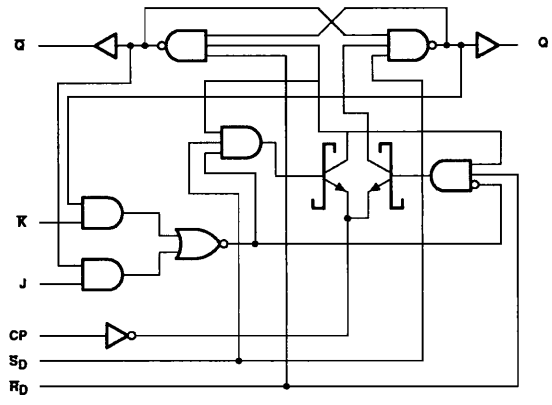
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2.

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↑	l	l	L	H
Load "1" (Set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the Low-to-High Clock transition
l = Low voltage level one setup time prior to the Low-to-High Clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High Clock transition
↑ = Low-to-High Clock transition

NOTE:
Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20.0	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	J, $\overline{K}$, CP inputs	V_{CC} = Max, V_I = 2.7V		1	20	µA
		$\overline{S}_D$, $\overline{R}_D$ inputs			1	20	µA
I_{IL}	Low-level input current	J, $\overline{K}$, CP inputs	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
		$\overline{S}_D$, $\overline{R}_D$ inputs			-1.3	-1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V	-60	-85	-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		12.3	17	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing & Specifying FAST Logic."

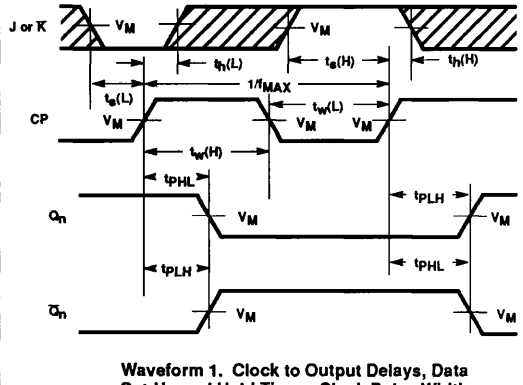
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	9.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	2.8 3.5	9.0 11.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

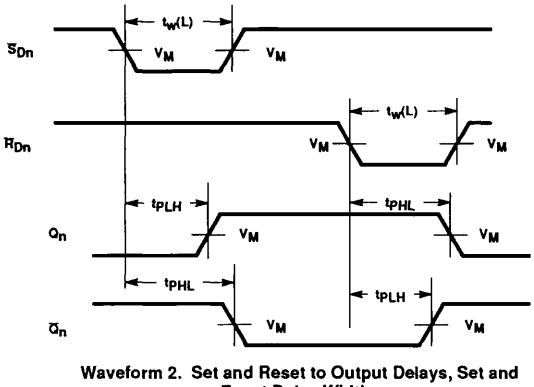
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time High or Low, J or $\overline{K}$ to CP	Waveform 1	3.0 3.0			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low, J or $\overline{K}$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns ns
$t_W(L)$	Set or Reset pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, Set or Reset to clock	Waveform 3	2.0			2.0		ns

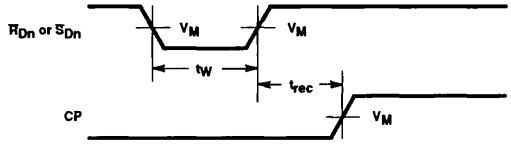
AC WAVEFORMS



Waveform 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width



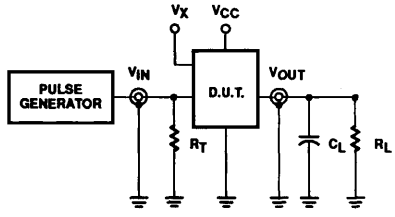
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths



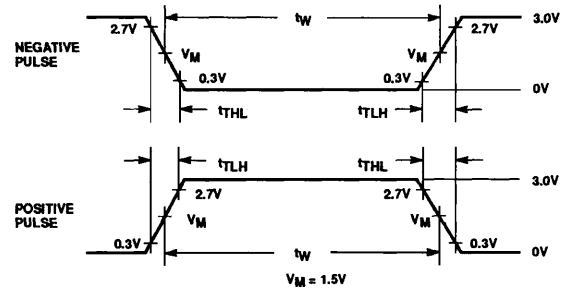
Waveform 3. Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns