

Document Title**256K x8 bit 3.0V Low Power CMOS slow SRAM**Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
10	Revision History Insert Revised - Improved operating current Icc1 : 60mA -> 30mA	Jul.29.2000	Final
11	Change the Notch Location of sTSP - Left-Top => Left-Center	Sep.04.2000	Final
12	Revised - VIH max : Vcc + 0.2V => Vcc + 0.3V - VIL min : - 0.2V => - 0.3V	Dec.16.2000	Final
13	Changed Logo - HYUNDAI -> hynix	Apr.30.2001	Final

DESCRIPTION

The HY62U8200 is a high speed, low power and 2M bit CMOS SRAM organized as 262,144 words by 8bit. The HY62U8200 uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

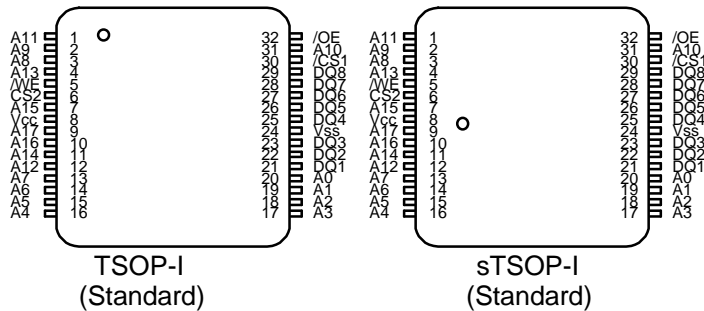
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL-part)
 - . 2.0V(min) data retention
- Standard pin configuration
 - . 32-sTSOPI-8X13.4, 32-TSOPI-8X20 (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)	Temperature (°C)
HY62U8200	2.7~3.3	70*/85/100	5	25	0~70
HY62U8200-E	2.7~3.3	70*/85/100	5	25	-25~85(E)
HY62U8200-I	2.7~3.3	70*/85/100	5	25	-40~85(I)

- Note 1. Blank : Commercial, E : Extended, I : Industrial
 2. Current value is max.
 3. * 70ns is available with 30pF test load

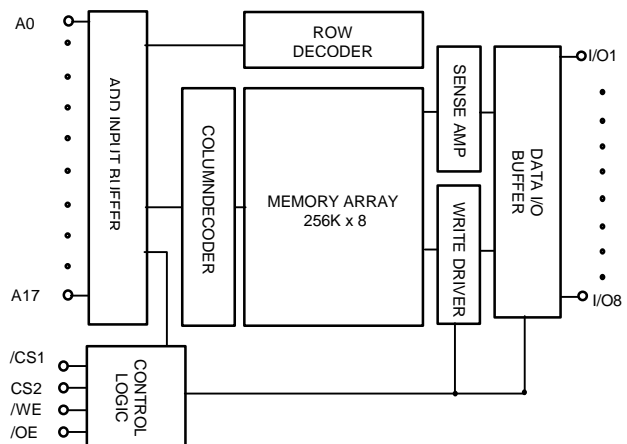
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A17	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(2.7V~3.3V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62U8200LLT1	70*/85/100	LL-part		TSOPI(Standard)
HY62U8200LLR1	70*/85/100	LL-part		TSOPI(Reversed)
HY62U8200LLST	70*/85/100	LL-part		Smaller TSOPI(Standard)
HY62U8200LLSR	70*/85/100	LL-part		Smaller TSOPI(Reversed)
HY62U8200LLT1-E	70*/85/100	LL-part	E	TSOPI(Standard)
HY62U8200LLR1-E	70*/85/100	LL-part	E	TSOPI(Reversed)
HY62U8200LLST-E	70*/85/100	LL-part	E	Smaller TSOPI(Standard)
HY62U8200LLSR-E	70*/85/100	LL-part	E	Smaller TSOPI(Reversed)
HY62U8200LLT1-I	70*/85/100	LL-part	I	TSOPI(Standard)
HY62U8200LLR1-I	70*/85/100	LL-part	I	TSOPI(Reversed)
HY62U8200LLST-I	70*/85/100	LL-part	I	Smaller TSOPI(Standard)
HY62U8200LLSR-I	70*/85/100	LL-part	I	Smaller TSOPI(Reversed)

Note 1. Blank : Commercial, E : Extended, I : Industrial

2. * measured with 30pF test load.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.2 to 3.9	V	
V _{CC}	Voltage on V _{CC} supply relative to V _{SS}	-0.2 to 4.0	V	
T _A	Operating Temperature	0 to 70	°C	HY62U8200
		-25 to 85	°C	HY62U8200-E
		-40 to 85	°C	HY62U8200-I
T _{STG}	Storage Temperature	-55 to 150	°C	
P _D	Power Dissipation	1.0	W	
I _{OUT}	Data Output Current	50	mA	
T _{SOLDER}	Lead Soldering Temperature & Time	260 • 5	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	Mode	I/O	Power
H	X	X	X	Deselected	High-Z	Standby
X	L	X	X	Deselected	High-Z	Standby
L	H	H	H	Output Disabled	High-Z	Active
L	H	H	L	Read	Dout	Active
L	H	L	X	Write	DIN	Active

Note :

- H=V_{IH}, L=V_{IL}, X=don't care(V_{IH} or V_{IL})

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	2.7	3.0	3.3	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note

 1. V_{IL} = -1.5V for pulse width less than 30ns

DC ELECTRICAL CHARACTERISTICS

 V_{CC} = 2.7V~3.3V, T_A = 0°C to 70°C/ -25°C to 85°C (E)/ -40°C to 85°C (I), unless otherwise specified

Sym.	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	-	1	μA	
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS1 = V _{IH} or CS2 = V _{IL} or /OE = V _{IH} or /WE = V _{IL}	-1	-	1	μA	
I _{CC}	Operating Power Supply Current	/CS1 = V _{IL} , CS2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA	-	-	5	mA	
I _{CC1}	Average Operating Current	Min Duty Cycle = 100%, /CS1 = V _{IL} CS2 = V _{IH} , V _{IN} = V _{IH} or V _{IL}	-	-	30	mA	
		Cycle time = 1μs, I _{I/O} = 0Ma, /CS1 ≤ 0.2V, CS2 ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} - 0.2V	-	-	6	mA	
I _{SB}	TTL Standby Current (TTL Input)	/CS1 = V _{IH} or CS2 = V _{IL} -	-	-	0.5	mA	
I _{SB1}	Standby Current (CMOS Input)	HY62U8200B	/CS1 ≥ V _{CC} - 0.2V, CS2 ≥ 0.2V or CS2 ≥ V _{CC} - 0.2V	-	-	25	μA
		HY62U8200B-E		-	-	25	μA
		HY62U8200B-I		-	-	25	μA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -1mA	2.2	-	-	V	

 Note : Typical values are at V_{CC} = 3.0V, T_A = 25°C

CAPACITANCE

(Temp = 25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance	V _{I/O} = 0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

V_{CC}= 2.7V~3.3V, T_A = 0°C to 70°C/ -25°C to 85°C(E)/ -40°C to 85°C(I), unless otherwise specified

#	Symbol	Parameter	-70*		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	t _{RC}	Read Cycle Time	70	-	85	-	100	-	ns
2	t _{AA}	Address Access Time	-	70	-	85	-	100	ns
3	t _{ACS}	Chip Select Access Time	-	70	-	85	-	100	ns
4	t _{OE}	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	t _{CLZ}	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	t _{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t _{CHZ}	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
8	t _{OHZ}	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	t _{OH}	Output Hold from Address Change	15	-	15	-	15	-	ns
WRITE CYCLE									
10	t _{WC}	Write Cycle Time	70	-	85	-	100	-	ns
11	t _{CW}	Chip Selection to End of Write	60	-	70	-	80	-	ns
12	t _{AW}	Address Valid to End of Write	60	-	70	-	80	-	ns
13	t _{AS}	Address Set-up Time	0	-	0	-	0	-	ns
14	t _{WP}	Write Pulse Width	50	-	60	-	70	-	ns
15	t _{WR}	Write Recovery Time	0	-	0	-	0	-	ns
16	t _{WHZ}	Write to Output in High Z	0	20	0	25	0	30	ns
17	t _{DW}	Data to Write Time Overlap	30	-	35	-	40	-	ns
18	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t _{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

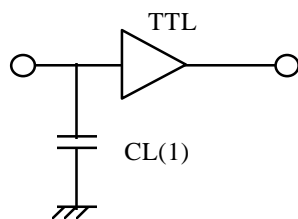
T_A = 0°C to 70°C / -25°C to 85°C (E)/ -40°C to 85°C (I), unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	t _{CLZ} ,t _{OLZ} ,t _{CHZ} ,t _{OHZ} ,t _{WHZ} ,t _{OW}	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load
		CL = 30pF + 1TTL Load

Note

* : Test load is 30pF for 70ns device.

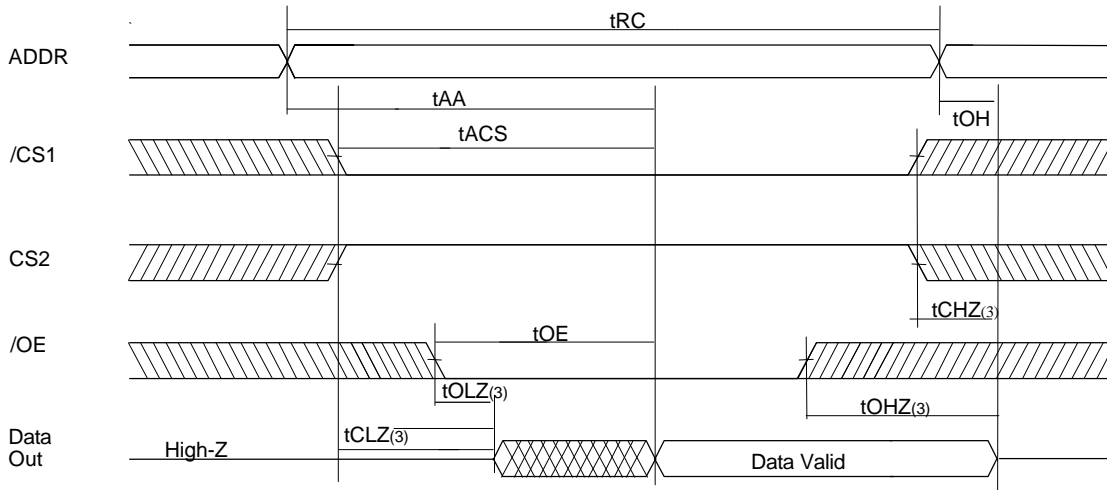
AC TEST LOADS



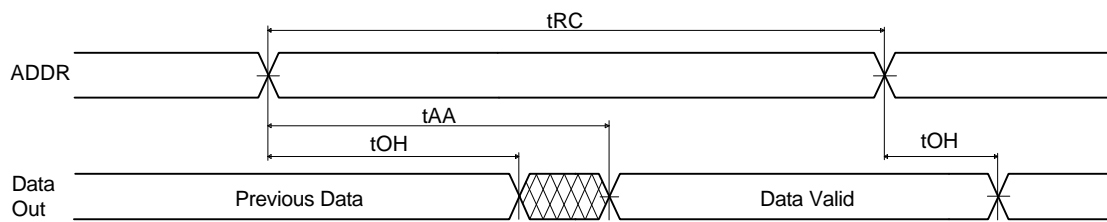
Note : 1 Including jig and scope capacitance

TIMING DIAGRAM

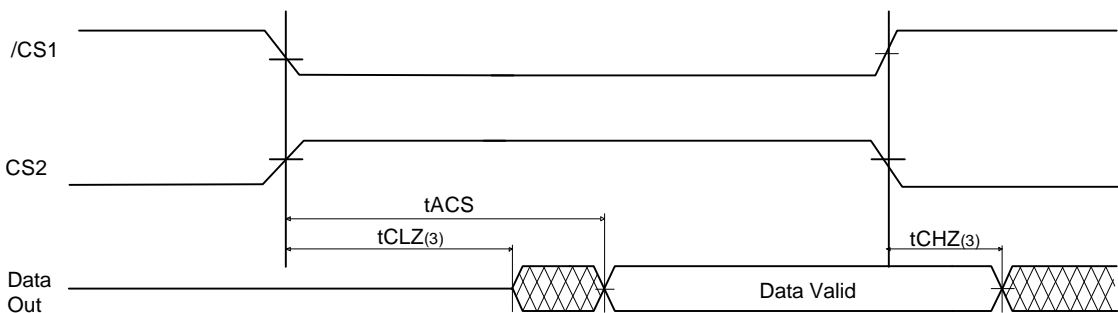
READ CYCLE 1 (Note 1,4)



READ CYCLE 2 (Note 1,2,4)



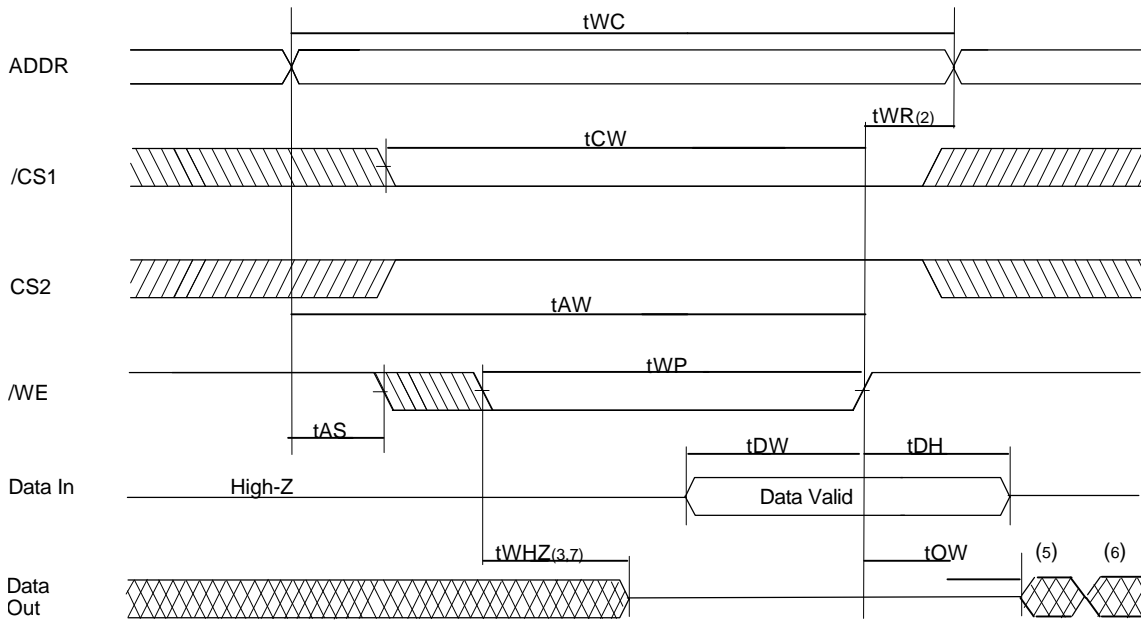
READ CYCLE 3 (Note 1,2,4)



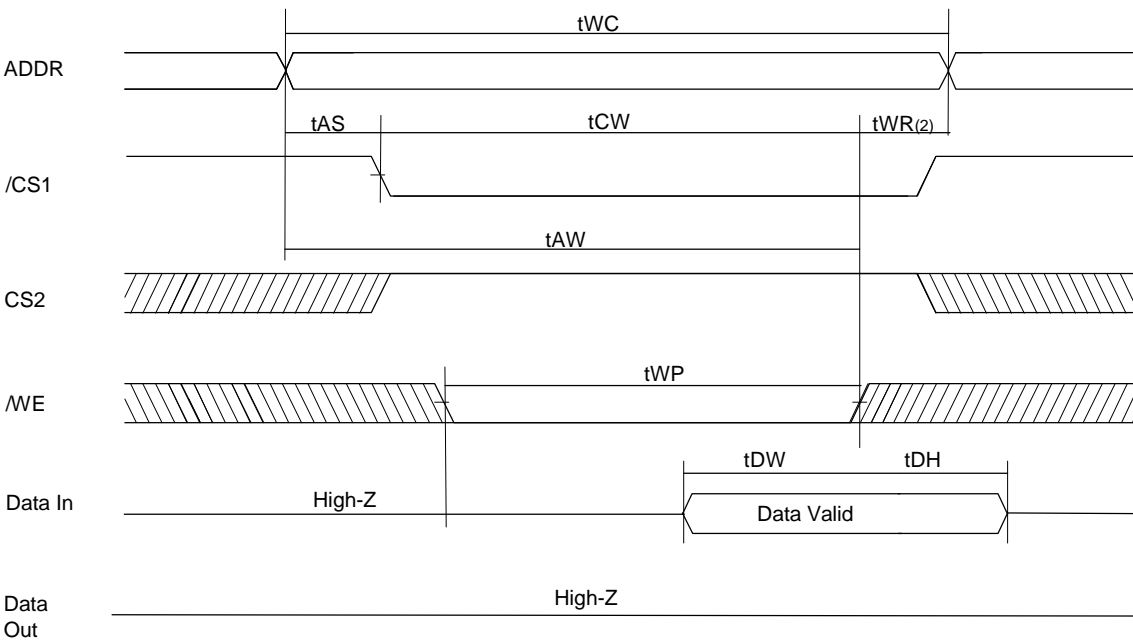
Notes:

1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS1 and a high CS2.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active
CS2 in low for the standby, high for active

WRITE CYCLE 1(1,4,5,8) (/WE Controlled)



WRITE CYCLE 1(1,4,5,8) (/CS1, CS2 Controlled)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS1, a high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 is applied in case a write ends as /CS1, or /WE going high, and tWR2 is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION ELECTRIC CHARACTERISTIC

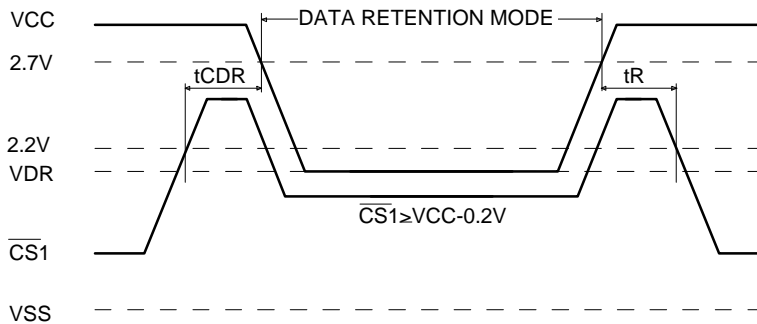
T_A = 0°C to 70°C / -25°C to 85°C (E)/ -40°C to 85°C (I)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
VDR	V _{cc} for Data Retention		/CS1 ≥ V _{cc} -0.2V, CS2 ≤ 0.2V or ≥ V _{cc} - 0.2V, V _{ss} ≤ V _{IN} ≤ V _{cc}	2.0	-	-	V
ICCDR	Data Retention Current	HY62U8200	V _{cc} =3.0V, /CS1 ≥ V _{cc} - 0.2V, CS2 ≤ 0.2V or ≥ V _{cc} - 0.2V, V _{ss} ≤ V _{IN} ≤ V _{cc}	-	-	25	uA
		HY62U8200-E		-	-	25	uA
		HY62U8200-I		-	-	25	uA
Tcdr	Chip Deselect to Data Retention Time		See Data Retention Timing Diagram	0	-	-	ns
Tr	Operating Recovery Time			5	-	-	ms

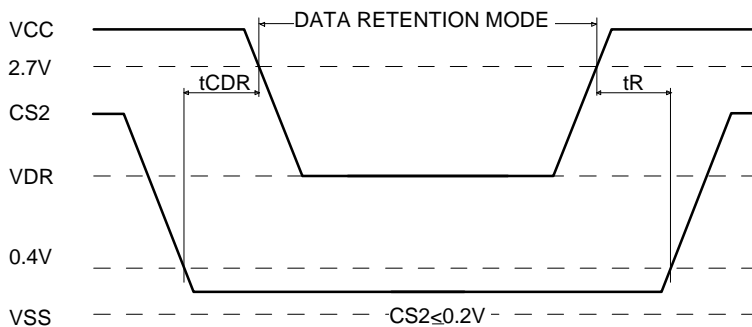
Notes:

1. Typical values are under the condition of T_A = 25°C.

DATA RETENTION TIMING DIAGRAM 1

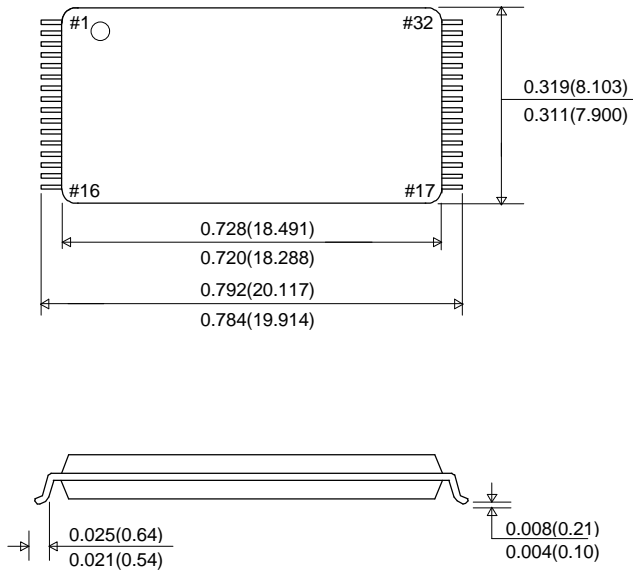


DATA RETENTION TIMING DIAGRAM 2

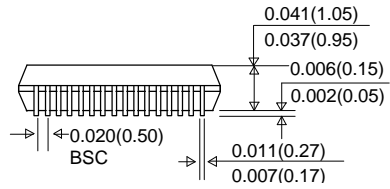


PACKAGE INFORMATION

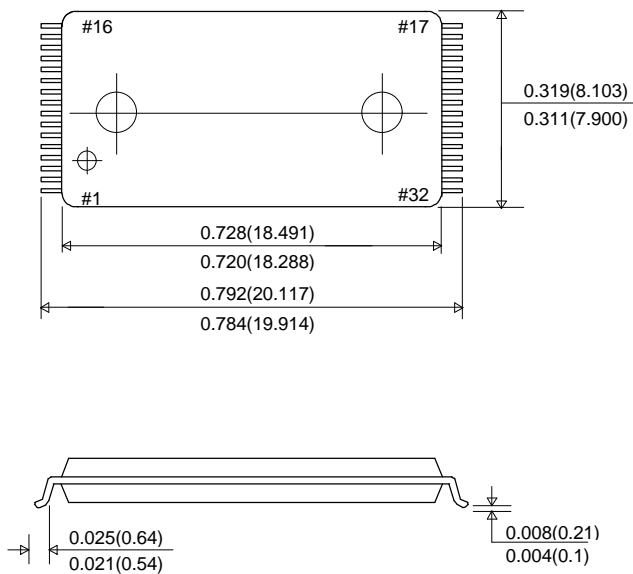
32pin 8x20mm Thin Small Outline Package Standard(T1)



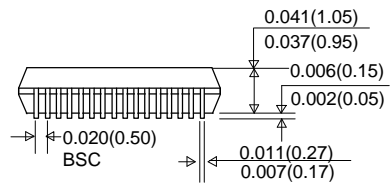
UNIT : INCH(mm)



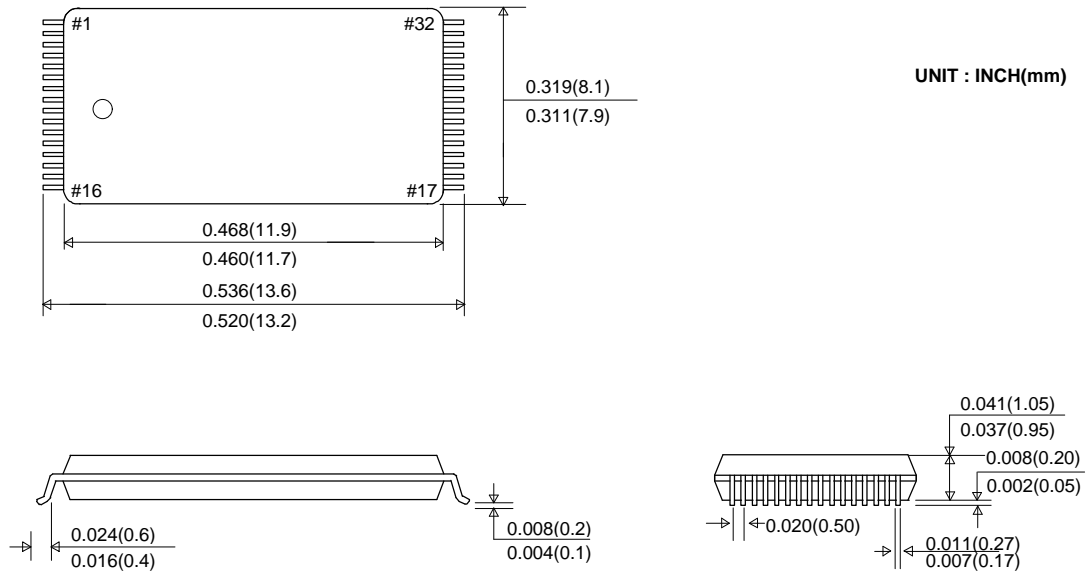
32pin 8x20mm Thin Small Outline Package Reversed(R1)



UNIT : INCH(mm)



32pin 8x13.4mm Smaller Thin Small Outline Package Standard(ST)



32pin 8x13.4mm Smaller Thin Small Outline Package Reversed (SR)

