

CD4049UBMS

CMOS Hex Buffer/Converter

FN3315
Rev 1.00
March 6, 2007

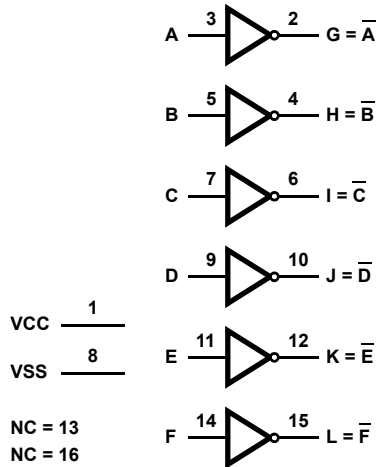
The CD4049UBMS is an inverting hex buffer and features logic level conversion using only one supply (voltage (VCC)). The input signal high level (VIH) can exceed the VCC supply voltage when this device is used for logic level conversions. This device is intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (VCC = 5V, VOL ≤ 0.4V, and IOL ≥ 3.3mA).

The CD4049UBMS is designated as replacement for CD4009UB. Because the CD4049UBMS requires only one power supply, it is preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB in all inverter, current driver, or logic level conversion applications. In these applications the CD4049UBMS is pin compatible with the CD4009UB, and can be substituted for this device in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UBMS, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UBMS is supplied in these 16 lead outline packages:

- Braze Seal DIP H4S
- Frit Seal DIP H1E
- Ceramic Flatpack H3X

Functional Diagram



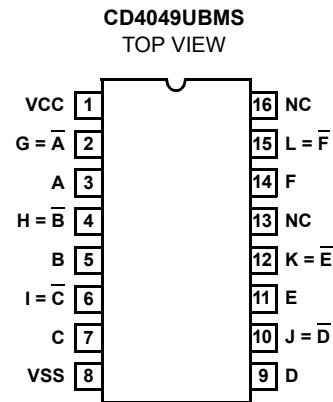
Features

- High Voltage Type (20V Rating)
- Inverting Type
- High Sink Current for Driving 2 TTL Loads
- High-to-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1mA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current “Sink” or “Source” Driver
- CMOS High-to-Low Logic Level Converter

Pinout



Schematic

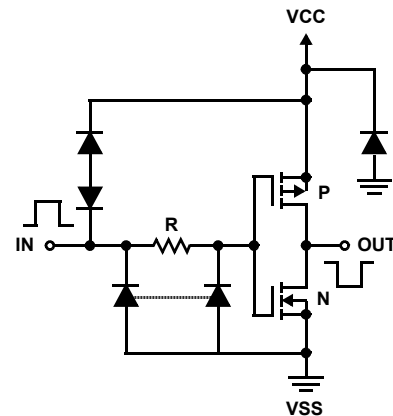


FIGURE 1. SCHEMATIC DIAGRAM, 1 OF 6 IDENTICAL UNITS

Ordering Information

| PART NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|------------------------|-------------------------|-----------------------------|-----------------------------|------------------------|
| CD4049UBDMSR | Q 5962R96 63601VEC | -55 to +125 | 16 Ld SBDIP, Solder Seal | D16.3 |
| CD4049UBKMSR | Q 5962R96 63601VXC | -55 to +125 | 16 Ld Flatpack, Solder Seal | K16.A |
| CD4049UBKNSR | Q 5962R96 63602VXC | -55 to +125 | 16 Ld Flatpack, Solder Seal | K16.A |

DC Electrical Specifications

| PARAMETER | SYMBOL | CONDITIONS (Note 1) | GROUP A SUBGROUPS | TEMP (°C) | LIMITS | | UNITS |
|--------------------------------|-----------------|--|----------------------|----------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Input Voltage Low (Note 2) | V _{IL} | V _{DD} = 5V, V _{OH} > 4.5V, V _{OL} < 0.5V | 1, 2, 3 | +25, +125, -55 | - | 1.0 | V |
| Input Voltage High (Note 2) | V _{IH} | V _{DD} = 5V, V _{OH} > 4.5V, V _{OL} < 0.5V | 1, 2, 3 | +25, +125, -55 | 4.0 | - | V |
| Input Voltage Low (Note 2) | V _{IL} | V _{DD} = 15V, V _{OH} > 13.5V, V _{OL} < 1.5V | 1, 2, 3 | +25, +125, -55 | - | 2.5 | V |
| Input Voltage High (Note 2) | V _{IH} | V _{DD} = 15V, V _{OH} > 13.5V, V _{OL} < 1.5V | 1, 2, 3 | +25, +125, -55 | 12.5 | - | V |

NOTES:

1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to V_{DD}. Limit is 0.050V max.

AC Electrical Specifications

| PARAMETER | SYMBOL | CONDITIONS (Notes 4, 5) | GROUP A SUBGROUPS | TEMP (°C) | LIMITS | | UNITS |
|-------------------|------------------|--|----------------------|-----------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Propagation Delay | t _{PHL} | V _{DD} = 5V, V _{IN} = V _{DD} or GND | 9 | +25 | - | 65 | ns |
| | | | 10, 11 | +125, -55 | - | 88 | ns |
| Propagation Delay | t _{PLH} | V _{DD} = 5V, V _{IN} = V _{DD} or GND | 9 | +25 | - | 120 | ns |
| | | | 10, 11 | +125, -55 | - | 162 | ns |
| Transition Time | t _{THL} | V _{DD} = 5V, V _{IN} = V _{DD} or GND | 9 | +25 | - | 60 | ns |
| | | | 10, 11 | +125, -55 | - | 81 | ns |
| Transition Time | t _{TLH} | V _{DD} = 5V, V _{IN} = V _{DD} or GND | 9 | +25 | - | 160 | ns |
| | | | 10, 11 | +125, -55 | - | 216 | ns |

NOTES:

4. C_L = 50pF, R_L = 200k, Input t_R, t_F < 20ns.
5. -55°C and +125°C limits guaranteed, 100% testing being implemented.

Post Irradiation Electrical Performance Characteristics

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMP (°C) | LIMITS | | UNITS |
|----------------|-----------------|---|-------|----------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Supply Current | I _{DD} | V _{DD} = 5V, V _{IN} = V _{DD} or GND | 6, 7 | -55, +25 | - | 1 | μA |
| | | | | +125 | - | 30 | μA |
| | | V _{DD} = 10V, V _{IN} = V _{DD} or GND | 6, 7 | -55, +25 | - | 2 | μA |
| | | | | +125 | - | 60 | μA |
| | | V _{DD} = 15V, V _{IN} = V _{DD} or GND | 6, 7 | -55, +25 | - | 2 | μA |
| +125 | - | 120 | μA | | | | |
| Output Voltage | V _{OL} | V _{DD} = 5V, No Load | 6, 7 | +25, +125, -55 | - | 50 | mV |
| Output Voltage | V _{OL} | V _{DD} = 10V, No Load | 6, 7 | +25, +125, -55 | - | 50 | mV |
| Output Voltage | V _{OH} | V _{DD} = 5V, No Load | 6, 7 | +25, +125, -55 | 4.95 | - | V |
| Output Voltage | V _{OH} | V _{DD} = 10V, No Load | 6, 7 | +25, +125, -55 | 9.95 | - | V |

Post Irradiation Electrical Performance Characteristics

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMP (°C) | LIMITS | | UNITS |
|-------------------------|-------------------|---|---------|----------------|--------|-------|-------|
| | | | | | MIN | MAX | |
| Output Current (Sink) | I _{OL4} | V _{DD} = 4.5V, V _{OUT} = 0.4V | 6, 7 | +125 | 1.8 | - | mA |
| | | | | -55 | 3.3 | - | mA |
| Output Current (Sink) | I _{OL5} | V _{DD} = 5V, V _{OUT} = 0.4V | 6, 7 | +125 | 2.4 | - | mA |
| | | | | -55 | 4.0 | - | mA |
| Output Current (Sink) | I _{OL10} | V _{DD} = 10V, V _{OUT} = 0.5V | 6, 7 | +125 | 5.6 | - | mA |
| | | | | -55 | 10 | - | mA |
| Output Current (Sink) | I _{OL15} | V _{DD} = 15V, V _{OUT} = 1.5V | 6, 7 | +125 | 18 | - | mA |
| | | | | -55 | 26 | - | mA |
| Output Current (Source) | I _{OH5A} | V _{DD} = 5V, V _{OUT} = 4.6V | 6, 7 | +125 | - | -0.48 | mA |
| | | | | -55 | - | -0.81 | mA |
| Output Current (Source) | I _{OH5B} | V _{DD} = 5V, V _{OUT} = 2.5V | 6, 7 | +125 | - | -1.55 | mA |
| | | | | -55 | - | -2.6 | mA |
| Output Current (Source) | I _{OH10} | V _{DD} = 10V, V _{OUT} = 9.5V | 6, 7 | +125 | - | -1.18 | mA |
| | | | | -55 | - | -2.0 | mA |
| Output Current (Source) | I _{OH15} | V _{DD} = 15V, V _{OUT} = 13.5V | 6, 7 | +125 | - | -3.1 | mA |
| | | | | -55 | - | -5.2 | mA |
| Input Voltage Low | V _{IL} | V _{DD} = 10V, V _{OH} > 9V, V _{OL} < 1V | 6, 7 | +25, +125, -55 | - | 2 | V |
| Input Voltage High | V _{IH} | V _{DD} = 10V, V _{OH} > 9V, V _{OL} < 1V | 6, 7 | +25, +125, -55 | 8 | - | V |
| Propagation Delay | t _{PHL} | V _{IN} = 10V, V _{DD} = 5V | 6, 7, 8 | +25 | - | 30 | ns |
| | | V _{IN} = 10V, V _{DD} = 10V | 6, 7, 8 | +25 | - | 40 | ns |
| Propagation Delay | t _{PLH} | V _{IN} = 10V, V _{DD} = 5V | 6, 7, 8 | +25 | - | 90 | ns |
| | | V _{IN} = 10V, V _{DD} = 10V | 6, 7, 8 | +25 | - | 65 | ns |
| Propagation Delay | t _{PHL} | V _{IN} = 15V, V _{DD} = 5V | 6, 7, 8 | +25 | - | 20 | ns |
| | | V _{IN} = 15V, V _{DD} = 15V | 6, 7, 8 | +25 | - | 30 | ns |
| Propagation Delay | t _{PLH} | V _{IN} = 15V, V _{DD} = 5V | 6, 7, 8 | +25 | - | 90 | ns |
| | | V _{IN} = 15V, V _{DD} = 15V | 6, 7, 8 | +25 | - | 50 | ns |
| Transition Time | t _{THL} | V _{DD} = 10V, V _{IN} = V _{DD} OR GND | 6, 7, 8 | +25 | - | 40 | ns |
| | | V _{DD} = 15V, V _{IN} = V _{DD} OR GND | 6, 7, 8 | +25 | - | 30 | ns |
| Transition Time | t _{TLH} | V _{DD} = 10V, V _{IN} = V _{DD} OR GND | 6, 7, 8 | +25 | - | 80 | ns |
| | | V _{DD} = 15V, V _{IN} = V _{DD} OR GND | 6, 7, 8 | +25 | - | 60 | ns |
| Input Capacitance | C _{IN} | Any Input | 6, 7 | +25 | - | 22.5 | pF |

NOTES:

6. All voltages referenced to device GND.
7. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
8. C_L = 50pF, R_L = 200k, Input t_R, t_F < 20ns.

Post Irradiation Electrical Performance Characteristics

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMP (°C) | LIMITS | | UNITS |
|---------------------------|------------------------|--|---------------|-----------|---------------------|---------------------|---------|
| | | | | | MIN | MAX | |
| Supply Current | I_{DD} | $V_{DD} = 20V, V_{IN} = V_{DD}$ or GND | 9, 12 | +25 | - | 7.5 | μA |
| N Threshold Voltage | V_{NTH} | $V_{DD} = 10V, I_{SS} = -10\mu A$ | 9, 12 | +25 | -2.8 | -0.2 | V |
| N Threshold Voltage Delta | ΔV_{TND} | $V_{DD} = 10V, I_{SS} = -10\mu A$ | 9, 12 | +25 | - | ± 1 | V |
| P Threshold Voltage | V_{TP} | $V_{SS} = 0V, I_{DD} = 10\mu A$ | 9, 12 | +25 | 0.2 | 2.8 | V |
| P Threshold Voltage Delta | ΔV_{TPD} | $V_{SS} = 0V, I_{DD} = 10\mu A$ | 9, 12 | +25 | - | ± 1 | V |
| Functional | F | $V_{DD} = 18V, V_{IN} = V_{DD}$ or GND | 9 | +25 | $V_{OH} > V_{DD}/2$ | $V_{OL} < V_{DD}/2$ | V |
| | | $V_{DD} = 3V, V_{IN} = V_{DD}$ or GND | | | | | |
| Propagation Delay Time | t_{PHL} t_{PLH} | $V_{DD} = 5V$ | 9, 10, 11, 12 | +25 | - | 1.35 x +25 Limit | ns |

NOTES:

9. All voltages referenced to device GND.
10. $C_L = 50pF, R_L = 200k$, Input $t_R, t_F < 20ns$.
11. See Table 2 for +25°C limit.
12. Read and Record

TABLE 1. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

| PARAMETER | SYMBOL | DELTA LIMIT |
|-------------------------|------------|-------------------------------|
| Supply Current - MSI-1 | I_{DD} | $\pm 0.2\mu A$ |
| Output Current (Sink) | I_{OL5} | $\pm 20\%$ x Pre-Test Reading |
| Output Current (Source) | I_{OH5A} | $\pm 20\%$ x Pre-Test Reading |

TABLE 2. APPLICABLE SUBGROUPS

| CONFORMANCE GROUP | MIL-STD-883 METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|-------------------------------|--------------------|---------------------------------------|------------------------------|
| Initial Test (Pre Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 1 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 2 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 13) | 100% 5004 | 1, 7, 9, Deltas | |
| Interim Test 3 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 13) | 100% 5004 | 1, 7, 9, Deltas | |
| Final Test | 100% 5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | 1, 7, 9 | |
| Group D | Sample 5005 | 1, 2, 3, 8A, 8B, 9 | Subgroups 1, 2, 3 |

NOTES:

13. 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 3. TOTAL DOSE IRRADIATION

| CONFORMANCE GROUPS | MIL-STD-883 METHOD | TEST | | READ AND RECORD | |
|--------------------|--------------------|-----------|------------|-----------------|------------|
| | | PRE-IRRAD | POST-IRRAD | PRE-IRRAD | POST-IRRAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 |

TABLE 4. BURN-IN AND IRRADIATION TEST CONNECTIONS

| FUNCTION | OPEN | GROUND | VDD | 9V ± 0.5V | OSCILLATOR | |
|----------------------------|-----------------------------|------------------|---------------------------|---------------------|--------------------|-------|
| | | | | | 50kHz | 25kHz |
| Static Burn-In 1 (Note 14) | 2, 4, 6, 10, 12, 13, 15 | 3, 5, 7-9, 11-14 | 1, 16 | | | |
| Static Burn-In 2 (Note 14) | 2, 4, 6, 10, 12, 13, 15 | 8 | 1, 3, 5, 7, 9, 11, 14, 16 | | | |
| Dynamic Burn-In (Note 16) | 13 | 8 | 1, 16 | 2, 4, 6, 10, 12, 15 | 3, 5, 7, 9, 11, 14 | |
| Irradiation (Note 15) | 2, 4, 6, 10, 12, 13, 15, 16 | 8 | 1, 3, 5, 7, 9, 11, 14 | | | |

NOTES:

- 14. Each pin except pin 1, pin 16, and GND will have a series resistor of $10k \pm 5\%$, $V_{DD} = 18V \pm 0.5V$
- 15. Each pin except pin 1, pin 16, and GND will have a series resistor of $47k \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, $V_{DD} = 10V \pm 0.5V$
- 16. Each pin except pin 1, pin 16, and GND will have a series resistor of $4.75k \pm 5\%$, $V_{DD} = 18V \pm 0.5V$

Typical Performance Characteristics

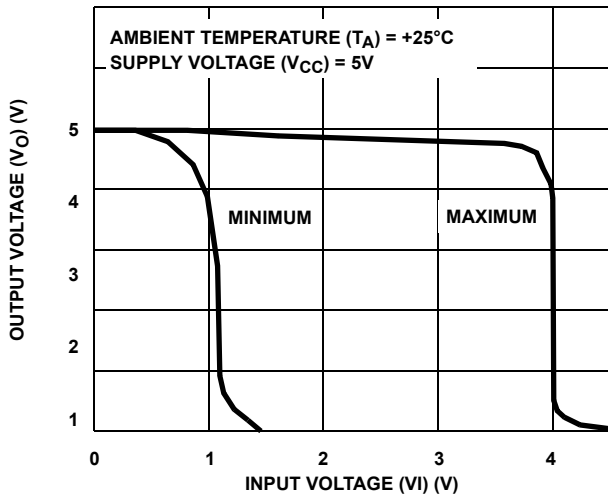


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

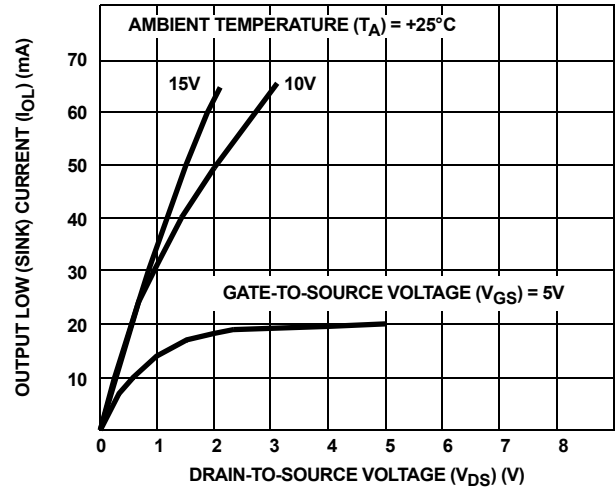


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

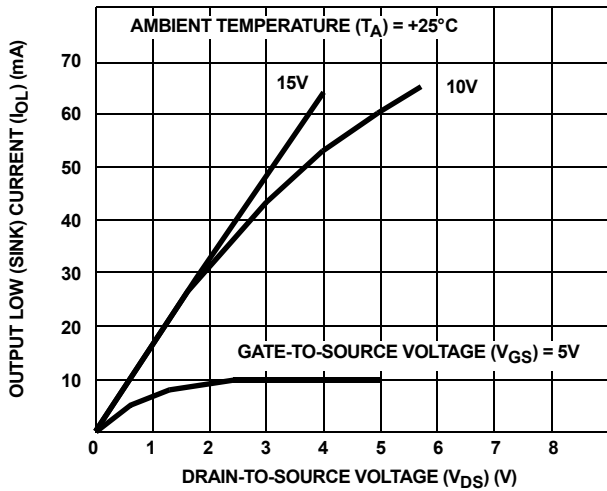


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

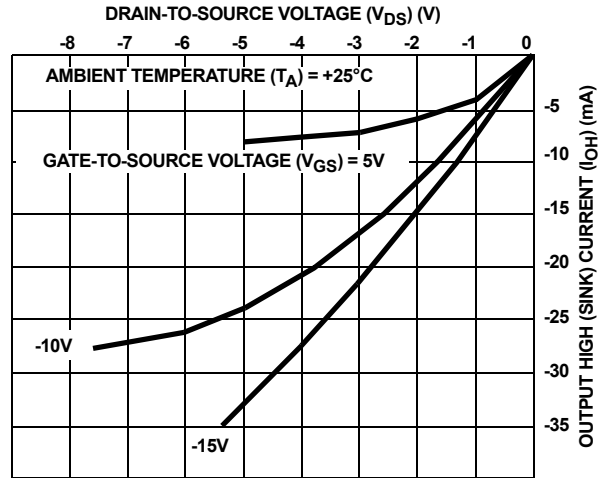


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

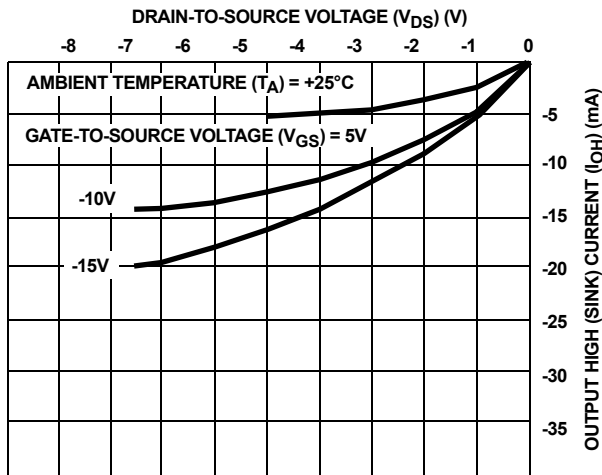


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

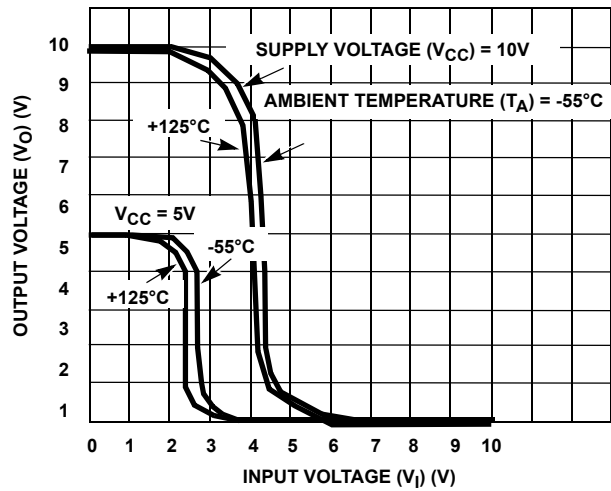


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

Typical Performance Characteristics (Continued)

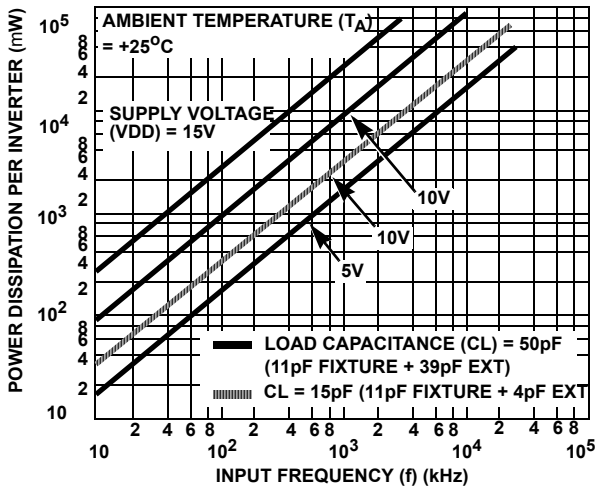


FIGURE 8. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

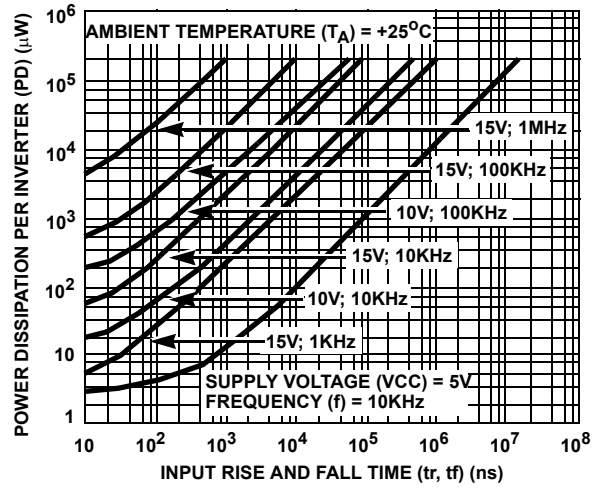
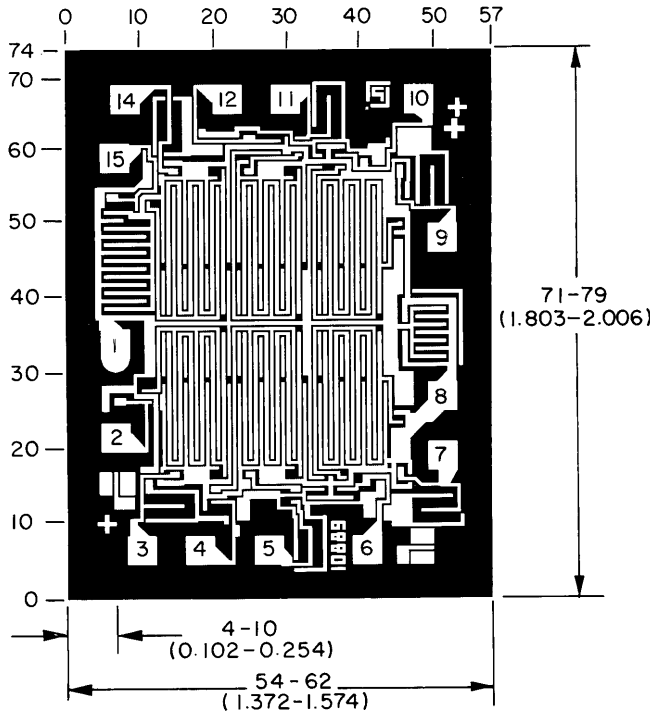


FIGURE 9. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

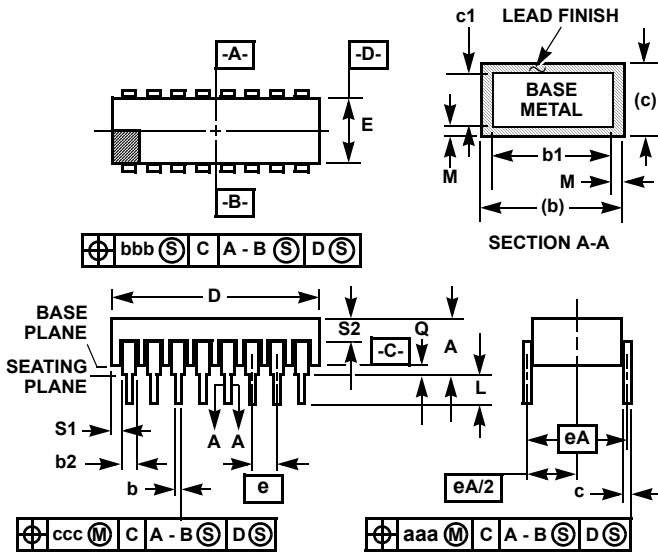
METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



**D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.840 | - | 21.34 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| α | 90° | 105° | 90° | 105° | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 16 | | 16 | | 8 |

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

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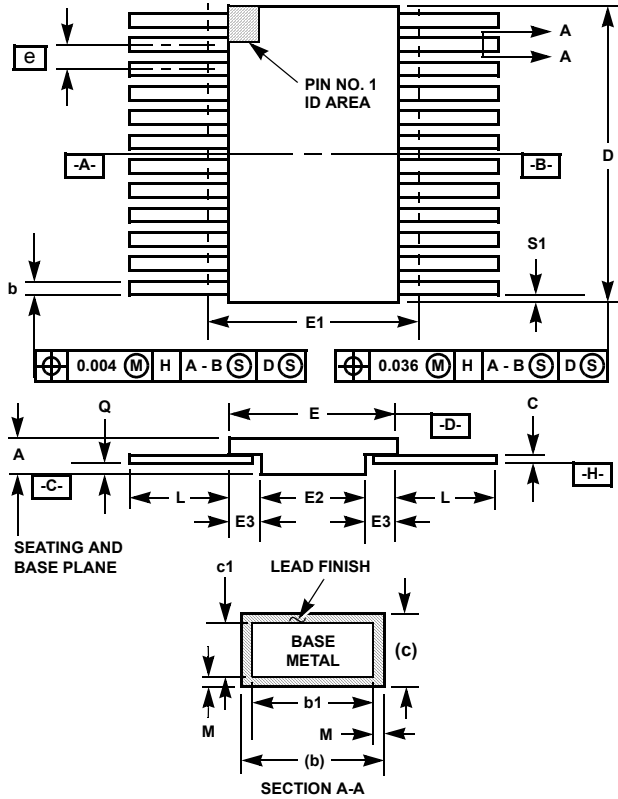
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Ceramic Metal Seal Flatpack Packages (Flatpack)



**K16.A MIL-STD-1835 CDFP4-F16 (F-5A, CONFIGURATION B)
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.045 | 0.115 | 1.14 | 2.92 | - |
| b | 0.015 | 0.022 | 0.38 | 0.56 | - |
| b1 | 0.015 | 0.019 | 0.38 | 0.48 | - |
| c | 0.004 | 0.009 | 0.10 | 0.23 | - |
| c1 | 0.004 | 0.006 | 0.10 | 0.15 | - |
| D | - | 0.440 | - | 11.18 | 3 |
| E | 0.245 | 0.285 | 6.22 | 7.24 | - |
| E1 | - | 0.315 | - | 8.00 | 3 |
| E2 | 0.130 | - | 3.30 | - | - |
| E3 | 0.030 | - | 0.76 | - | 7 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| k | 0.008 | 0.015 | 0.20 | 0.38 | 2 |
| L | 0.250 | 0.370 | 6.35 | 9.40 | - |
| Q | 0.026 | 0.045 | 0.66 | 1.14 | 8 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| M | - | 0.0015 | - | 0.04 | - |
| N | 16 | | 16 | | - |

Rev. 1 2-20-95

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH