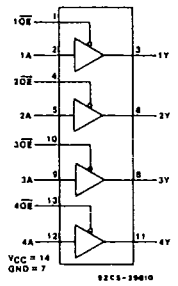
File Number 1771

CD54/74HC125
CD54/74HCT125

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Buffer; 3-State

Type Features:

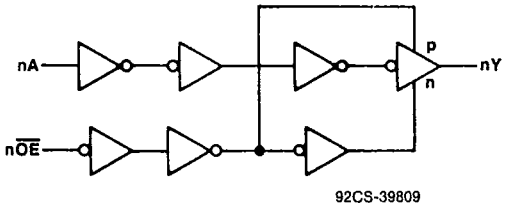
- *Separate output enable inputs*
- *3-state outputs*

The RCA-CD54/74HC125 and CD54/74HCT125 contain 4 independent 3-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high impedance state.

The CD54HC125 and CD54HCT125 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC125 and CD74HCT125 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



92CS-39809

Fig. 1 - Logic diagram.

TRUTH TABLE

Inputs		Outputs
nA	nOE	nY
H	L	H
L	L	L
X	H	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance, OFF State

CD54/74HC125
CD54/74HCT125

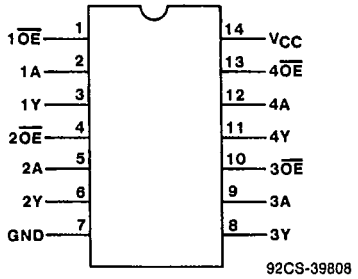
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5$ V) ..... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:* CD54/74HC Types CD54/74HCT Types	 2 4.5	 6 5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A: CD74 Types CD54 Types	 -40 -55	 +85 +125	°C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	 0 0 0	 1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC125
CD54/74HCT125

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC125/CD54HC125										CD74HCT125/CD54HCT125								UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
nA, $n\overline{OE}$	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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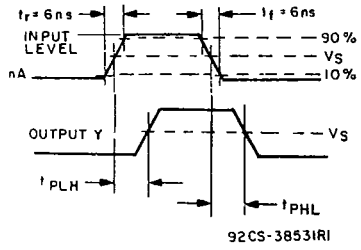
SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

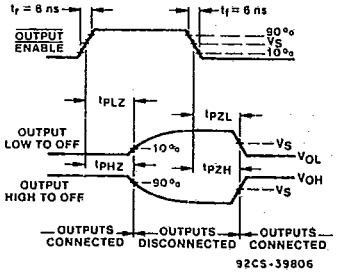
CHARACTERISTIC		C_L pF	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Time: (Fig. 2) nA to nY	t_{PHL} t_{PLH}	15	8	10	ns
Output Enabling Time	t_{PZL}, t_{PZH}	15	10	10	ns
Output Disabling Time	t_{PLZ}, t_{PHZ}	15	10	11	ns
Power Dissipation Capacitance*	C_{PD}	—	29	34	pF

*C_{PD} is used to determine the dynamic power consumption, per channel. $P_D=V_{CC}^2 f_i (C_{PD}+C_L)$ where: f_i=input frequency, C_L=load capacitance, V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC} V	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay Time nA to nY (Fig. 2)	t_{PLH} t_{PHL}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
		4.5	—	20	—	25	—	25	—	31	—	30	—	38	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Enable Delay Time (Fig. 2)	t_{PZH} t_{PZL}	2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	25	—	31	—	31	—	38	—	38	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Disable Delay Time	t_{PHZ}, t_{PLZ}	2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	28	—	31	—	35	—	38	—	42	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Ouput Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 — Transition and propagation delay times.

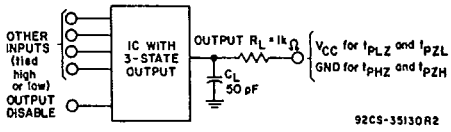


Fig. 3 - Three-state propagation delay test circuit.