ANALOG DEVICES

T-79-10

Low Noise, Low Drift Single-Supply Operational Amplifier

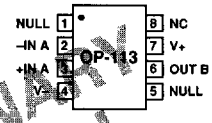
OP-113/OP-213/OP-413

FEATURES
Single-Supply Operation
Low Noise: 6 nV/√Hz @ 1 kHz
Wide Bandwidth: 3 MHz
Low Offset Voltage: 150 μV
Very Low Drift: 0.2 μV/°C
Unity-Gain Stable
No Phase Reversal

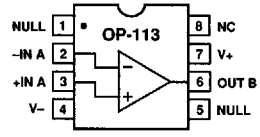
APPLICATIONS
Digital Scales
Multimedia
Strain Gages
Battery Powered Instrumentation
Temperature Transducer Amplifier

PIN CONNECTIONS

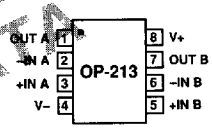
8-Lead Narrow-Body SOIC (S Suffix)



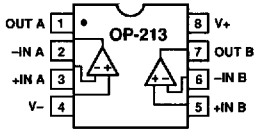
8-Lead Epoxy DIP (P Suffix)



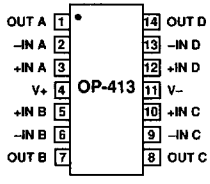
8-Lead Narrow-Body SOIC (S Suffix)



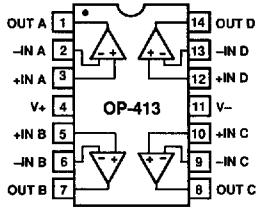
8-Lead Epoxy DIP (P Suffix)



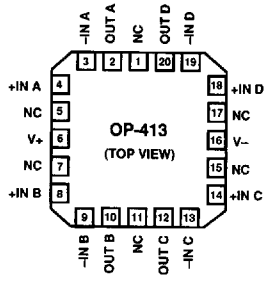
14-Lead Narrow-Body SOIC (S Suffix)



14-Lead Epoxy DIP (P Suffix)



20-Position Chip Carrier (RC Suffix)



GENERAL DESCRIPTION

Designed for systems with internal calibration, the OP-113 single, OP-213 dual and OP-413 quad operational amplifiers feature very low noise and drift. Drift and noise are parameters that are difficult to calibrate out. Most systems with internal calibration use a microprocessor and have +5 V and +12 V supplies, so these amplifiers are designed to be used in single-supply applications. They operate from 4.5 V to 30 V while maintaining precision performance. These unity gain stable amplifiers have a typical gain bandwidth of 3 MHz.

Systems that require low noise and single-supply operation include strain gage applications such as digital scales and multimedia. With a wide common-mode range, that includes the negative supply, and an output that swings from the negative supply to within 1 volt of the positive rail, are other parameters provided for these applications.

The OP-213 is specified over the extended industrial temperature range. Both single, dual and quad amplifiers are available in plastic and ceramic DIP plus SOIC surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

OP-113/OP-213/OP-413—SPECIFICATIONS T-79-10

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				150	μV
Input Bias Current	I_B	V_{CM} = 0 V		500	600	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V			200	nA
Input Voltage Range	V_{CM}		−15		+13	V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	86	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
		R_L = 10 kΩ		1500		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2		μV/°C
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz				%
Voltage Noise Density	e_N	f = 10 Hz				nV/√Hz
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz		0.3		μV p–p
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−15		+14	V
Short Circuit Limit	I_{SC}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±15 V		120		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞			4	mA
Supply Voltage Range	V_S		+4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1		V/μs
Full-Power Bandwidth	BW_p					kHz
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_0					Degrees

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				150	μV
Input Bias Current	I_B	V_{CM} = 2.5 V		500	600	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V			200	nA
Input Voltage Range	V_{CM}		0		4	V
Common-Mode Rejection	CMR	V_{CM} = ± V	86	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
		R_L = 10 kΩ		1500		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2		μV/°C
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz				%
Voltage Noise Density	e_N	f = 10 Hz				nV/√Hz
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz		0.3		μV p–p
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	0		+4	V
Short Circuit Limit	I_{SC}			±30		mA
POWER SUPPLY						
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞			3.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1		V/μs
Full-Power Bandwidth	BW_p					kHz
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_0					Degrees

Specifications subject to change without notice.

OP-113/OP-213/OP-413

T-79-10

WAFER TEST LIMITS (@ V_S = +5.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		150	mV max
Input Bias Current	I_B	V_{CM} = 0 V	600	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	200	nA max
Input Voltage Range[1]				V min
Common-Mode Rejection	CMRR	0 ≤ V_{CM} ≤ 4	86	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±15 V		μV/V
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	200	V/mV min
Output Voltage Range	V_O	R_L = 2 kΩ	4	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	3.5	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on DICE lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration to GND[3] . . . . . Indefinite
Storage Temperature Range
Z, RC Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-213A . . . . . −55°C to +125°C
OP-213G . . . . . −40°C to +85°C
Junction Temperature Range
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W
20-Contact LCC (RC)	98	38	°C/W

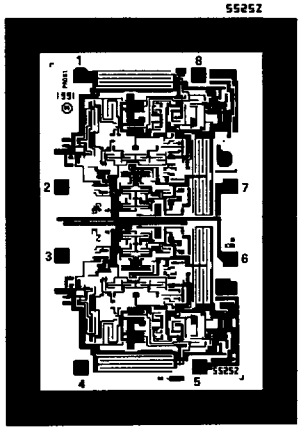
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]Shorts to either supply may destroy the device. See data sheet for full details.
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP113AZ/883	−55°C to +125°C	8-Pin Cerdip
OP113GP	−40°C to +85°C	8-Pin Plastic DIP
OP113GS	−40°C to +85°C	8-Pin SOIC
OP113GBC	+25°C	DICE
OP213AZ/883	−55°C to +125°C	8-Pin Cerdip
OP213ARC/883	−55°C to +125°C	20-Contact LCC
OP213GP	−40°C to +85°C	8-Pin Plastic DIP
OP213GS	−40°C to +85°C	8-Pin SOIC
OP213GBC	+25°C	DICE
OP413AZ/883	−55°C to +125°C	14-Pin Cerdip
OP413ARC/883	−55°C to +125°C	20-Contact LCC
OP413GP	−40°C to +85°C	14-Pin Plastic DIP
OP413GS	−40°C to +85°C	14-Pin SOIC
OP413GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-213 Die Size 0.062 in. × 0.097 in. (6,014 sq. mils.)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.