Philips Semiconductors-Signetics

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FAST Products	

FAST 74F552 Transceiver

Octal Registered Transceiver With Parity and Flags (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

FEATURES

- **8-Bit bidirectional I/O port with handshake**
- **Register status flag flip-flops**
- **Separate clock enable and output enable**
- **Parity generation and parity check**
- **B outputs and parity output sink 64mA**

DESCRIPTION

The 74F552 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ($\overline{CER}$, $\overline{CES}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{OEAS}$, $\overline{OEBR}$) for its 3-state buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B_0-B_7 is checked.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F552N
28-Pin Plastic SOL[1]	N74F552D

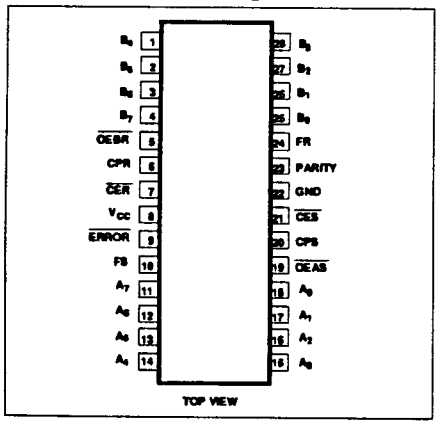
NOTE: Thermal mounting technique are recommended. See AN SMD-100 ProcessApplications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

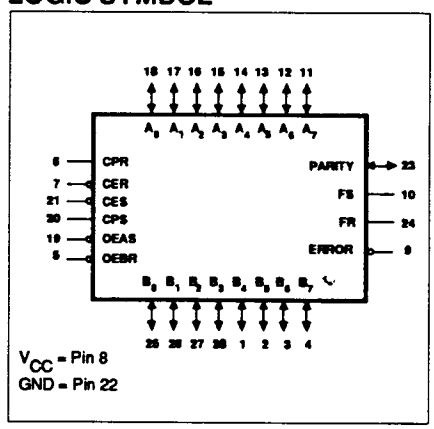
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A Data inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	B Data inputs	3.5/1.0	70µA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OEBR}$	A-to-B Output Enable input (active Low) and clear FS output (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OEAS}$	B-to-A Output Enable input (active Low) and clear FR output (active Low)	1.0/2.0	20µA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70µA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A_0 - A_7	A Data outputs	150/40	3.0mA/24mA
B_0 - B_7	B Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

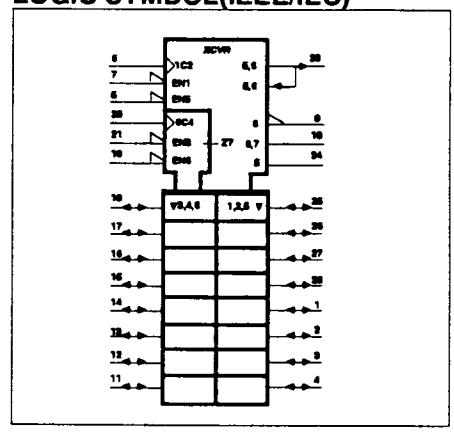
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR clock pulse, provided that the $\overline{CER}$ is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the $\overline{CER}$ returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the $\overline{OEBR}$ has gone Low. When $\overline{OEBR}$ is Low, a parity bit appears at the PARITY pin, which will be set High when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the $\overline{OEBR}$ pin from Low to High. Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the $\overline{CES}$ pin and a Low-to-High transition at the CPS pin enters the B input data and the parity input data into the S register and the parity register respectively and set the flag output FS to High. A Low signal at the $\overline{OEAS}$ pin enables the A port I/O pins and a Low-to-High transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is Low, the parity check output $\overline{ERROR}$ will be High if there is an odd number of 1s at the Q outputs of the S registers and the parity register.

R or S REGISTER FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
A_n or B_n	CPX	$\overline{CEX}$	INTERNAL Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	
X	↕	L	NC	Keep old data

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{CEX}$
↑ =Low-to-High transition
↕ =Not Low-to-High transition

OUTPUT CONTROL TABLE

INPUT	OUTPUTS		OPERATING MODE
$\overline{OEXX}$	INTERNAL Q	A_n or B_n	
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AS or BR
Z =High impedance "off" state

R or S FLAG FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{CEX}$	CPX	$\overline{OEXX}$	FR or FS	
H	X	↕	NC	Hold flag
L	↑	↕	H	Set flag
X	X	↑	L	Clear flag

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{CEX}$
XX=AS or BR
↑ =Low-to-High transition
↕ =Not Low-to-High transition

PARITY GENERATION FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
$\overline{OEBR}$	CPR	Number of Highs in The Q outputs of the R register	PARITY	
H	X	X	Z	Hold data
L	↑	0,2,4,6,8	H	Load data
L	↑	1,3,5,7	L	

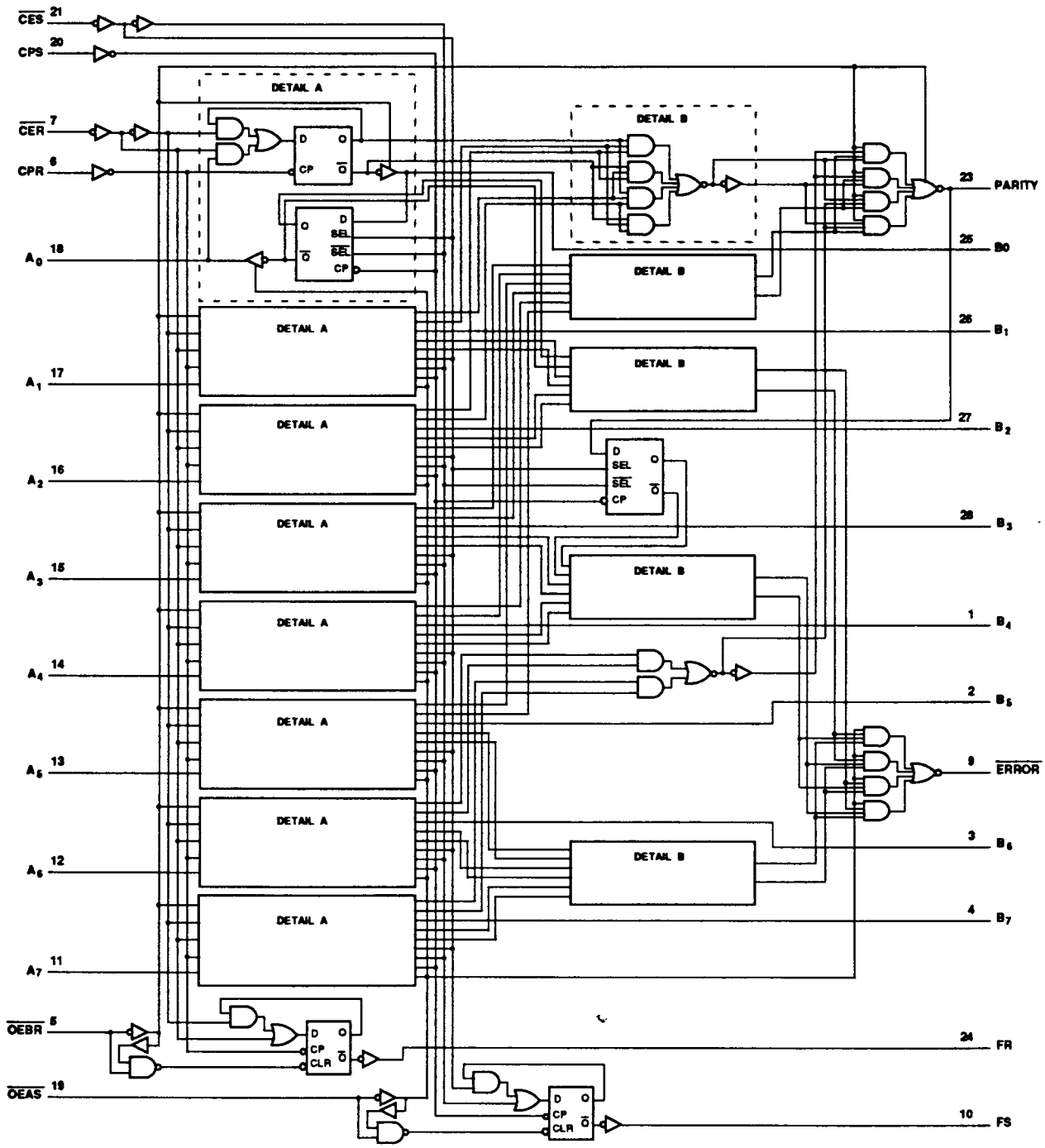
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state
↑ =Low-to-High transition

PARITY CHECK FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{OEAS}$	CPS	PARITY	Number of Highs in The Q outputs of the R register	$\overline{ERROR}$	
H	X	X	X	H	Parity check
L	↑	L	0,2,4,6,8	L	
L	↑	L	1,3,5,7	H	
L	↑	H	0,2,4,6,8	H	
L	↑	H	1,3,5,7	L	

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High transition

LOGIC DIAGRAM



V_{CC}=Pin 8
GND=Pin 22

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to $+V_{CC}$	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	FR, FS, $\overline{ERROR}$	40	mA
		A_0- A_7	48	mA
		B_0- B_7, PARITY	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	FR, FS, $\overline{ERROR}$			-1	mA
		A_0- A_7			-3	mA
		B_0- B_7, PARITY			-15	mA
I_{OL}	Low-level output current	FR, FS, $\overline{ERROR}$			20	mA
		A_0- A_7			24	mA
		B_0- B_7, PARITY			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		A_0- A_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0- B_7, PARITY		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		A_0- A_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0- B_7, PARITY		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		A_0- A_7, B_0- B_7, PARITY	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	others except A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{OEAS}$, $\overline{OEBA}$						-1.2	mA
I_{OZH}+ I_{IH}	Off-state output current, High-level voltage applied	A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{OZL}+ I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit Output current[3]	A_0-A_7, FS, FR, $\overline{ERROR}$	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, PARITY				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				115	170	mA
		I_{CCL}					125	185	mA
		I_{CCZ}					120	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

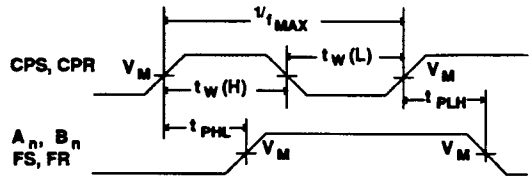
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CPS to A_n or CPR to B_n	Waveform 1	3.5 4.0	5.0 6.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
t_{PLH}	Propagation delay CPS to FS or CPR to FR	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t_{PHL}	Propagation delay $\overline{OEAS}$ to FS or $\overline{OEBR}$ to FR	Waveform 2	4.0	6.0	8.5	3.5	9.0	ns
t_{PLH} t_{PHL}	Propagation delay CPS to $\overline{ERROR}$	Waveform 4	6.5 7.5	13.0 11.5	16.5 15.0	6.0 7.0	18.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CPR to PARITY	Waveform 4	6.5 10.5	8.5 13.5	11.0 17.0	5.5 10.0	12.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEAS}$ to $\overline{ERROR}$	Waveform 3	3.5 3.0	5.5 5.0	8.0 7.0	3.0 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEAS}$ to A_n or $\overline{OEBR}$ to B_n	Waveform 7 Waveform 8	2.5 4.0	4.0 6.5	7.0 9.5	2.0 4.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEAS}$ to A_n or $\overline{OEBR}$ to B_n	Waveform 7 Waveform 8	2.0 2.0	4.0 3.5	7.0 7.0	1.5 1.5	8.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBR}$ to PARITY	Waveform 7 Waveform 8	2.0 4.0	4.0 5.5	7.0 8.0	2.0 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disnable time $\overline{OEBR}$ to PARITY	Waveform 7 Waveform 8	2.0 2.0	4.0 4.0	7.0 7.5	2.0 2.0	7.5 8.0	ns

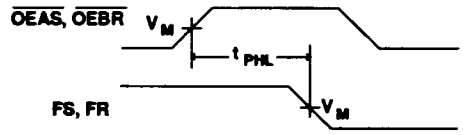
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.5		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	7.0 7.0			7.5 7.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	0 0			0 0		ns
t_w(H) t_w(L)	CPS or CPR Pulse width, High or Low	Waveform 1	5.0 6.5			6.5 7.5		ns
t_{REC}	Recovery time $\overline{OEBR}$ to CPR or $\overline{OEAS}$ to CPS	Waveform 6	14.5			16.5		ns

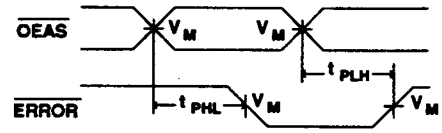
AC WAVEFORMS



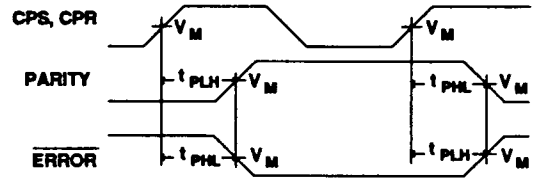
Waveform 1. Propagation Delay, Clock input to output and maximum clock frequency



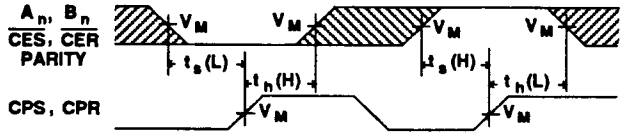
Waveform 2. Propagation Delay, Output Enable to Flag output



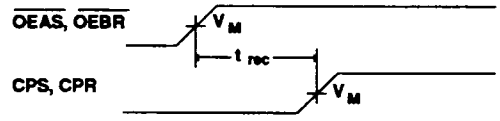
Waveform 3. Propagation Delay, Output Enable to $\overline{ERROR}$



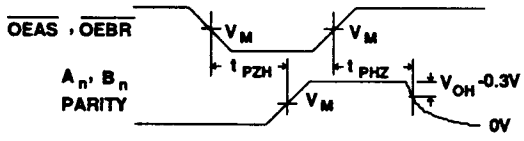
Waveform 4. Propagation Delay, Clock to PARITY and $\overline{ERROR}$



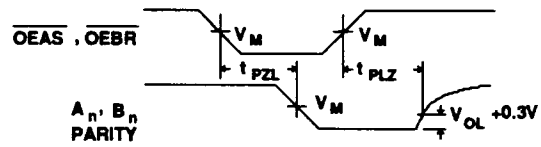
Waveform 5. Data Setup And Hold Times



Waveform 6. Recovery time from Output Enable to Clock



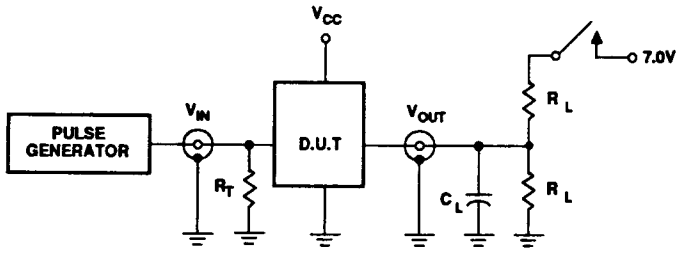
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level



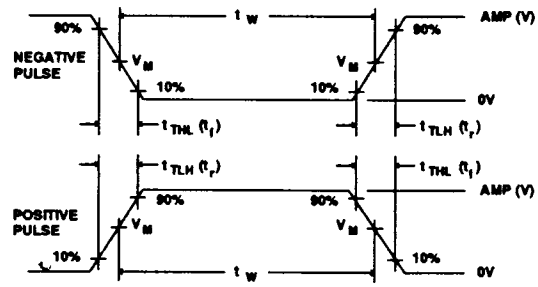
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns