D3199, NOVEMBER 1988

- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**

description

The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT543 is characterized for operation from 0°C to 70°C.

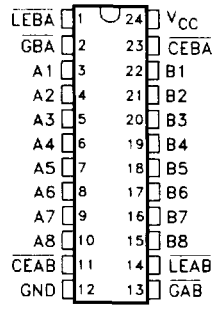
FUNCTION TABLE

INPUTS				OUTPUTS	LATCH STATUS
$\overline{GAB}$	$\overline{CEAB}$	$\overline{LEAB}$	DATA	B1 THRU B8	A TO B†
H	X	X	X	Z	OUTPUTS DISABLED
L	H	L	L	Z	OUTPUTS DISABLED
L	H	L	H	Z	DATA LATCHED
L	L	H	H	L	DATA LATCHED‡
L	L	H	H	H	
L	L	L	L	L	TRANSPARENT
L	L	L	H	H	

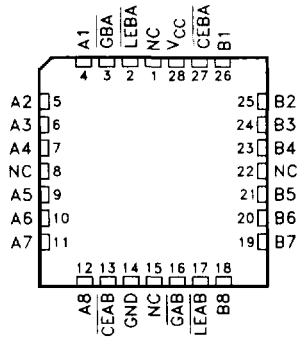
† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.

‡ Data present before low-to-high transition of $\overline{LEAB}$.

SN54BCT543 ... JT PACKAGE
SN74BCT543 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT543 ... FK PACKAGE
(TOP VIEW)

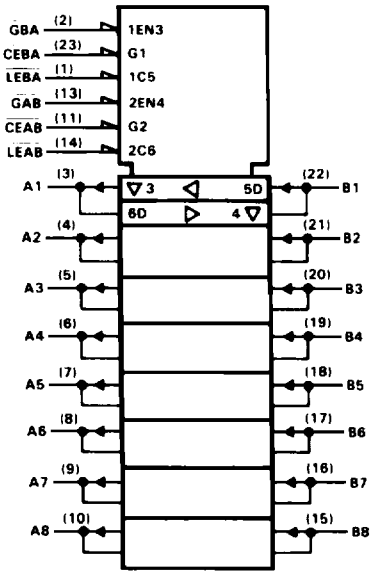


NC—No internal connection

2

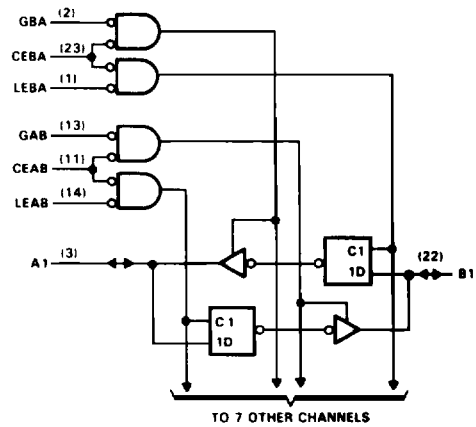
BiCMOS Circuits

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (I/O ports) (see Note 1)	−0.5 V to 5.5 V
Input voltage (Excluding I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT543	96 mA
SN74BCT543	128 mA
Operating free-air temperature range: SN54BCT543	−55°C to 125°C
SN74BCT543	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT543			SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT543			SN74BCT543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.4			0.4	mA
I_{IH}§	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A and B					70			70	
I_{IL}§	Control inputs	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
	A and B					−0.65			−0.65	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}		V_{CC} = 5.5 V			45	71		45	71	mA
I_{CCH}		V_{CC} = 5.5 V			5	8		5	8	mA
I_{CCZ}		V_{CC} = 5.5 V			9	15		5	15	mA
C_i	Control inputs	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_{io}	A and B	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			16			16		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN TO MAX†				UNIT
		'BCT543		SN54BCT543		SN74BCT543		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before latch enable ↑	4.5		4.5		4.5		ns
t_h	Hold time, data after latch enable ↑	1.5		1.5		1.5		ns
t_w	Pulse duration, latch enable low	7		7		7		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN TO MAX†				UNIT
			'BCT543			SN54BCT543		SN74BCT543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	5.7	7.5	2	9.9	2	8.8	ns
t_{PHL}			2	6.3	8.2	2	9.7	2	9.6	
t_{PLH}	$\overline{LE}$	A or B	2	8.2	10.3	2	13.9	2	12.9	ns
t_{PHL}			2	8.5	10.6	2	13.2	2	12.7	
t_{PZH}	$\overline{G}$	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
t_{PZL}			1	8.7	10.8	1	12.8	1	12.3	
t_{PHZ}	$\overline{G}$	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
t_{PLZ}			1	4.7	6.4	1	8.1	1	7.2	
t_{PZH}	$\overline{CE}$	A or B	1	7.6	9.8	1	12.8	1	12	ns
t_{PZL}			1	9.5	11.6	1	13.8	1	13.5	
t_{PHZ}	$\overline{CE}$	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
t_{PLZ}			1	4.8	6.7	1	8.4	1	7.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

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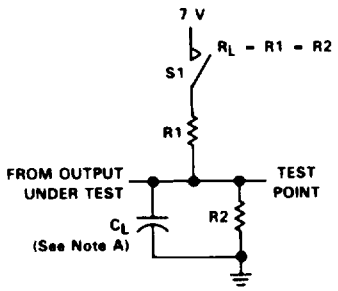
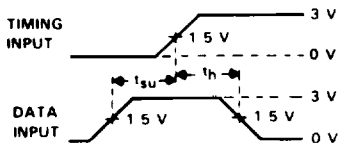
PARAMETER MEASUREMENT INFORMATION



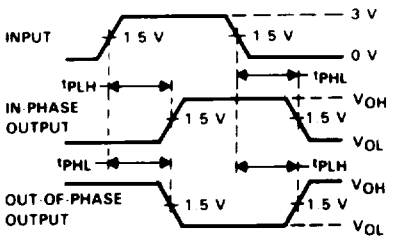
LOAD CIRCUIT

SWITCH POSITION TABLE

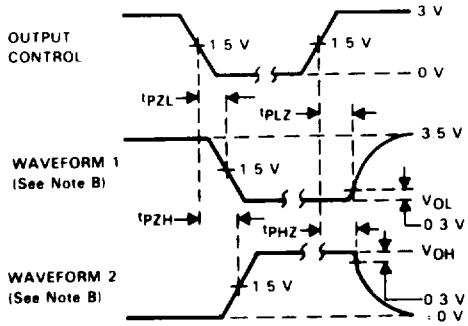
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS