Am29LV400B

4 Megabit (512 K x 8-Bit/256 K x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.32 µm process technology**
  - — Compatible with 0.5 µm Am29LV400 device
- **High performance**
  - — Full voltage range: access times as fast as 70 ns
  - — Regulated voltage range: access times as fast as 50 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 7 mA read current
  - — 15 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and seven 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Package option**
  - — 48-ball FBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

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GENERAL DESCRIPTION

The Am29LV400B is a 4 Mbit, 3.0 volt-only Flash memory organized as 524,288 bytes or 262,144 words. The device is offered in 48-ball FBGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system using only a single 3.0 volt V_{CC} supply. No V_{PP} is required for write or erase operations. The device can also be programmed in standard EPROM programmers.

This device is manufactured using AMD's 0.32 µm process technology, and offers all the features and benefits of the Am29LV400, which was manufactured using 0.5 µm process technology. In addition, the Am29LV400B features unlock bypass programming and in-system sector protection/unprotection.

The standard device offers access times of 50, 55, 70, 90 and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically pre-programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

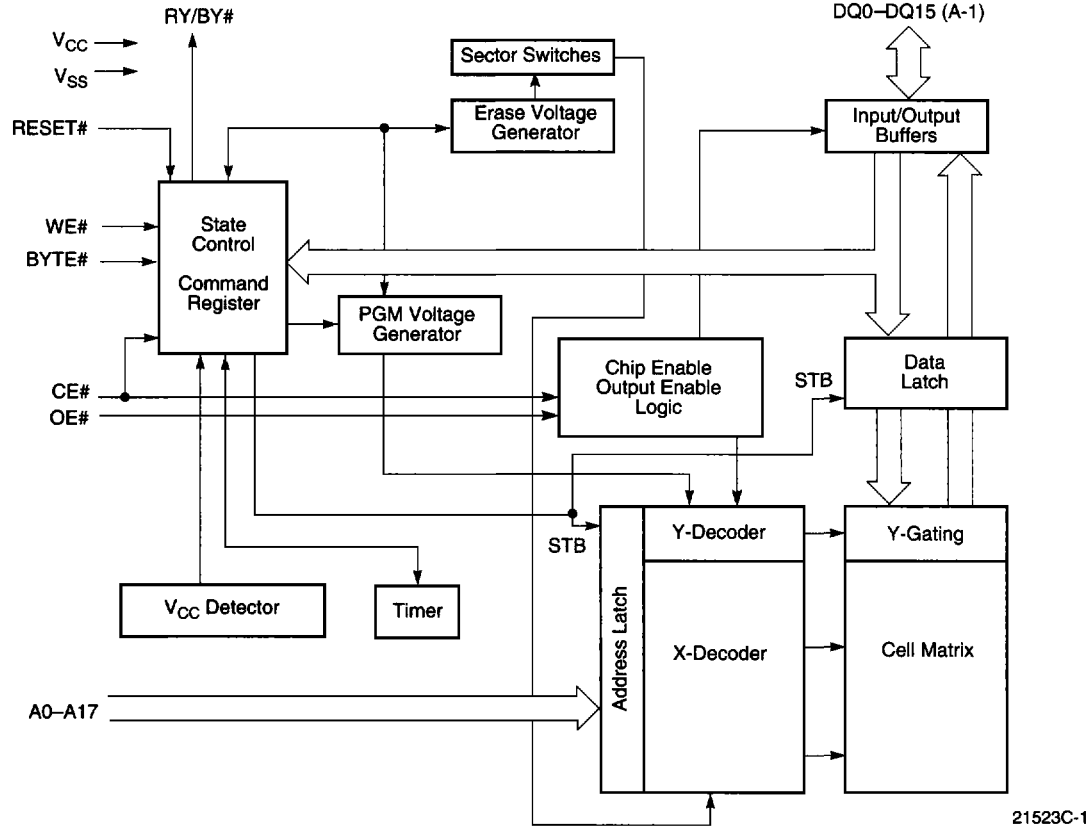
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

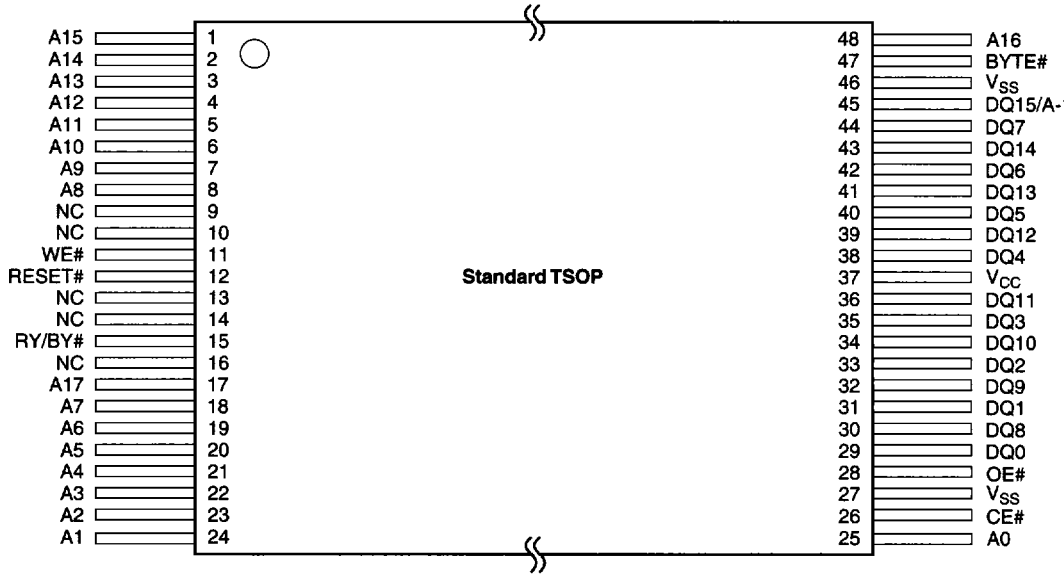
Family Part Number		Am29LV400B				
Speed Options	Regulated Voltage Range: 3.0 – 3.6 V	**50R**	**55R**			
	Full Voltage Range: 2.7 – 3.6 V			**70**	**90**	**120**
Max access time, ns (t_{ACC})		50	55	70	90	120
Max CE# access time, ns (t_{CE})		50	55	70	90	120
Max OE# access time, ns (t_{OE})		30	30	30	35	50

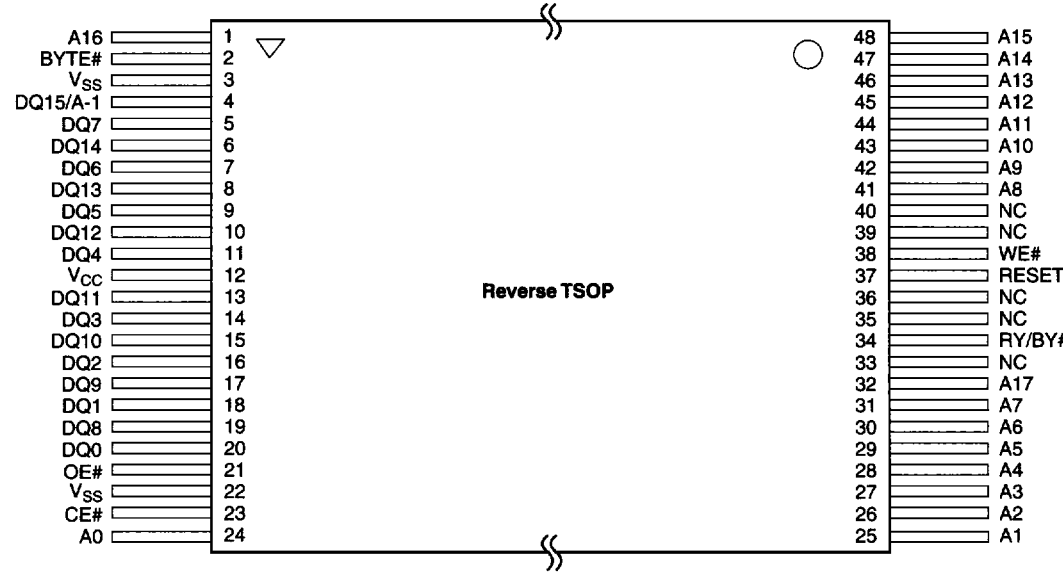
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS





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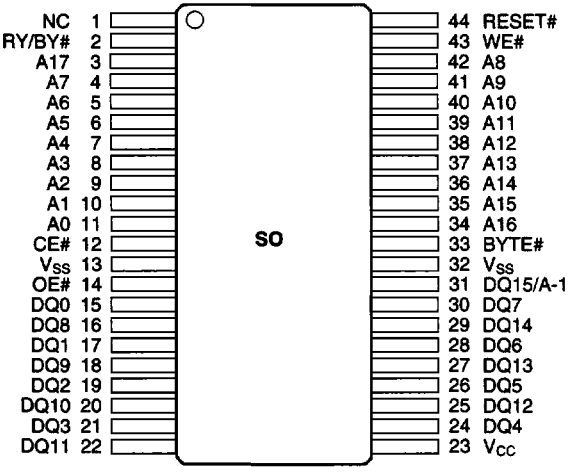
CONNECTION DIAGRAMS



FBGA
Top View, Balls Facing Down

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	NC	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	NC	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

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Special Handling Instructions for Fine Pitch Ball Grid Array (FBGA)

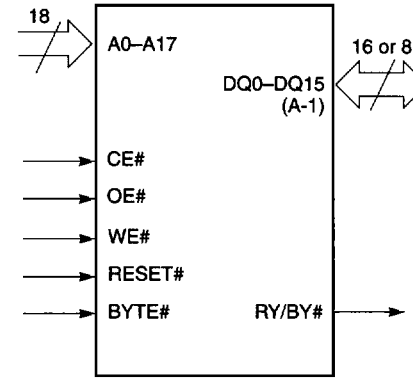
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A17	=	18 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin, active low
RY/BY#	=	Ready/Busy# output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



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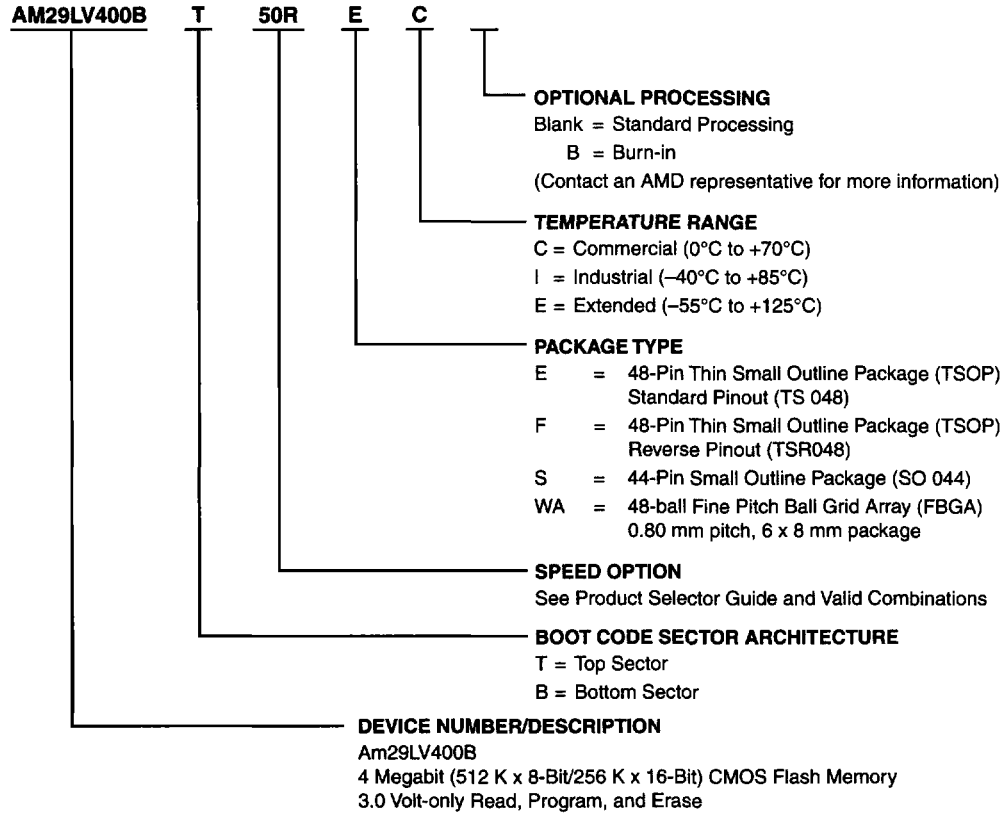
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations for TSOP and SO Packages	
AM29LV400BT50R, AM29LV400BB50R	EC, EI, FC, FI, SC, SI
AM29LV400BT55R, AM29LV400BB55R	
AM29LV400BT70, AM29LV400BB70	EC, EI, EE, FC, FI, FE, SC, SI, SE
AM29LV400BT90, AM29LV400BB90	
AM29LV400BT120, AM29LV400BB120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29LV400BT50R, AM29LV400BB50R	WAC, WAI	L400BT50R, L400BB50R	C, I
AM29LV400BT55R, AM29LV400BB55R		L400BT55R, L400BB55R	
AM29LV400BT70, AM29LV400BB70	WAC, WAI, WAE	L400BT70V, L400BB70V	C, I, E
AM29LV400BT90, AM29LV400BB90		L400BT90V, L400BB90V	
AM29LV400BT120, AM29LV400BB120		L400BT12V, L400BB12V	

DEVICE BUS OPERATIONS

For further details see "Device Bus Operations" on page 5-364.

Table 1. Am29LV400B Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Addresses In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. *Addresses are A17:A0 in word mode (BYTE# = V_{IH}), A17:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See "Sector Protection/Unprotection" on page 5-366.*

Table 2. Am29LV400BT Top Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
								(x8) Address Range	(x16) Address Range
SA0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
SA1	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA2	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA3	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA4	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA5	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA6	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA7	1	1	1	0	X	X	32/16	70000h–77FFFh	38000h–3BFFFh
SA8	1	1	1	1	0	0	8/4	78000h–79FFFh	3C000h–3CFFFh
SA9	1	1	1	1	0	1	8/4	7A000h–7BFFFh	3D000h–3DFFFh
SA10	1	1	1	1	1	X	16/8	7C000h–7FFFFh	3E000h–3FFFFh

Table 3. Am29LV400BB Bottom Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
								(x8) Address Range	(x16) Address Range
SA0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh
SA1	0	0	0	0	1	0	8/4	04000h–05FFFh	02000h–02FFFh
SA2	0	0	0	0	1	1	8/4	06000h–07FFFh	03000h–03FFFh
SA3	0	0	0	1	X	X	32/16	08000h–0FFFFh	04000h–07FFFh
SA4	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA5	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA6	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA7	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA8	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA9	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA10	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh

Note for Tables 2 and 3: *Address range is A17:A-1 in byte mode and A17:A0 in word mode. See "Word/Byte Configuration" on page 5-364 for more information.*

Table 4. Am29LV400B Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A17 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	X	L	L	X	01h
Device ID: Am29LV400B (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	B9h
	Byte	L	L	H									X	B9h
Device ID: Am29LV400B (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	BAh
	Byte	L	L	H									X	BAh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

COMMAND DEFINITIONS

For further details see "Command Definitions" on page 5-373.

Table 5. Am29LV400B Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2–5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	01				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22B9				
		Byte		AAA		555		AAA		X02	B9				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22BA				
		Byte		AAA		555		AAA		X02	BA				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00 XX01				
		Byte		AAA		555		AAA		(SA) X04	00 01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	XXX	B0										
Erase Resume (Note 13)			1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A17–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A17–A11 are don't cares for unlock and command cycles, except when SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" on page 5-369 for more information.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume command is valid only during the Erase Suspend mode.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and
RESET# (Note 2). . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 2.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . +3.0 V to +3.6 V

V_{CC} for full voltage range . . . . . +2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

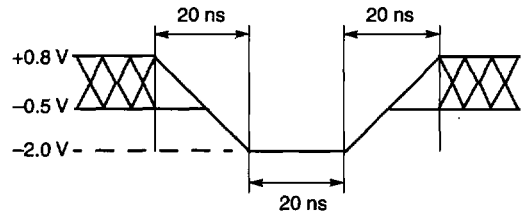


Figure 1. Maximum Negative Overshoot Waveform

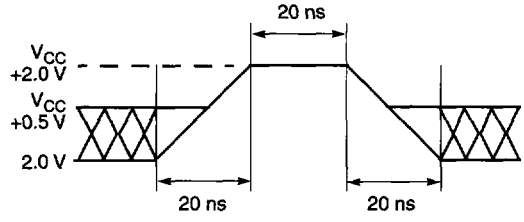


Figure 2. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS

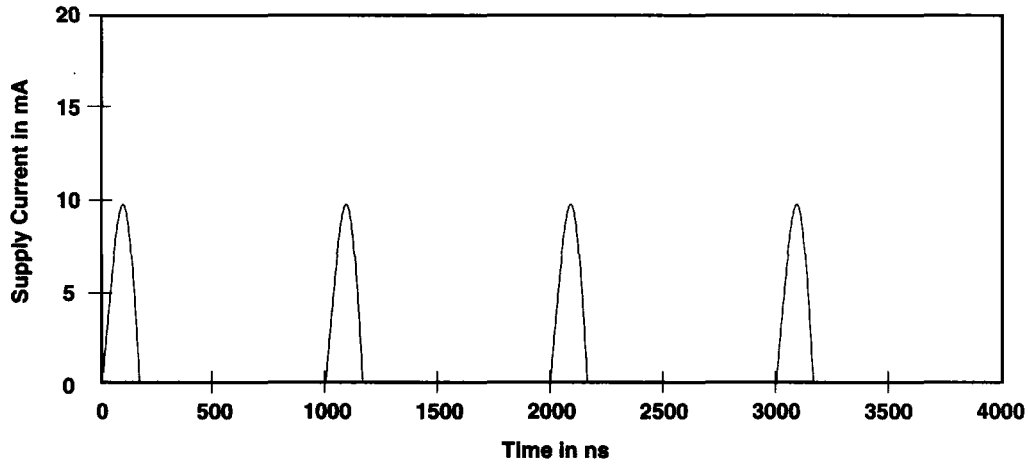
CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		7	12	mA
			1 MHz		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		7	12	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 5)	CE# = V_{IL}, OE# = V_{IH}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC}±0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
5. *Not 100% tested.*

DC CHARACTERISTICS
Zero Power Flash



Note: *Addresses are switching at 1 MHz*

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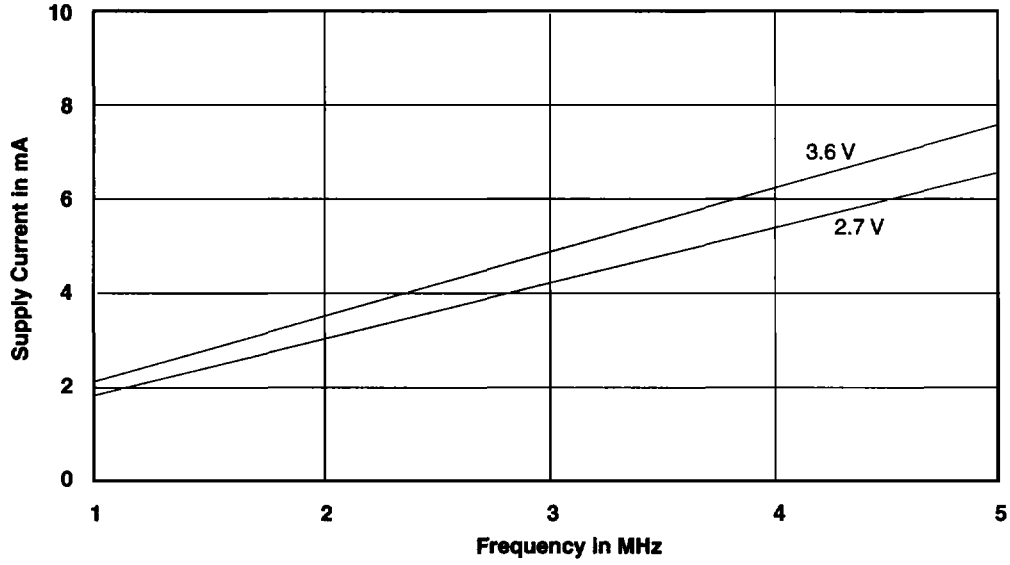
Figure 3. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

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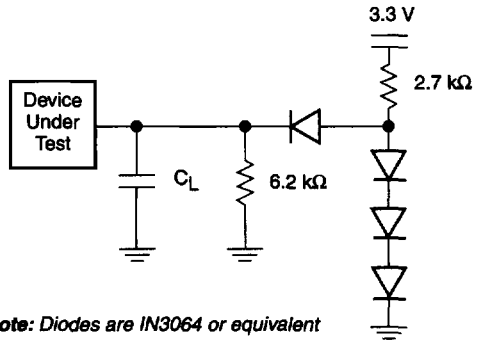
Figure 4. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

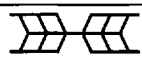
21523C-9

Figure 5. Test Setup

Table 6. Test Specifications

Test Condition	50R, 55R, 70,	90, 120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5	V	
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

21523C-10

Figure 6. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Options					Unit
JEDEC	Std					50R	55R	70	90	120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	50	55	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	50	55	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	50	55	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	30	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	25	25	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	25	25	25	30	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0					ns
			Toggle and Data# Polling		Min	10					ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0					ns

Notes:

1. *Not 100% tested.*
2. *See Figure 5 and Table 6 for test specifications.*

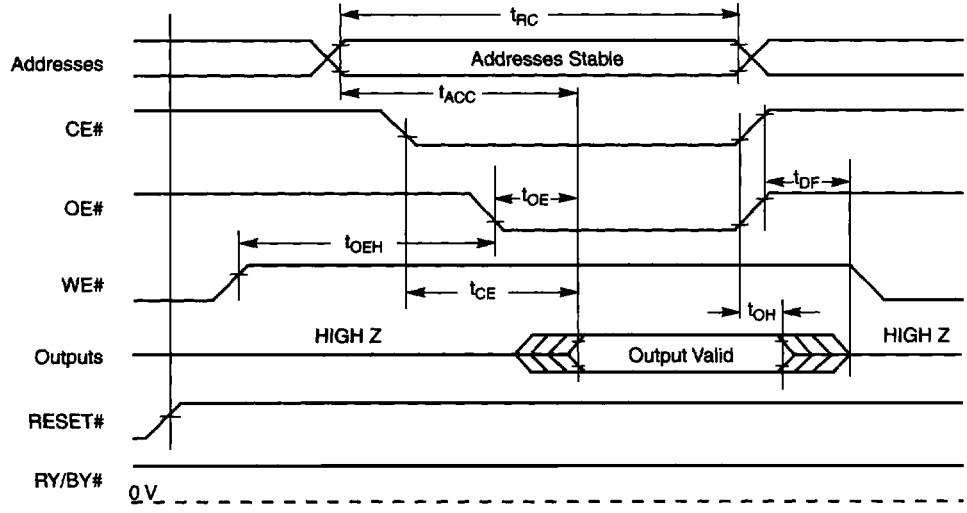


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Figure 7. Read Operations Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

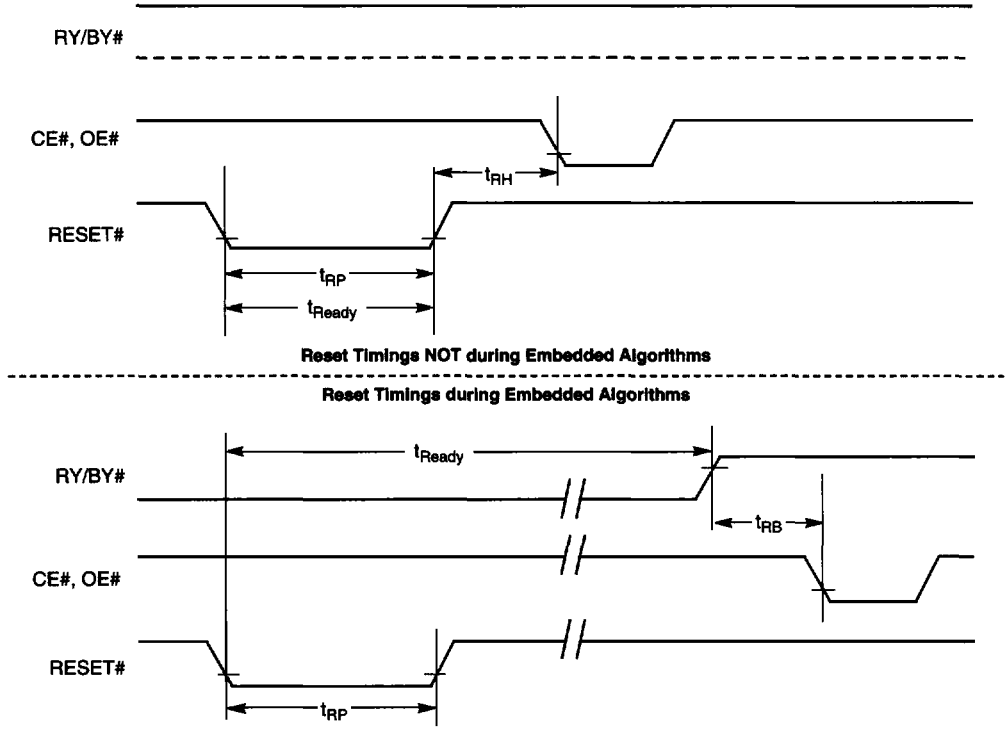

Figure 8. RESET# Timings

AC CHARACTERISTICS
Word/Byte Configuration (BYTE#)

Parameter				Speed Options					
JEDEC	Std	Description		50R	55R	70	90	120	Unit
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5					ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	25	25	25	30	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	50	55	70	90	120	ns

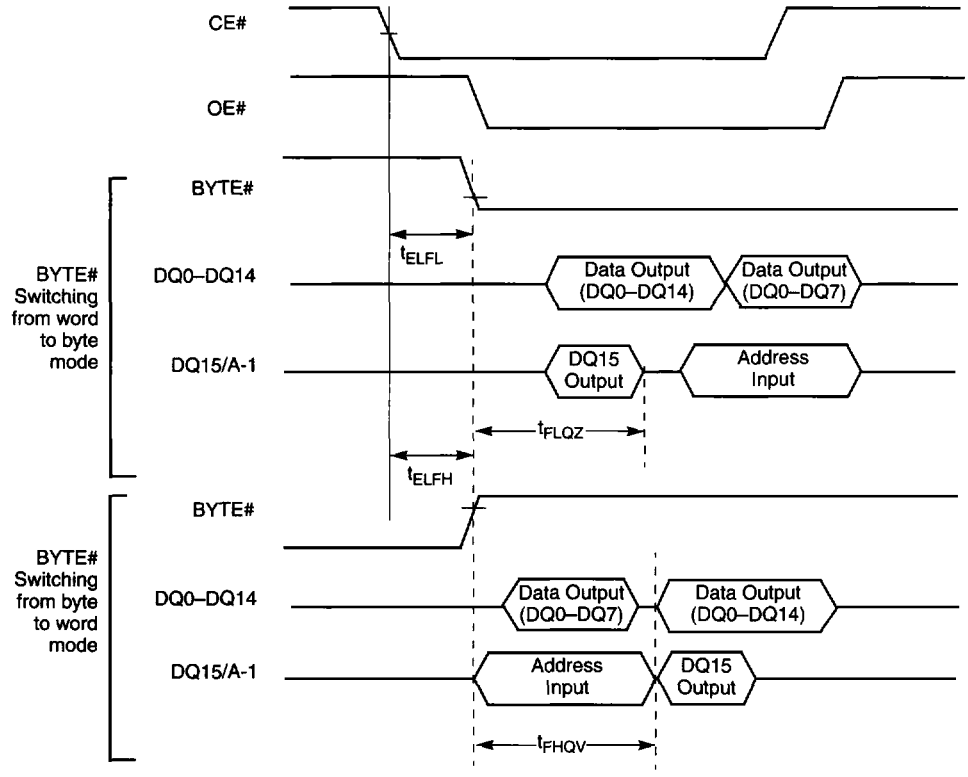

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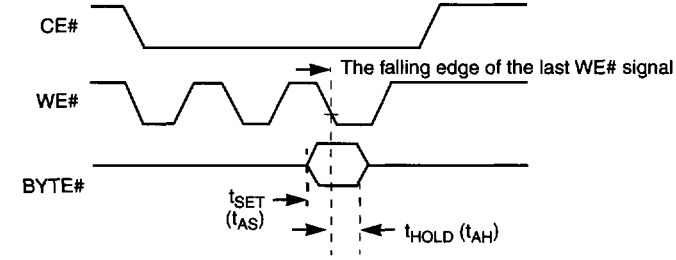
Figure 9. BYTE# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

21523C-14

Figure 10. BYTE# Timings for Write Operations

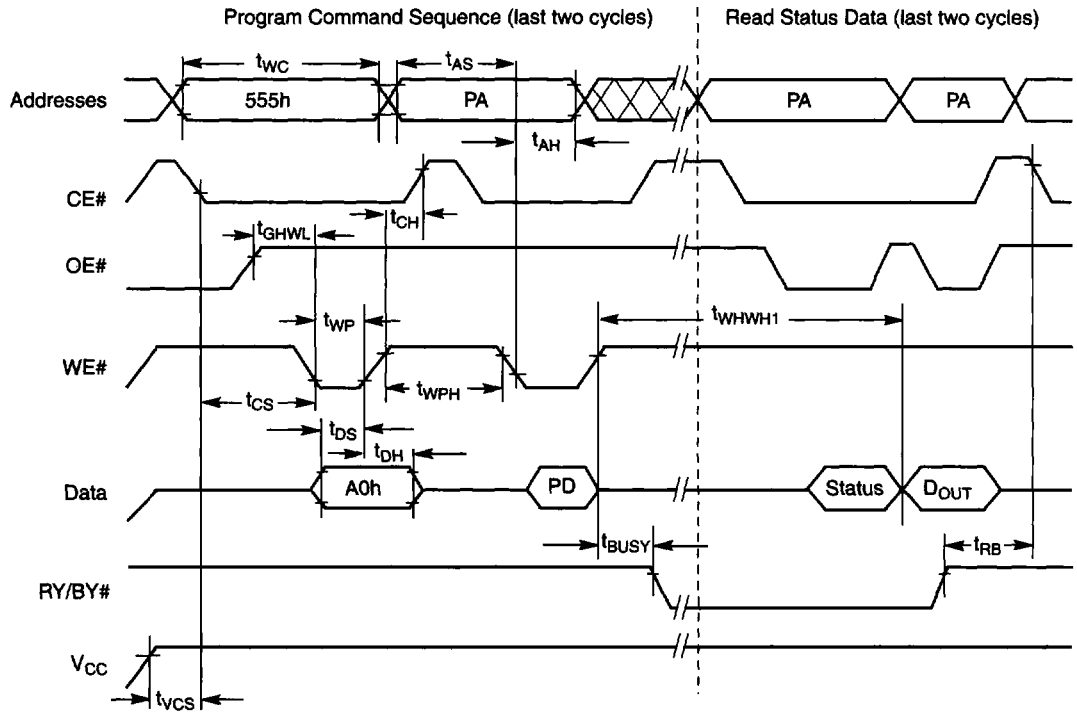
AC CHARACTERISTICS
Erase/Program Operations

Parameter					Speed Options					
JEDEC	Std	Description			50R	55R	70	90	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	50	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0					ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0					ns
	t_{OES}	Output Enable Setup Time		Min	0					ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0					ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0					ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0					ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30					ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9					µs
			Word	Typ	11					
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7					sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50					µs
	t_{RB}	Recovery Time from RY/BY#		Min	0					ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90					ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



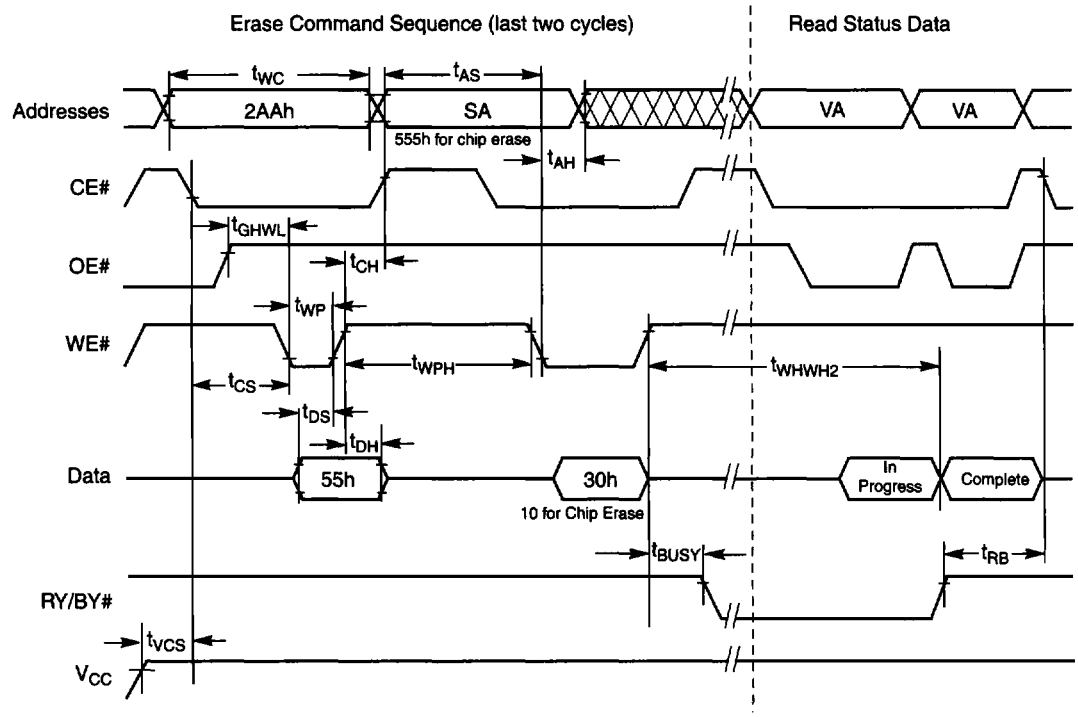
Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

21523C-15

Figure 11. Program Operation Timings

AC CHARACTERISTICS

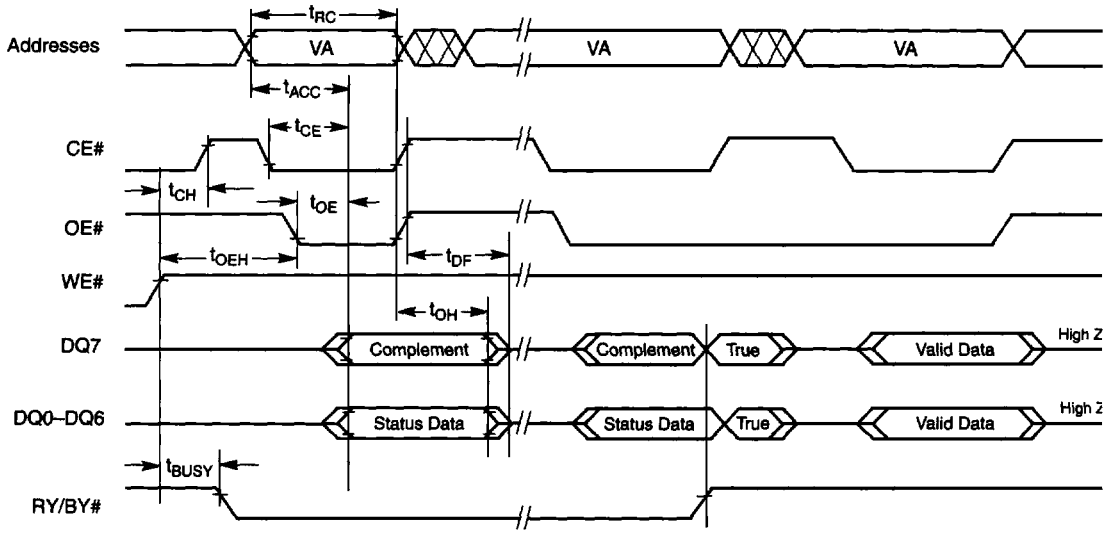


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status" on page 5-373).*
2. *Illustration shows device in word mode.*

21523C-16

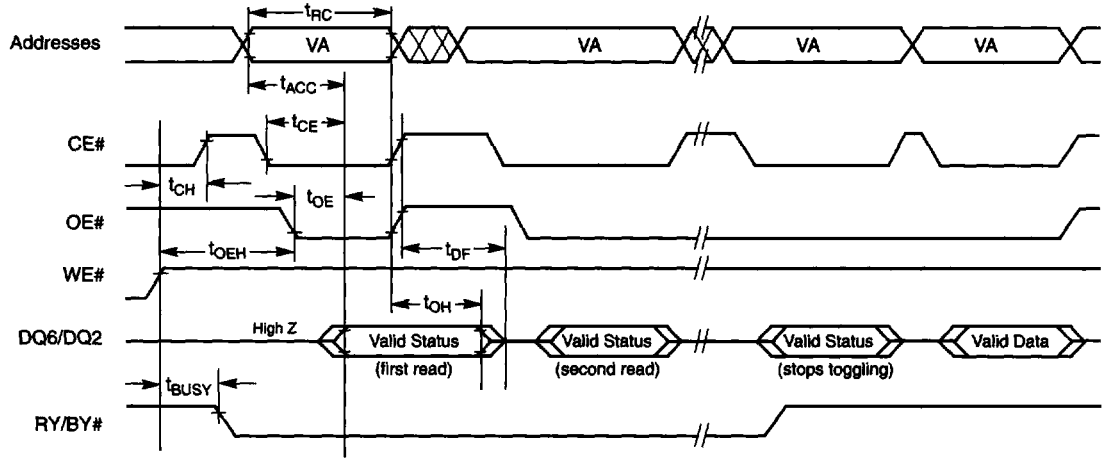
Figure 12. Chip/Sector Erase Operation Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

21523C-17

Figure 13. Data# Polling Timings (During Embedded Algorithms)

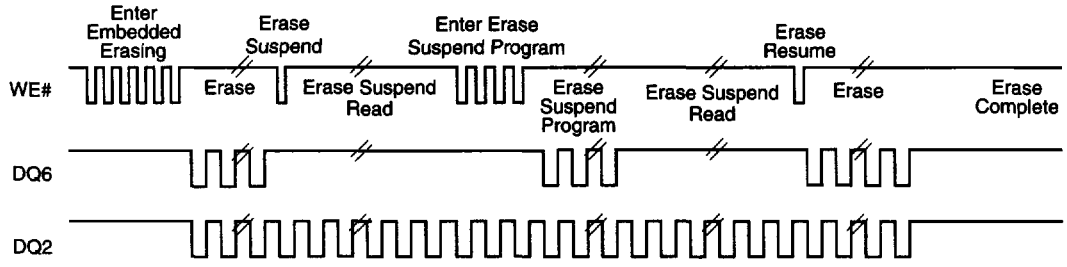


Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

21523C-18

Figure 14. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *The system may use OE# and CE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

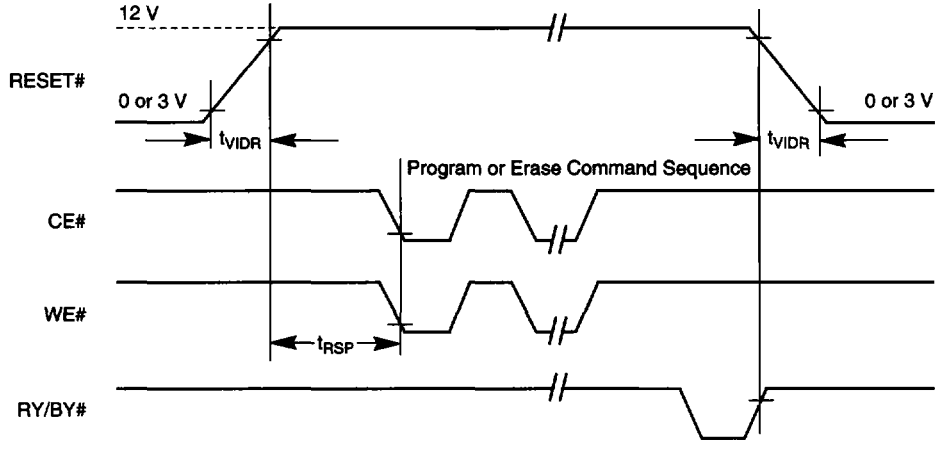
21523C-19

Figure 15. DQ2 vs. DQ6

Temporary Sector Unprotect

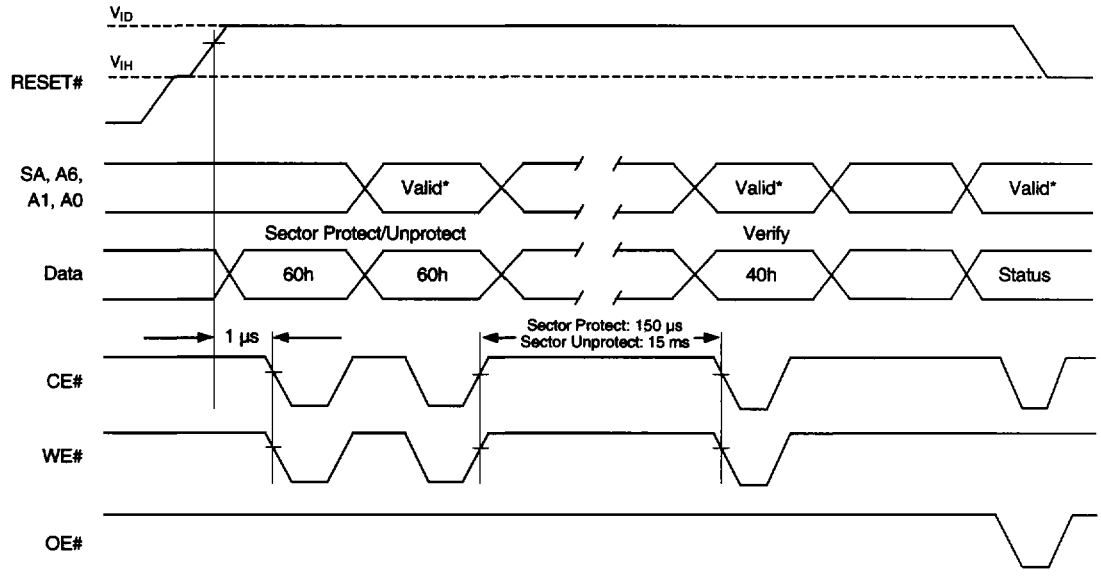
Parameter					
JEDEC	**Std**	**Description**		**All Speed Options**	**Unit**
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*



21523C-20

Figure 16. Temporary Sector Unprotect Timing Diagram



** For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

21523C-21

Figure 17. Sector Protect/Unprotect Timing Diagram

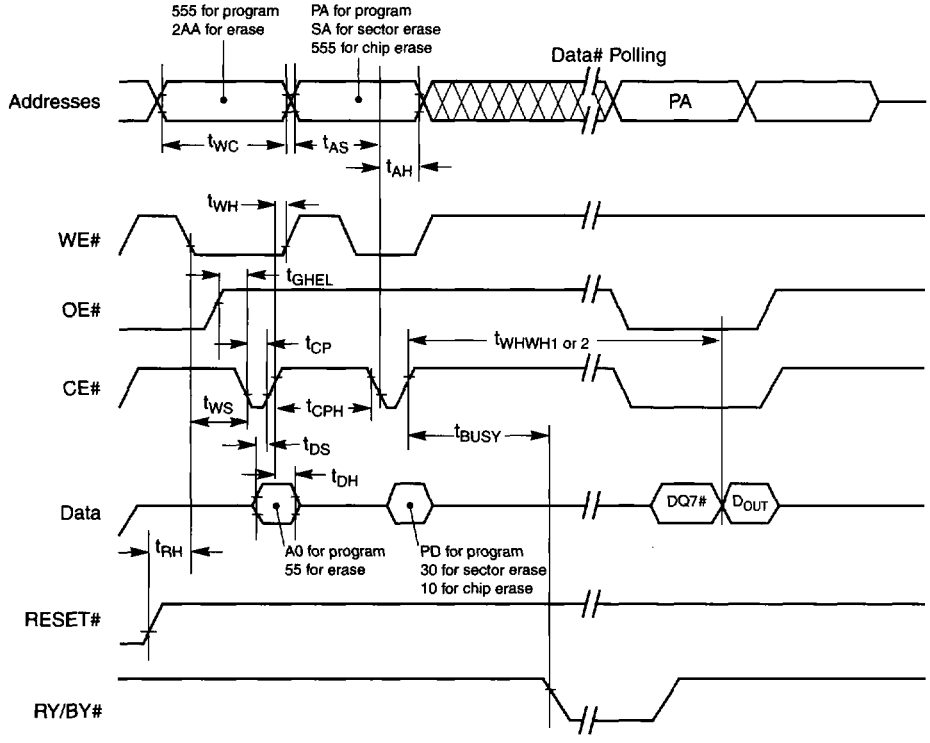
AC CHARACTERISTICS

Alternate CE# Controlled Erase/Program Operations

Parameter					Speed Options					
JEDEC	Std	Description			50R	55R	70	90	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	50	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0					ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0					ns
	t_{OES}	Output Enable Setup Time		Min	0					ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0					ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0					ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0					ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30					ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9					µs
			Word	Typ	11					
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7					sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, DOUT = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

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Figure 18. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		11		s	
Byte Programming Time		9	300	µs	Excludes system level overhead (Note 5)
Word Programming Time		11	360	µs	
Chip Programming Time (Note 3)	Byte Mode	4.5	13.5	s	
	Word Mode	2.9	8.7	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V (3.0 V for regulated speed options), 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP AND SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

REVISION SUMMARY

Revision B

Expanded data sheet from Advanced Information to Preliminary version.

Distinctive Characteristics

Changed "Manufactured on 0.35 µm process technology" to "Manufactured on 0.32 µm process technology".

General Description

Second paragraph: Changed "This device is manufactured using AMD's 0.35 µm process technology" to "This device is manufactured using AMD's 0.32 µm process technology".

Revision B+1

Global

Added the 55 ns speed option.

Connection Diagrams

Corrected the orientation identifiers on the reverse TSOP package. Changed the FBGA drawing to top view, balls facing down.

Revision C

Global

Added -50R speed option.

Ordering Information

Valid Combinations: Deleted the Am29LV400BT80 and Am29LV400BB80 entries.

Erase and Programming Performance

Note 2: Changed "(3.0 V for 55R)' to "(3.0 V for regulated speed options)".