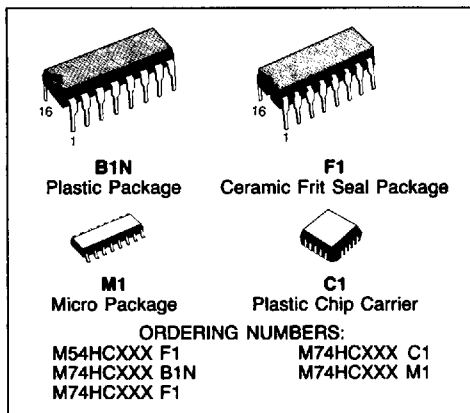



M54HC367/368
M74HC367/368

S G S-THOMSON

HEX BUS BUFFER (3-STATE)
HC367 NON-INVERTING, HC368 INVERTING

- HIGH SPEED
 $t_{PD} = 13 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$ 6V
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- OUTPUT DRIVE CAPABILITY
15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 6 \text{ mA}$ (MIN.)
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
WITH 54/74LS367/368



DESCRIPTION

The M54/74HC367 and the M54/74HC368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate CMOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\bar{G}1$) and the other two buffers are controlled by the other enable input ($\bar{G}2$); the outputs of each buffer group are enabled when $\bar{G}1$ and/or $\bar{G}2$ inputs are held low, and when held high these outputs are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).

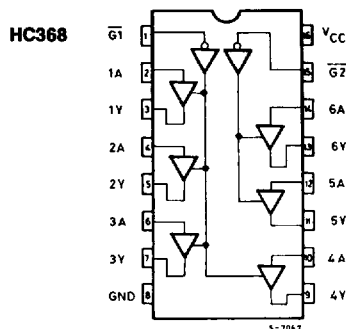
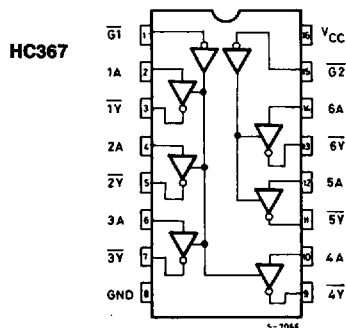
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS		OUTPUTS	
\bar{G}	A_n	Y_n (367)	\bar{Y}_n (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

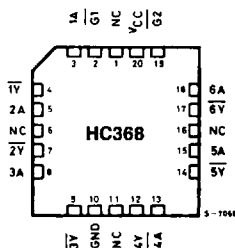
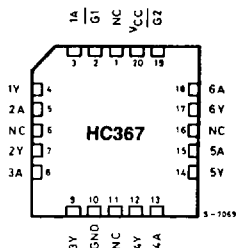
X: DON'T CARE Z: HIGH IMPEDANCE

PIN CONNECTIONS (top view)



CHIP CARRIER

S G S-THOMSON



NC = No internal Connection

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

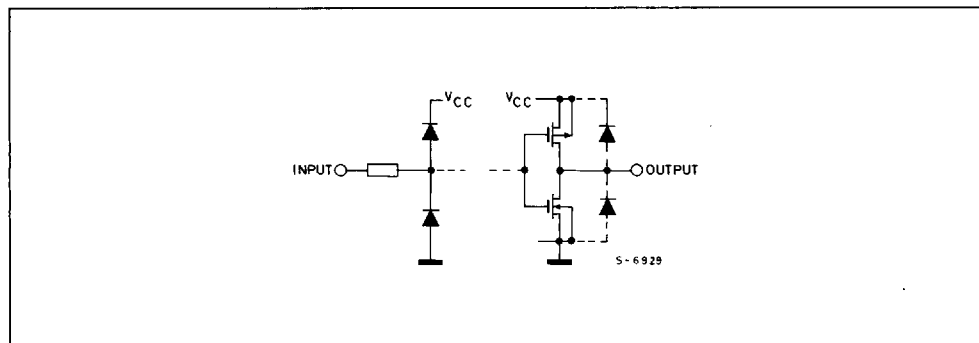
Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _A	Operating Temperature	74HC Series 54HC Series	-40 to 85 -55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

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Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V	
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V	
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	-20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0		-6.0 mA -7.8 mA	5.9	6.0	—	5.9	—	5.9	—	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5		6.0 mA	—	0.0	0.1	—	0.1	—	0.1	
		6.0		7.8 mA	—	0.0	0.1	—	0.1	—	0.1	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	±0.1	—	±1.0	—	±1.0	μA	
I _{OZ}	3-State Output Off-State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND	—	—	±0.5	—	±5.0	—	±10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND I _O = 0	—	—	4	—	40	—	80	μA	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

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Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	22 8 7	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t_{PLH} t_{PHL}	Propagation Delay Time *	2.0 4.5 6.0		— — —	60 15 13	120 24 20	— — —	150 30 26	— — —	180 36 31	
t_{PLH} t_{PHL}	Propagation Delay Time **	2.0 4.5 6.0		— — —	56 14 12	115 23 20	— — —	145 29 25	— — —	175 35 30	
t_{PZL} t_{PZH}	Output Enable Time	2.0 4.5 6.0	$R_L = 1\text{K}\Omega$	— — —	60 15 13	120 24 20	— — —	150 30 26	— — —	180 36 31	ns
t_{PLZ} t_{PHZ}	Output Disable Time	2.0 4.5 6.0	$R_L = 1\text{K}\Omega$	— — —	63 20 18	150 30 26	— — —	190 38 33	— — —	225 45 38	
C_{IN}	Input Capacitance	—		—	5	10	—	10	—	10	
C_{OUT}	Output Capacitance	—		—	10	—	—	—	—	—	pF
C_{PD} (1)	Power Dissipation	—	HC 367	—	34	—	—	—	—	—	pF
	Capacitance	—	HC 368	—	32	—	—	—	—	—	

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

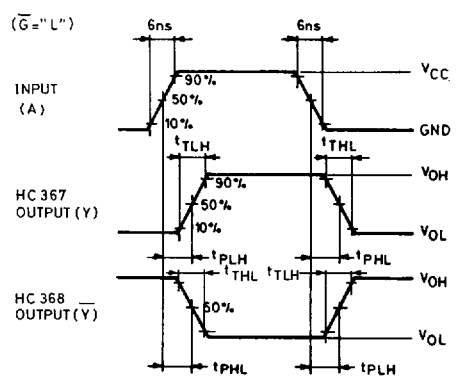
Average operating current can be obtained by the following equation.

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per circuit).}$$

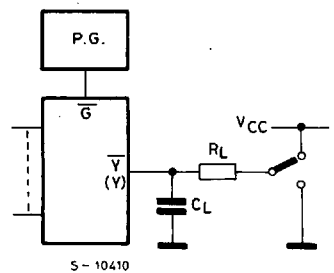
* For M54/74HC367 only

** For M54/74HC368 only

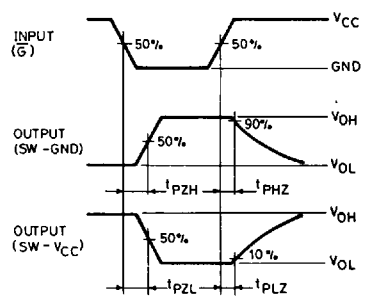
SWITCHING CHARACTERISTICS TEST WAVEFORM S G S-THOMSON



S-10409



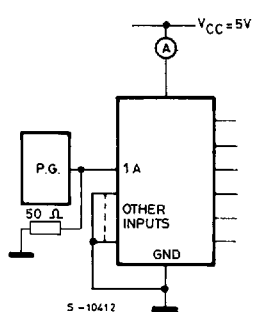
S-10410



S-10411

NOTE: SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL, WHEN THE OUTPUT IS ENABLE

TEST CIRCUIT I_{CC} (Opr.)



S-10412

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC} (Opr.)}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.