T54LS76A
T74LS76A

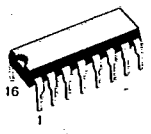
LOW POWER SCHOTTKY INTEGRATED CIRCUITS

PRELIMINARY DATA

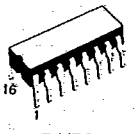
DUAL JK FLIP-FLOP WITH SET AND CLEAR

DESCRIPTION

The T54LS/T74LS76A dual flip-flops feature separate J, K, Clock Pulse, Direct Set and Direct Clear inputs.
Inputs are enabled and data is accepted when the clock goes HIGH.
The Logic levels of the J and K inputs correspond to the Truth Table if the minimum set-up times are observed. During the HIGH-to-LOW clock transition input data is transferred to the outputs.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

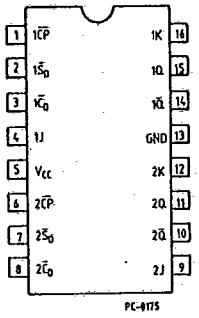
C1
Plastic Chip Carrier

ORDERING NUMBERS:

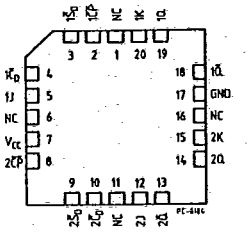
T54LS76A D2
T74LS76A D1
T74LS76A B1
T74LS76A C1
T74LS76A M1

PIN CONNECTION (top view)

DUAL IN LINE

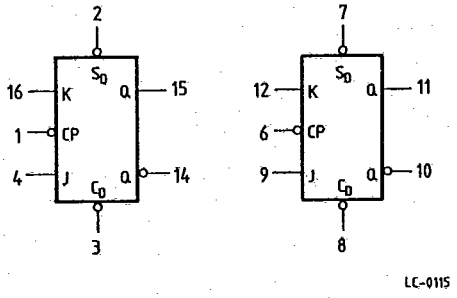


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL

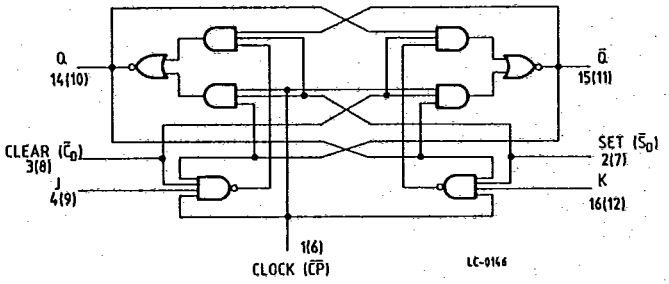


LOGIC DIAGRAM AND MODE SELECT TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	$\overline{q}$
Hold	H	H	l	l	q	$\overline{q}$

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go to HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't care
l,h,(q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.



V_{CC} = Pin 5
GND = Pin 13
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS76AD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS76AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current	J, K			20	V_{CC} = MAX, V_{IN} = 2.7V	μA
		Clear			60		
		Clock			80		
		J, K			0.1	V_{CC} = MAX, V_{IN} = 7.0V	mA
		Clear			0.3		
		Clock			0.4		
I_{IL}	Input LOW Current	J, K			−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
		Clear, Clock			−0.8		
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX	mA
I_{CC}	Power Supply Current				6.0	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
f_{MAX}	Maximum Clock Frequency	30	45		V_{CC} = 5.0V	MHz
t_{PLH}	Clock, Clear, Set to Output		15	20		ns
t_{PHL}			15	20		

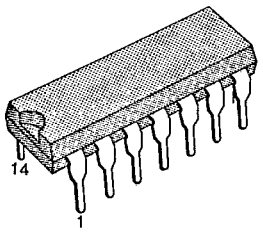
AC SET-UP REQUIREMENTS: T_A = 25°C

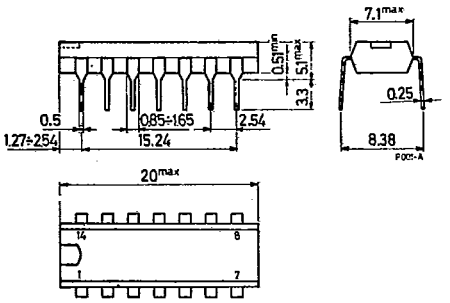
Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
t_W	Clock Pulse Width	20			V_{CC} = 5.0V	ns
t_W	Clear Set Pulse Width	25				ns
t_s	Set-up Time	20				ns
t_h	Hold Time	0				ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

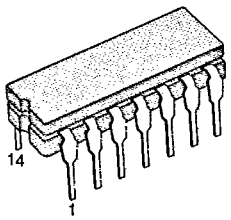
Packages

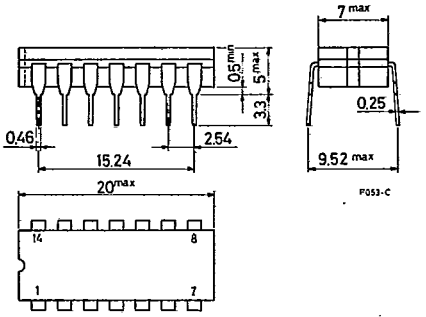
14-LEAD PLASTIC DIP



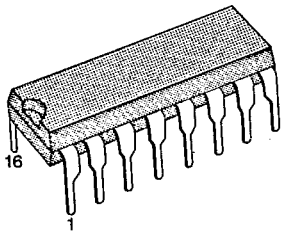


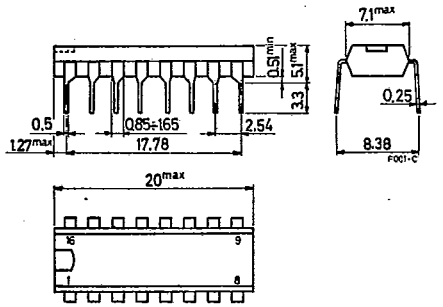
14-LEAD CERAMIC DIP





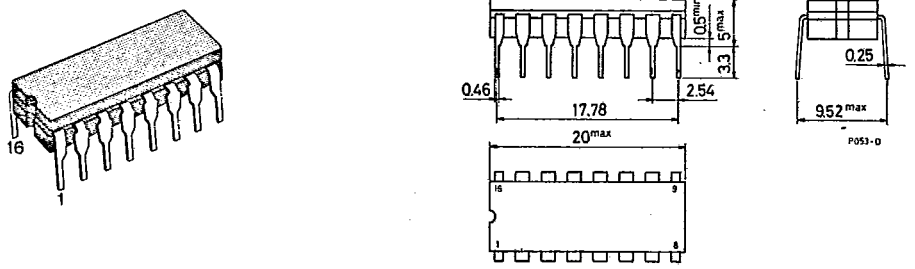
16-LEAD PLASTIC DIP





Packages

16-LEAD CERAMIC DIP



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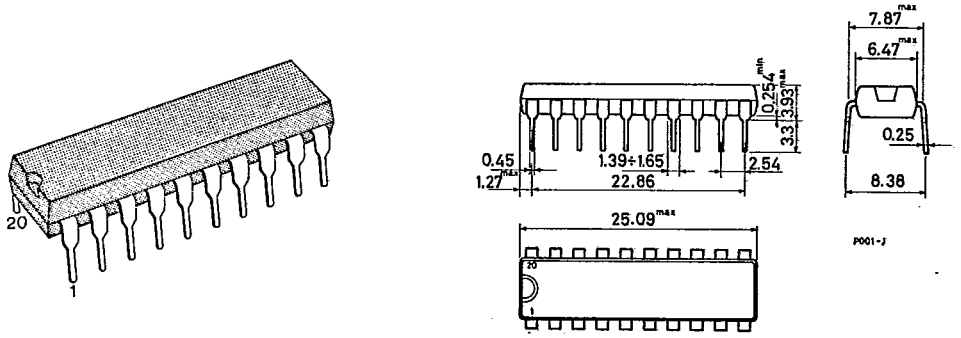

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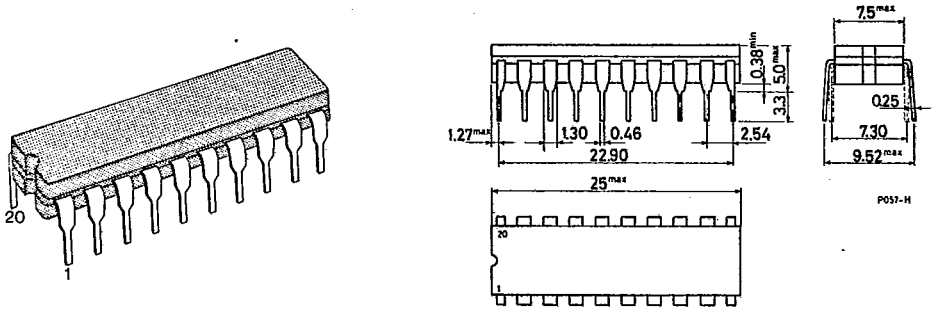
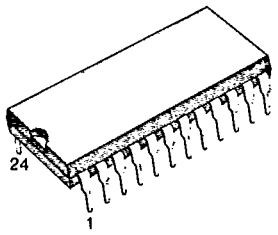
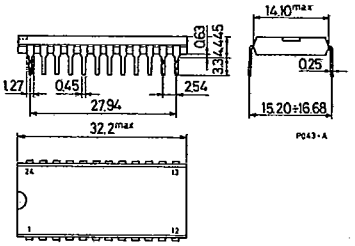


Packages

24-LEAD PLASTIC DIP





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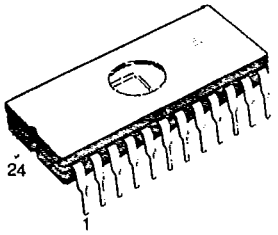
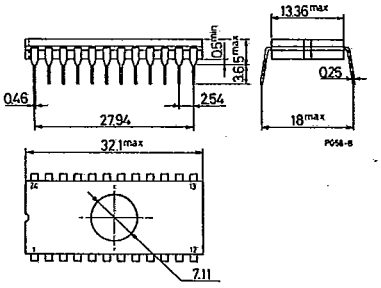
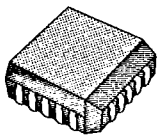
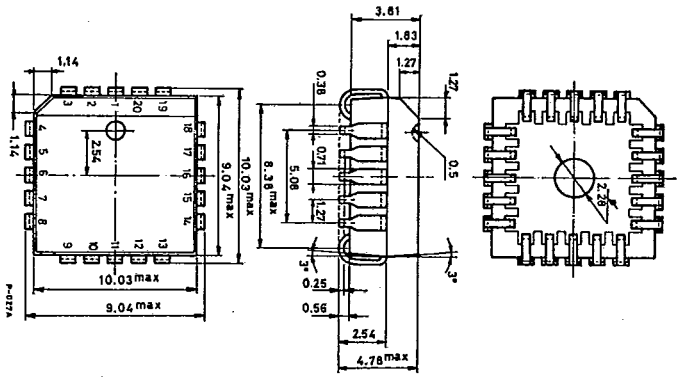




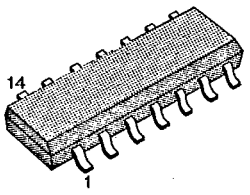
CHIP CARRIER 20 LEAD PLASTIC

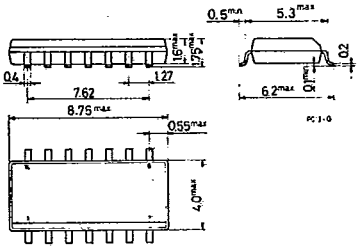




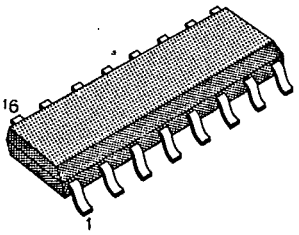
Packages

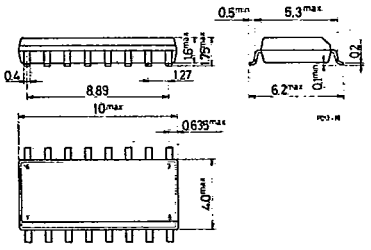
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.