

# 74ACT11646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS061A – D2957, JULY 1987 – REVISED APRIL 1993

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

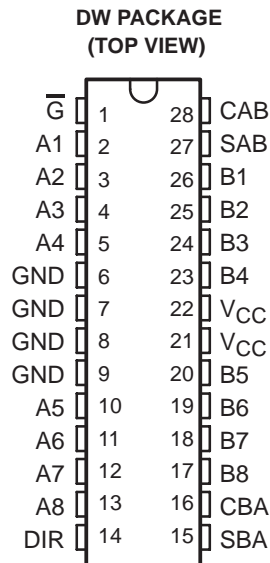
## description

These devices consist of bus transceiver circuits, 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ( $\overline{G}$ ) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable  $\overline{G}$  is active (low). In the isolation mode (control  $\overline{G}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74ACT11646 is characterized for operation from – 40°C to 85°C.



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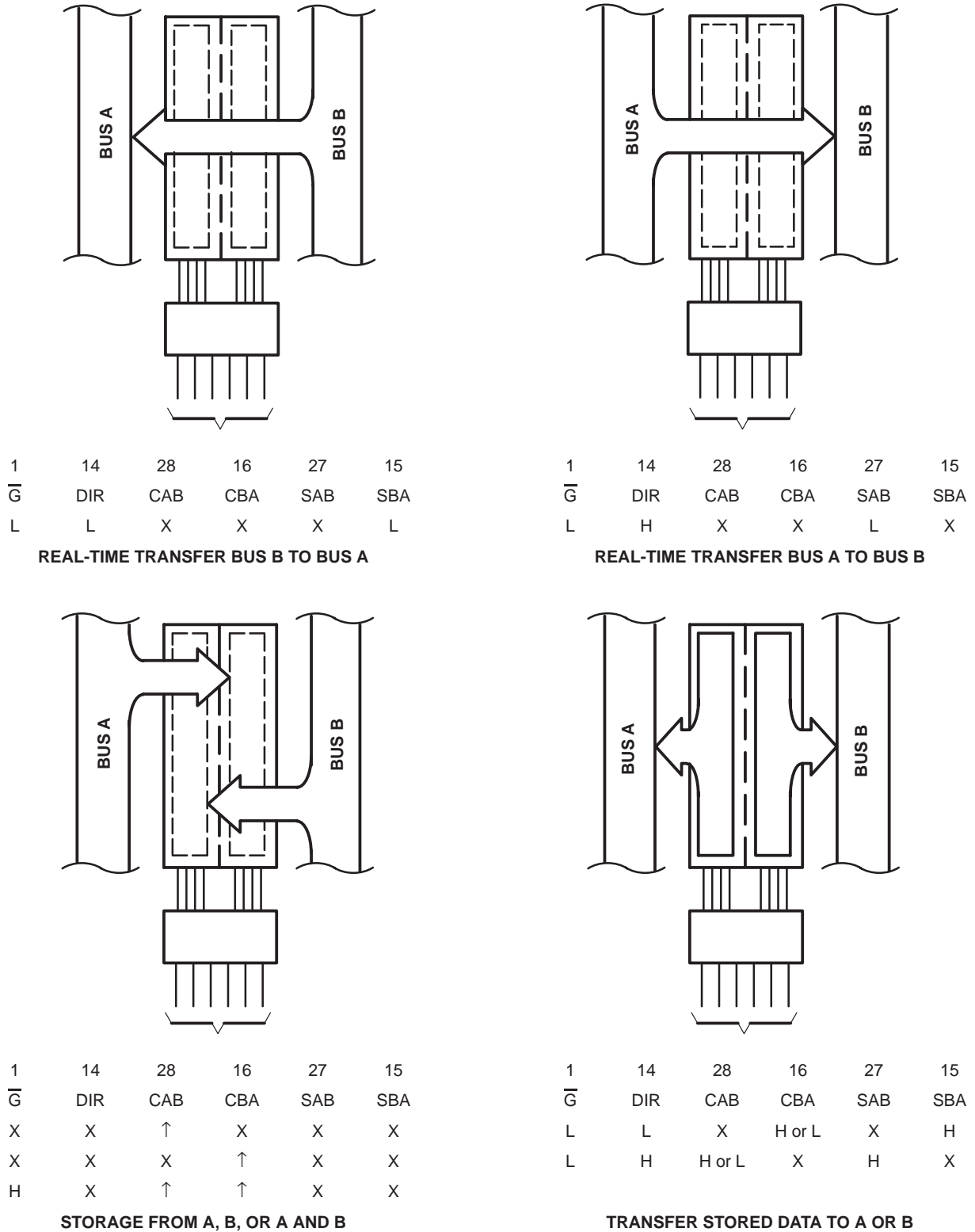


Figure 1. Bus-Management Functions

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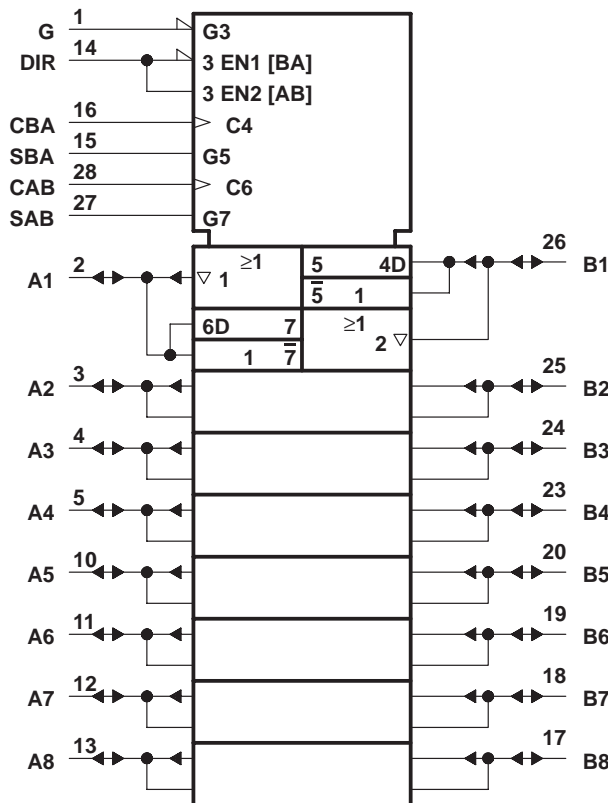
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FUNCTION TABLE

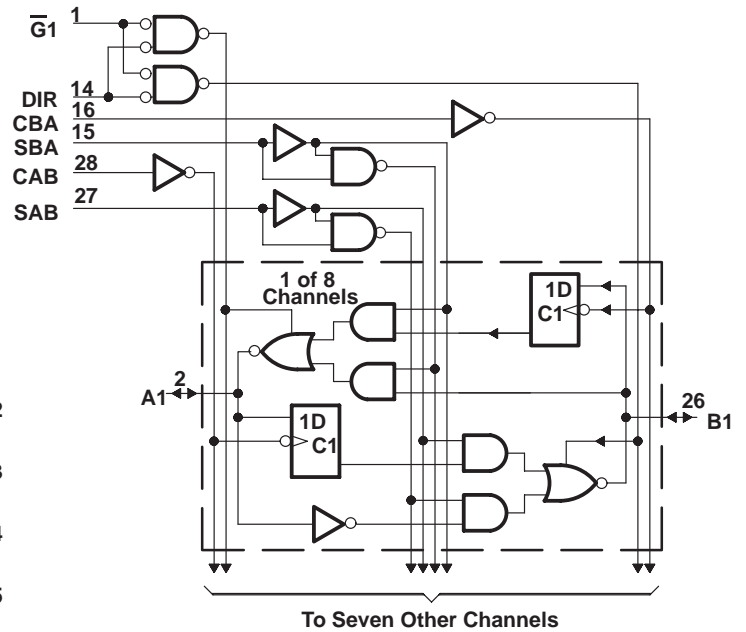
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified† Store B, A unspecified†
X	X	X	↑	X	X	Unspecified†	Input	
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation, hold storage
H	X	H or L	H or L	X	X			
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
L	L	X	H or L	X	H			
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
L	H	H or L	X	H	X			

† The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

### logic symbol‡



### functional block diagram (positive logic)



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# 74ACT11646

## OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 200$ mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4		4.4		V	
		5.5 V	5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	$I_{OH} = -75 \text{ mA}^\ddagger$	5.5 V			3.85			
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1	V	
		5.5 V			0.1	0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V				1.65		
$I_{OZ}$	A or B ports $^\S$	$V_O = V_{CC}$ or GND	5.5 V		$\pm 0.5$	$\pm 5$	$\mu\text{A}$	
$I_I$	$\overline{G}$ or DIR	$V_I = V_{CC}$ or GND	5.5 V		$\pm 0.1$	$\pm 1$	$\mu\text{A}$	
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		8	80	$\mu\text{A}$	
$\Delta I_{CC}^\parallel$		One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V		0.9	1	mA	
$C_i$		$V_I = V_{CC}$ or GND	5 V		4.5		pF	
$C_o$		$V_O = V_{CC}$ or GND	5 V		12		pF	

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ For I/O ports, the parameter  $I_{OZ}$  includes the leakage current.

¶ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f <sub>clock</sub>	Clock frequency	0	105	0	105	MHz
t <sub>w</sub>	Pulse duration, CAB or CBA high or low	4.8		4.8		ns
t <sub>su</sub>	Setup time, A before CLK↑ or B before CBA↑	4.5		4.5		ns
t <sub>h</sub>	Hold time, A after CAB↑ or B after CBA↑	2.5		2.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			105			105		MHz
t <sub>PLH</sub>	A or B	B or A	1.5	7.3	10.1	1.5	11.5	ns
t <sub>PHL</sub>			1.5	7.2	11	1.5	12	
t <sub>PZH</sub>	$\bar{G}$	A or B	1.5	7.7	12.8	1.5	14.4	ns
t <sub>PZL</sub>			1.5	9.2	13.8	1.5	15.3	
t <sub>PHZ</sub>	$\bar{G}$	A or B	1.5	8.6	10.7	1.5	11.6	ns
t <sub>PLZ</sub>			1.5	7.8	9.7	1.5	10.6	
t <sub>PLH</sub>	CBA or CAB	A or B	1.5	8.8	11.9	1.5	13.5	ns
t <sub>PHL</sub>			1.5	10	13.4	1.5	14.9	
t <sub>PZH</sub>	DIR	A or B	1.5	10.2	13.7	1.5	15.3	ns
t <sub>PZL</sub>			1.5	10.9	14.8	1.5	16.5	
t <sub>PHZ</sub>	DIR	A or B	1.5	7.9	10.5	1.5	11.3	ns
t <sub>PLZ</sub>			1.5	7.3	9.5	1.5	10.3	
t <sub>PLH</sub>	SBA or SAB (A or B high)	A or B	1.5	6.7	10.3	1.5	11.5	ns
t <sub>PHL</sub>			1.5	9.1	12.1	1.5	13.5	
t <sub>PLH</sub>	SBA or SAB (A or B low)	A or B	1.5	8	10.9	1.5	12.4	ns
t <sub>PHL</sub>			1.5	8.1	11.9	1.5	13.1	

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

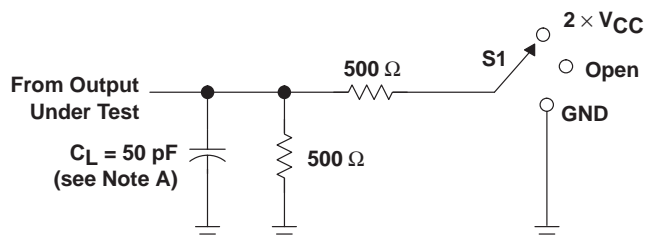
PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	C <sub>L</sub> = 50 pF, f = 1 MHz	63	pF
			14	



# 74ACT11646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

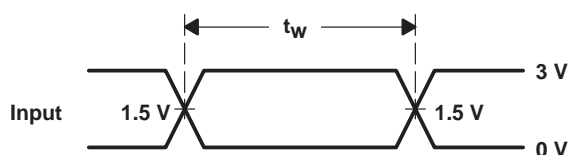
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## PARAMETER MEASUREMENT INFORMATION

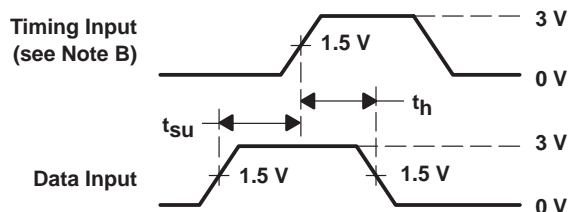


LOAD CIRCUIT

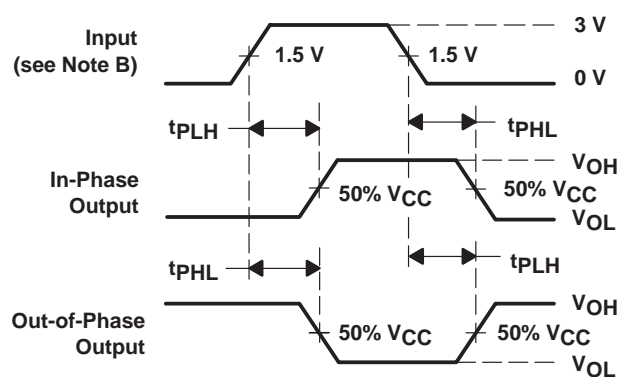
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



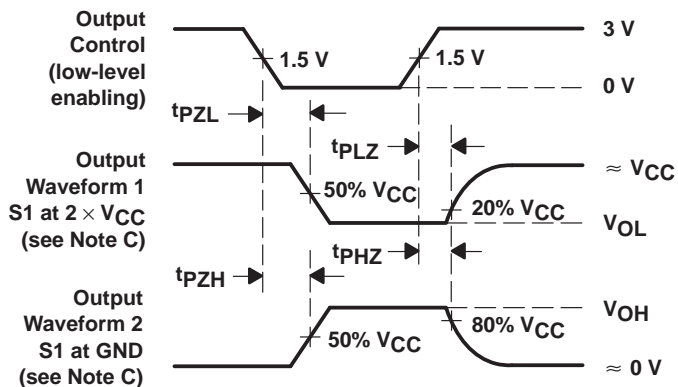
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT11646DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
74ACT11646DWR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
74ACT11646NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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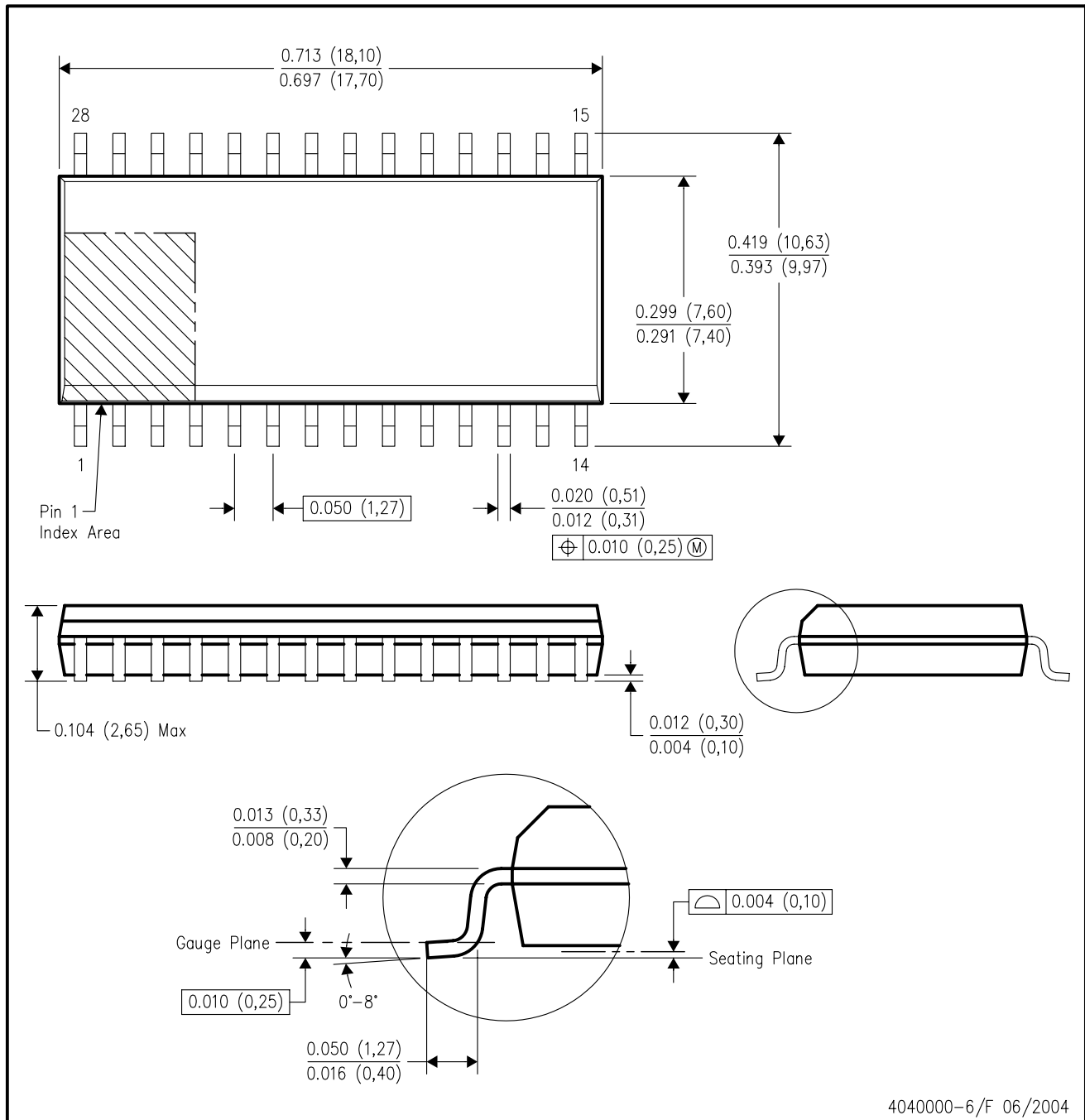
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE



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- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AE.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
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74ACT11646DWR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
74ACT11646NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI

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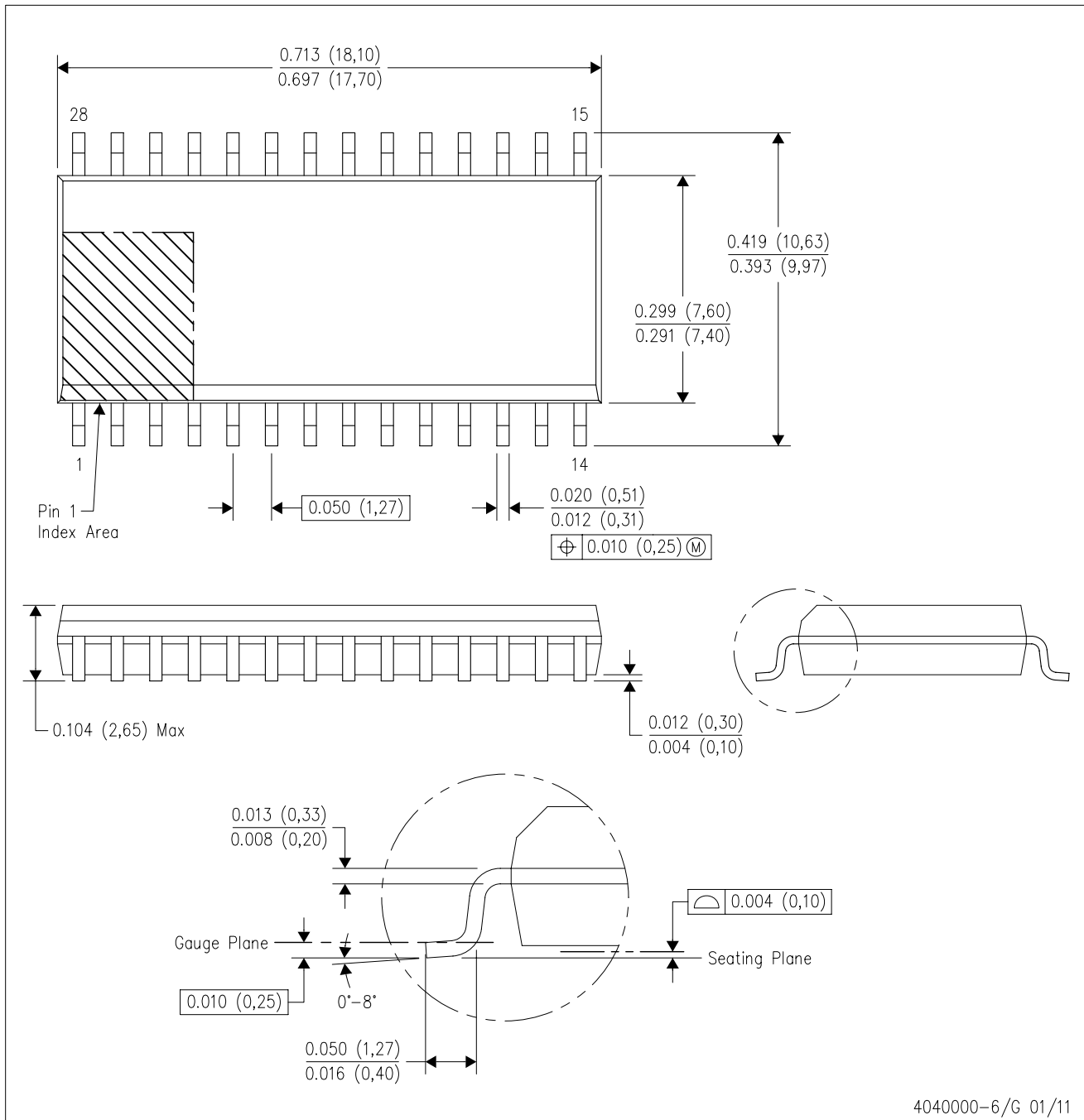
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DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



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Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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