

4 Megabit 3.3V Static RAM 512K x 8-Bit

Features

- High-speed access times
Com'l: 8, 10, 12, 15, and 20 ns
Ind'l.: 12, 15 and 20 ns
- Low power operation
- PDM31096SA
Active: 300 mA (Max)
Standby: 25mW
- Single +3.3V ($\pm 0.3V$) power supply
- TTL-compatible inputs and outputs
- Packages
Plastic SOJ (400 mil) - SO
Plastic TSOP (II) - T

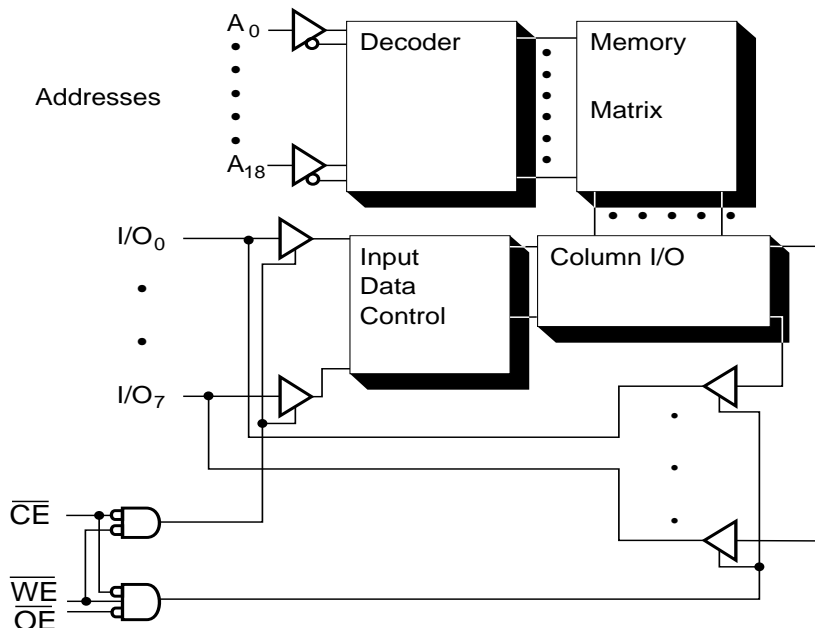
Description

The PDM31096 is a high-performance CMOS static RAM organized as 524,288 x 8 bits. Writing is accomplished when the write enable (\overline{WE}) and chip enable \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} and \overline{OE} are both LOW.

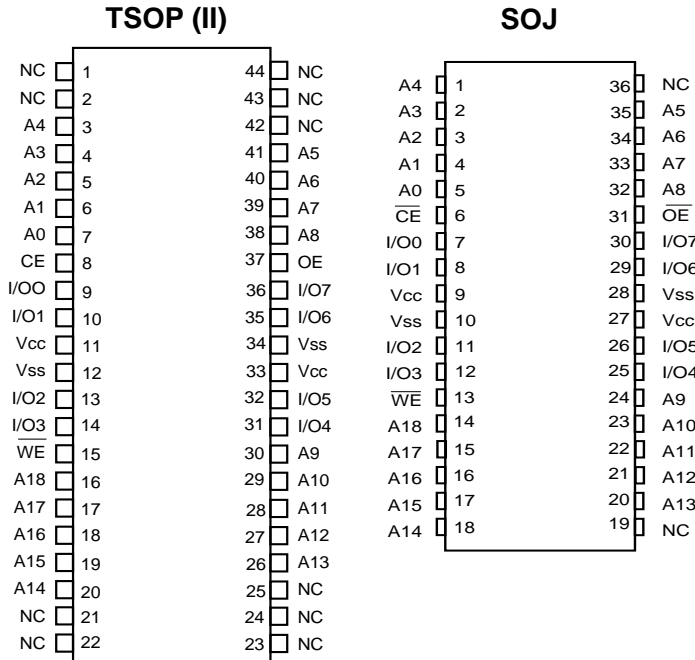
The PDM31096 operates from a single +3.3V power supply and all the inputs and outputs are fully TTL-compatible.

The PDM31096 is available in a 36-pin 400-mil plastic SOJ package and a 44-pin plastic TSOP (II) package.

Functional Block Diagram



Pin Configuration



Pin Description

Name	Description
A18-A0	Address Inputs
I/O7-I/O0	Data Inputs/Outputs
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
\overline{CE}	Chip Enable Inputs
NC	No Connect
V _{CC}	Power (+3.3V)
V _{SS}	Ground

Truth Table⁽¹⁾

\overline{OE}	\overline{WE}	\overline{CE}	I/O	MODE
X	X	H	Hi-Z	Standby
X	X	X	Hi-Z	Standby
L	H	L	D _{OUT}	Read
X	L	L	D _{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings ⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect to V _{SS}	-0.5 to +4.6	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA
T _j	Maximum Junction Temperature ⁽²⁾	125	145	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: $T_j = T_a + P * \theta_{ja}$ where T_a is the ambient temperature, P is average operating power and θ_{ja} the thermal resistance of the package. For this product, use the following θ_{ja} value:

SOJ: 59° C/W
 TSOP : TBD

DC Electrical Characteristics ($V_{CC} = 3.3V \pm 0.3V$)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = V_{SS} \text{ to } V_{CC}$	-5	5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.},$ $\overline{CE} = V_{IH}$ $V_{OUT} = V_{SS} \text{ to } V_{CC}$	-5	5	μA
V_{IL}	Input Low Voltage		-0.3 ⁽¹⁾	0.8	V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$	2.4	—	V

NOTE: 1. $V_{IL}(\text{min}) = -3.0V$ for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter	-8	-10	-12		-15		-20		Unit
		Com'l.	Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{CC}	Operating Current $\overline{CE} = V_{IL}$ $f = f_{MAX} = 1/t_{RC}$ $V_{CC} = \text{Max.}$ $I_{OUT} = 0 \text{ mA}$	230	215	200	220	160	200	120	160	mA
I_{SB}	Standby Current $\overline{CE} = V_{IH}$ $f = f_{MAX} = 1/t_{RC}$ $V_{CC} = \text{Max.}$	50	45	40	45	35	40	30	35	mA
I_{SB1}	Full Standby Current $\overline{CE} \geq V_{CC} - 0.2V$ $f = 0$ $V_{CC} = \text{Max.},$ $V_{IN} \geq V_{CC} - 0.2V \text{ or } \leq 0.2V$	10	10	10	15	10	15	10	15	mA

NOTES: All values are maximum guaranteed values.

Capacitance⁽¹⁾ ($T_A = +25^\circ C, f = 1.0 \text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	-0	25	70	°C

AC Test Conditions

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	2.5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

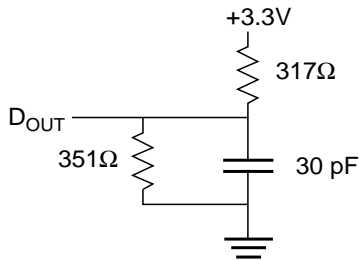


Figure 1. Output Load Equivalent

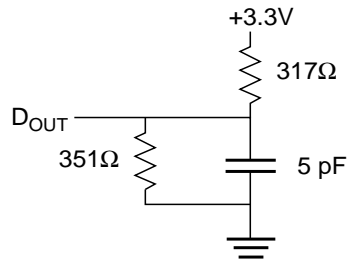
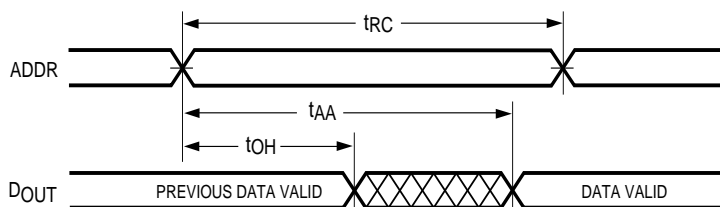
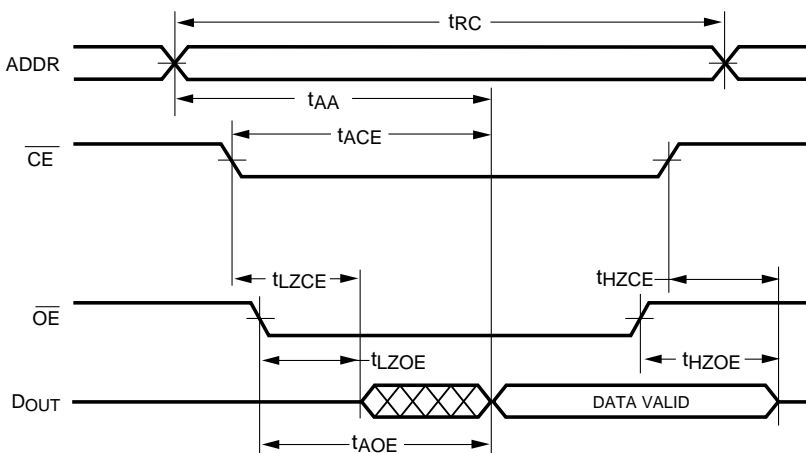


Figure 2. Output Load Equivalent
(for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

Read Cycle No. 1^(4, 5)



Read Cycle No. 2^(2, 4, 6)

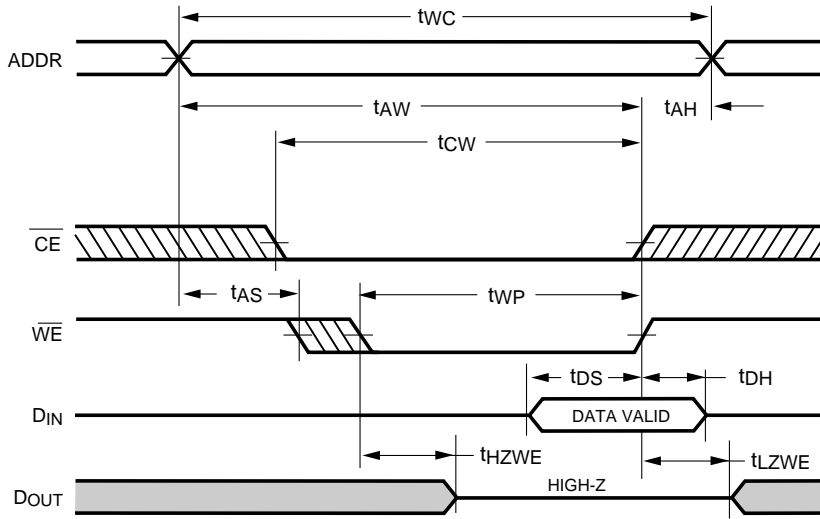


AC Electrical Characteristics

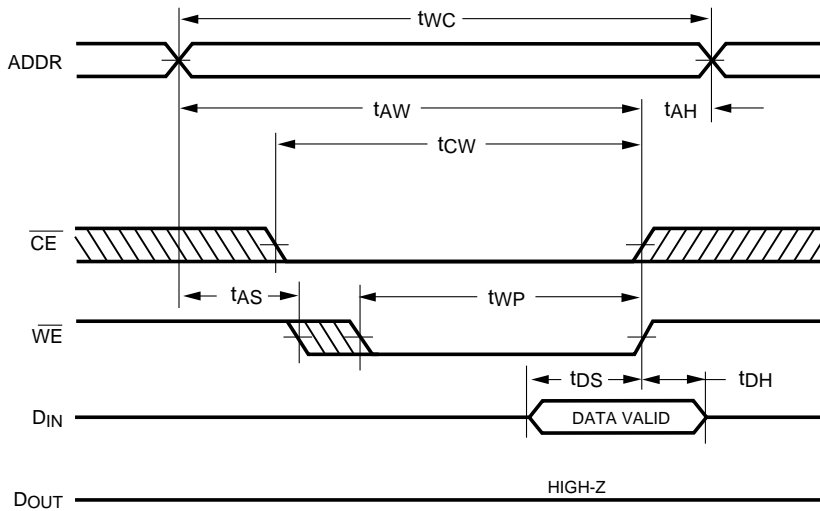
Description	Sym	-8*		-10*		-12		-15		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
READ Cycle	t_{RC}	8	—	10	—	12	—	15	—	20	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	—	15	—	20	ns
Chip enable access time	t_{ACE}	—	8	—	10	—	12	—	15	—	20	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ^(1,3)	t_{LZCE}	3	—	3	—	3	—	3	—	3	—	ns
Chip disable to output in high Z ^(1,2,3)	t_{HZCE}	—	4	—	5	—	6	—	7	—	7	ns
Output enable access time	t_{AOE}	—	4	—	5	—	6	—	7	—	8	ns
Output Enable to output in low Z ^(1,3)	t_{LZOE}	0	—	0	—	0	—	0	—	0	—	ns
Output disable to output in high Z ^(1,3)	t_{HZOE}	—	4	—	4	—	5	—	6	—	7	ns

* $V_{CC} = 3.3V \pm 5\%$

Write Cycle No. 1 (Write Enable Controlled)

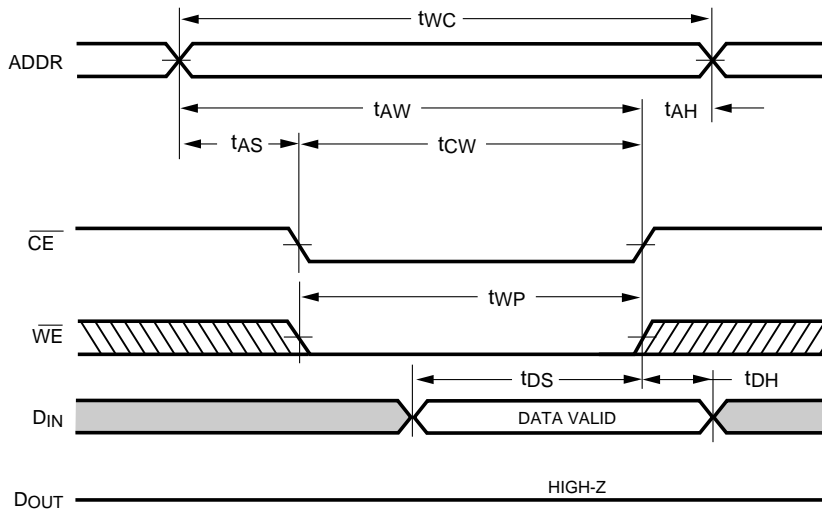


Write Cycle No. 2 (Write Enable Controlled)



NOTE: Output Enable (\overline{OE}) is inactive (high)

Write Cycle No. 3 (Chip Enable Controlled)



NOTE: Output Enable (\overline{OE}) is inactive (high)

AC Electrical Characteristics

Description	Sym	-8*		-10*		-12		-15		-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE Cycle												
WRITE cycle time	t_{WC}	8	—	10	—	12	—	15	—	20	—	ns
Chip enable to end of write	t_{CW}	8	—	10	—	10	—	11	—	13	—	ns
Address valid to end of write	t_{AW}	8	—	10	—	10	—	11	—	13	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	7	—	8	—	8	—	9	—	10	—	ns
Data setup time	t_{DS}	5	—	6	—	7	—	8	—	9	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns
Write disable to output in low $Z^{(1,3)}$	t_{LZWE}	0	—	0	—	0	—	0	—	0	—	ns
Write enable to output in high $Z^{(1,3)}$	t_{HZWE}	—	4	—	5	—	6	—	7	—	9	ns

* $V_{CC} = 3.3V \pm 5\%$

NOTES: (For two previous Electrical Characteristics tables)

1. The parameter is tested with $CL = 5\text{ pF}$ as shown in Figure 2. Transition is measured $\pm 200\text{ mV}$ from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .
3. This parameter is sampled.
4. \overline{WE} is high for a READ cycle.
5. The device is continuously selected. All the Chip Enables are held in their active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.

Ordering Information

