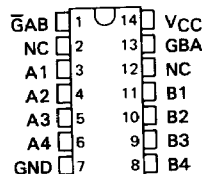


# TYPES SN54ALS1242, SN54ALS1243, SN74ALS1242, SN74ALS1243 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- 2-Way Asynchronous Communication between Data Buses
- P-N-P Inputs Reduce DC Loading
- Low-Power Version of 'ALS242, and 'ALS243
- Three-State Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1242, SN54ALS1243 . . . J PACKAGE  
SN74ALS1242, SN74ALS1243 . . . N PACKAGE  
(TOP VIEW)



### description

These quadruple bus transceivers are designed for two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and  $\overline{\text{GAB}}$ ).

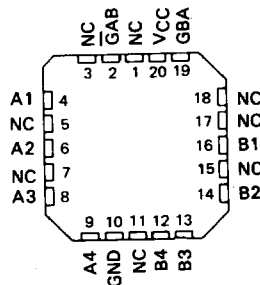
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1242 and 'ALS1243 the capability to store data by simultaneous enabling of  $\overline{\text{GAB}}$  and GBA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will remain at their last states. The 4-bit codes appearing on the two sets of buses will be complementary for the 'ALS1242 or identical for the 'ALS1243.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum  $I_{OL}$  is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1242 and SN54ALS1243 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS1242 and SN74ALS1243 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS1242, SN54ALS1243 . . . FH PACKAGE  
SN74ALS1242, SN74ALS1243 . . . FN PACKAGE  
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE

$\overline{\text{GAB}}$	GBA	'ALS1242	'ALS1243
L	L	$\overline{\text{A}}$ to B	A to B
H	H	$\overline{\text{B}}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B (A = B)	Latch A and B (A = B)

2

ALS AND AS CIRCUITS

### PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

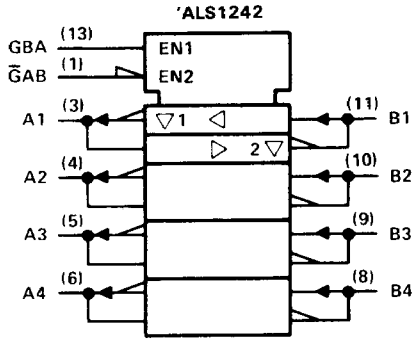
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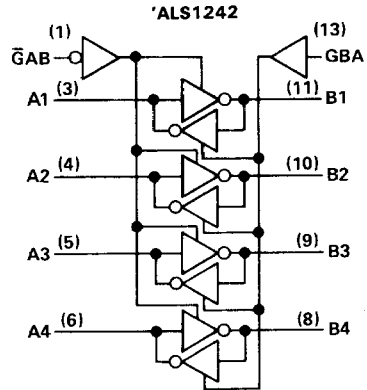
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**TYPES SN54ALS1242, SN54ALS1243,  
SN74ALS1242, SN74ALS1243  
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

logic symbols

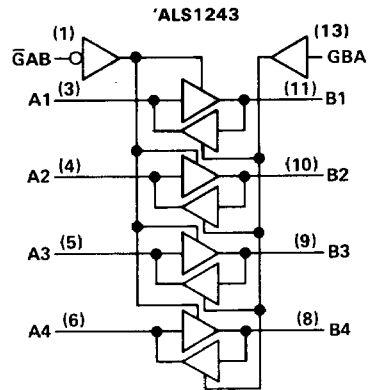
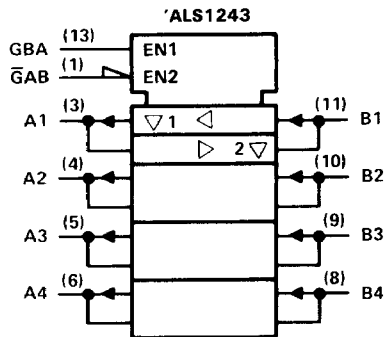


logic diagrams (positive logic)



**2**

**ALS AND AS CIRCUITS**



Pin numbers shown are for J and N packages.



**TYPES SN54ALS1242, SN54ALS1243,  
SN74ALS1242, SN74ALS1243  
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

'ALS1242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX						UNIT
			SN54ALS1242			SN74ALS1242			
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
t <sub>PLH</sub>	A or B	B or A	9			9			ns
t <sub>PHL</sub>			9			9			
t <sub>PZH</sub>	A̅B	B	17			17			ns
t <sub>PZL</sub>			19			19			
t <sub>PHZ</sub>	A̅B	B	7			7			ns
t <sub>PLZ</sub>			6			6			
t <sub>PZH</sub>	GBA	A	17			17			ns
t <sub>PZL</sub>			19			19			
t <sub>PHZ</sub>	GBA	A	7			7			ns
t <sub>PLZ</sub>			6			6			

'ALS1242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX						UNIT
			SN54ALS1243			SN74ALS1243			
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
t <sub>PLH</sub>	A or B	B or A	11			11			ns
t <sub>PHL</sub>			11			11			
t <sub>PZH</sub>	A̅B	B	19			19			ns
t <sub>PZL</sub>			21			21			
t <sub>PHZ</sub>	A̅B	B	9			9			ns
t <sub>PLZ</sub>			8			8			
t <sub>PZH</sub>	GBA	A	19			19			ns
t <sub>PZL</sub>			21			21			
t <sub>PHZ</sub>	GBA	A	9			9			ns
t <sub>PLZ</sub>			8			8			

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

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ALS AND AS CIRCUITS

Additional information on these products can be obtained from the factory as it becomes available.

**PRODUCT PREVIEW**

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