

FEATURES

- ❑ 2K x 8 Static RAM with Chip Select Powerdown, Output Enable
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 10 ns maximum
- ❑ Low Power Operation
 - Active:
 - 250 mW typical at 35 ns
 - Standby (typical):
 - 100 μW (L6116)
 - 50 μW (L6116-Low Power)
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ DESC SMD Drawing No.
 - 5962-84036 — L6116
 - 5962-89690 — L6116
 - 5962-88740 — L6116-Low Power
- ❑ Plug Compatible with IDT6116, Cypress CY7C128/CY6116
- ❑ Package Styles Available:
 - 24-pin Plastic DIP
 - 24-pin CerDIP
 - 24-pin Plastic SOJ
 - 24-pin CerFlat
 - 28-pin Ceramic LCC
 - 32-pin Ceramic LCC

DESCRIPTION

The L6116 is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 2048 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in six speeds with maximum access times from 10 ns to 35 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L6116 is 250 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) for the L6116 and 60 mW (typical) for the L6116-L when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L6116 and L6116-L consume only 15 μW and 6 μW

(typical) respectively, at 3 V, allowing effective battery backup operation.

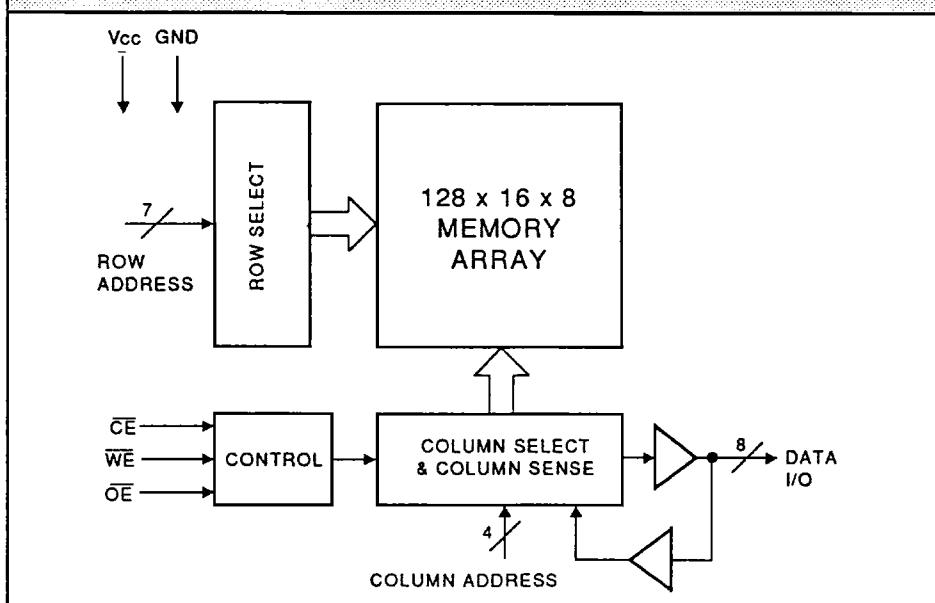
The L6116 provides asynchronous (unlocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A10. Reading from a designated location is accomplished by presenting an address and driving \overline{CE} and \overline{OE} low, while \overline{WE} remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when \overline{CE} or \overline{OE} is high, or \overline{WE} is low.

Writing to an addressed location is accomplished when the active-low \overline{CE} and \overline{WE} inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L6116 can withstand an injection current of up to 200 mA on any pin without damage.

L6116 BLOCK DIAGRAM



L6116

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
Vcc supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ Vcc ≤ 5.5 V
Active Operation, Military	-55°C to +125°C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ Vcc ≤ 5.5 V
Data Retention, Military	-55°C to +125°C	2.0 V ≤ Vcc ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	L6116			L6116-L			Unit
			Min	Typ	Max	Min	Typ	Max	
VOH	Output High Voltage	IOH = -4.0 mA, Vcc = 4.5 V	2.4			2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4			0.4	V
VIH	Input High Voltage		2.2		Vcc + 0.3	2.2		Vcc + 0.3	V
VIL	Input Low Voltage	(Note 3)	-3.0		0.8	-3.0		0.8	V
IIX	Input Leakage Current	GND ≤ VIN ≤ Vcc	-10		+10	-10		+10	μA
IOZ	Output Leakage Current	GND ≤ VOUT ≤ Vcc, CE = Vcc	-10		+10	-10		+10	μA
ICC2	Vcc Current, TTL Inactive	(Note 7)		15	30		12	20	mA
ICC3	Vcc Current, CMOS Standby	(Note 8)		20	100		10	30	μA
ICC4	Vcc Current, Data Retention	Vcc = 3.0 V (Note 9)		5	50		2	10	μA
CIN	Input Capacitance	Ambient Temp = 25°C, Vcc = 5.0 V			5			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

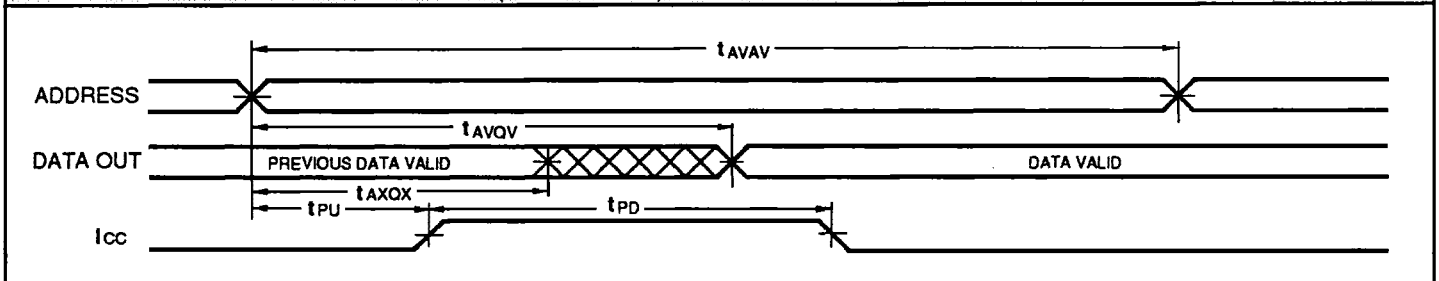
Symbol	Parameter	Test Condition	L6116-							Unit
			35	25	20	15	12	10		
ICC1	Vcc Current, Active	(Note 6)	75	100	125	160	200	220		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

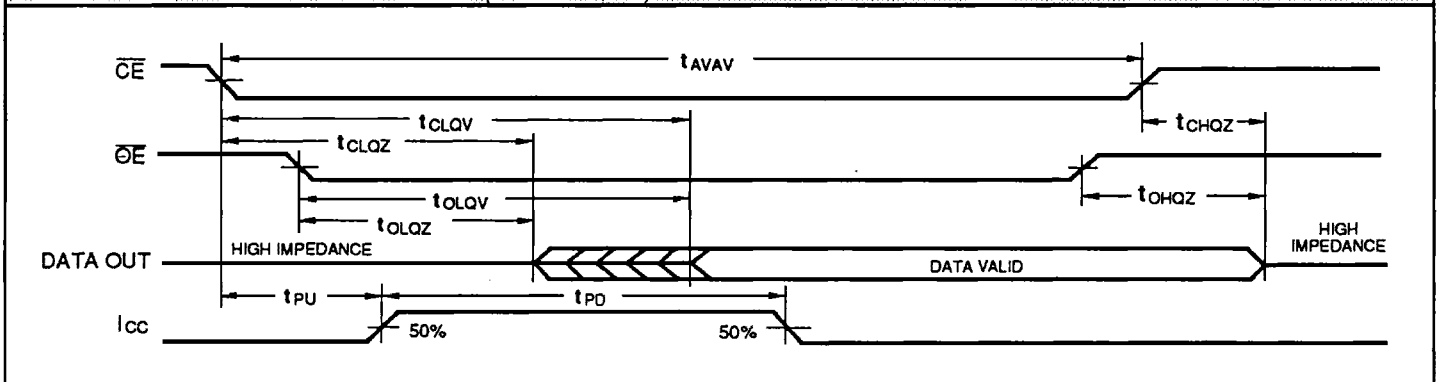
READ CYCLE (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L6116-													
		35		25		20		15		12		10		Min	Max
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tAVAV	Read Cycle Time	35		25		20		15		12		10			
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		
tAXQX	Address Change to Output Change	3		3		3		3		3		3			
tCLOV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		
tCLOZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3			
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		5		
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0			

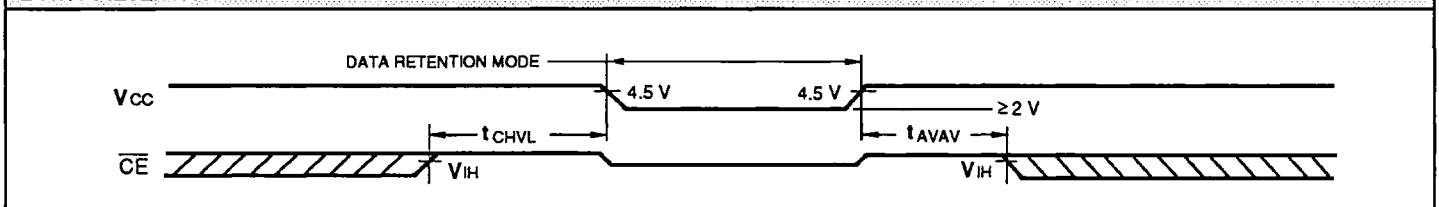
READ CYCLE — ADDRESS CONTROLLED (Notes 13, 14)



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED (Notes 13, 15)



DATA RETENTION

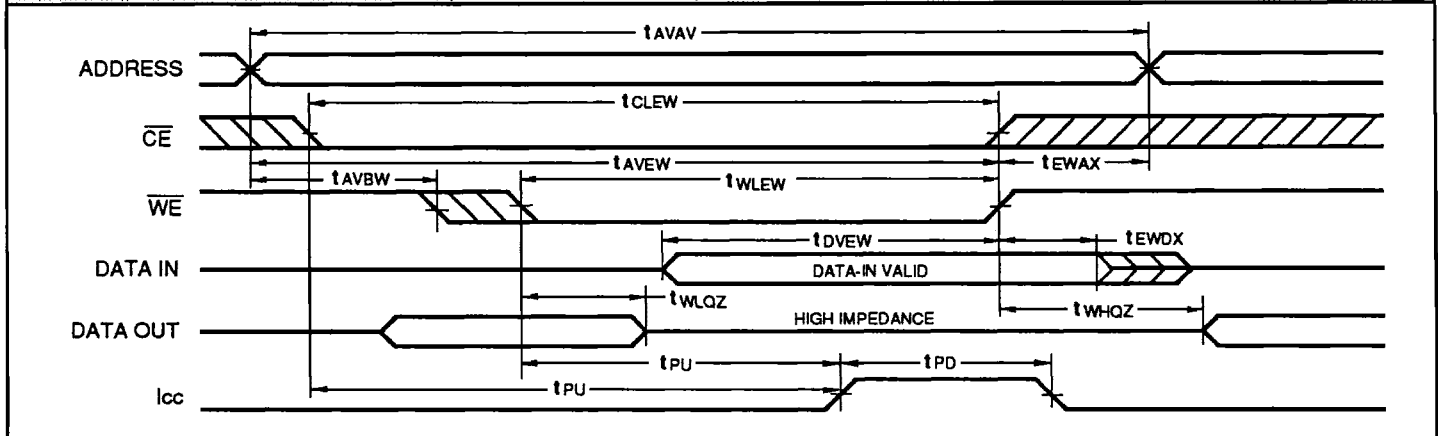


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

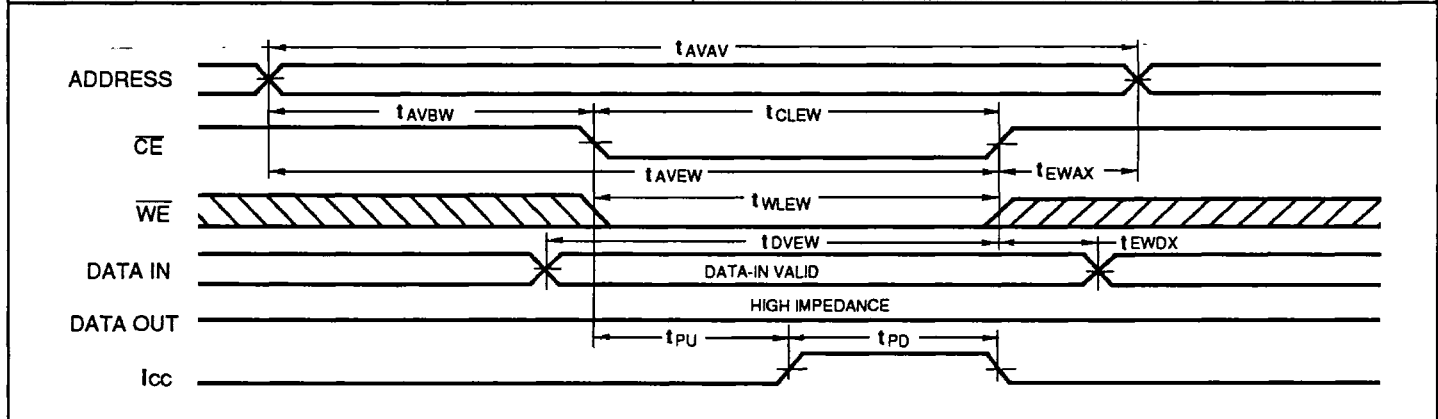
WRITE CYCLE (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L6116-													
		35		25		20		15		12		10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12		10			
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0			
twLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8			
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5			
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1		1			
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0			
twLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		

WRITE CYCLE — WE CONTROLLED (Notes 16, 17, 18, 19)



WRITE CYCLE — CE CONTROLLED (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at -0.6 V. A current in excess of 100 mA is required to reach -2 V. The device can withstand indefinite operation with inputs as low as -3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \leq V_{IL}$, $\overline{WE} \leq V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \geq V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. \overline{CE} must be $\geq V_{CC} - 0.2$ V. For the L6116, all other inputs must meet $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V is required to ensure full powerdown. For the L6116 (low power version), this requirement applies only to \overline{CE} and \overline{WE} ; there are no restrictions on data and addresses.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. \overline{WE} is high for the read cycle.

14. The chip is continuously selected (\overline{CE} low).

15. All address lines are valid prior-to or coincident-with the \overline{CE} transition to low.

16. The internal write cycle of the memory is defined by the overlap of \overline{CE} low and \overline{WE} low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If \overline{WE} goes low before or concurrent with \overline{CE} going low, the output remains in a high impedance state.

18. If \overline{CE} goes high before or concurrent with \overline{WE} going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

- a. Falling edge of \overline{CE} .
- b. Falling edge of \overline{WE} (\overline{CE} active).
- c. Transition on any address line (\overline{CE} active).
- d. Transition on any data line (\overline{CE} and \overline{WE} active).

The device automatically powers down from ICC1 to ICC2 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

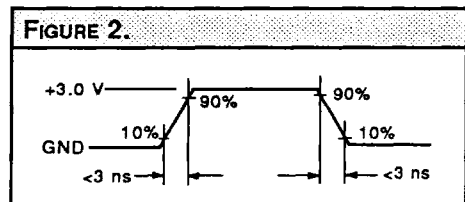
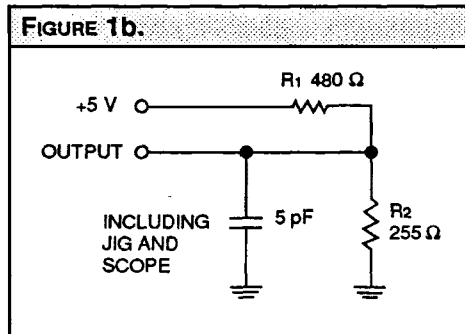
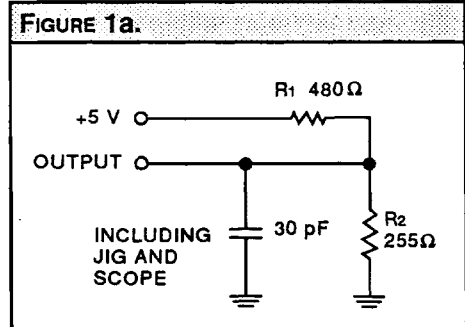
21. Transition is measured ± 200 mV from steady state voltage with specified loading

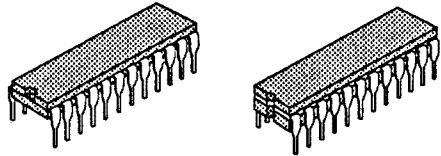
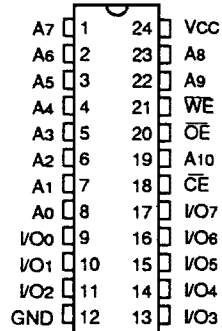
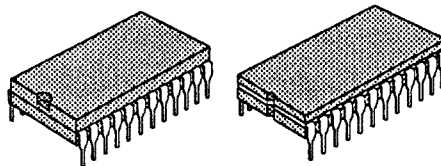
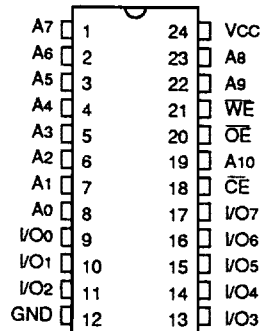
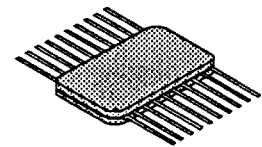
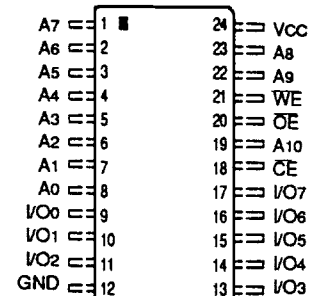
in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. \overline{CE} or \overline{WE} must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.



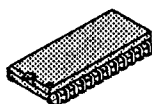
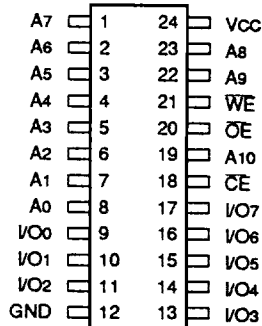
ORDERING INFORMATION
24-pin — DIP (0.3" wide)

24-pin — DIP (0.6" wide)

24-pin — CERFLAT


Speed	Plastic DIP (P2)	CerDIP (C1)	Plastic DIP (P1)	CerDIP (C4)	CerFlat (M1)
0°C to +70°C — COMMERCIAL SCREENING					
35 ns	L6116PC35*	L6116CC35*	L6116NC35*	L6116IC35*	L6116MC35*
25 ns	" " 25*	" " 25*	" " 25*	" " 25*	" " 25*
20 ns	" " 20*	" " 20*	" " 20*	" " 20*	" " 20*
15 ns	" " 15*	" " 15*	" " 15*	" " 15*	" " 15*
12 ns	" " 12*	" " 12*	" " 12*	" " 12*	" " 12*
10 ns	" " 10*	" " 10*	" " 10*	" " 10*	" " 10*
-55°C to +125°C — COMMERCIAL SCREENING					
35 ns		L6116CM35*		L6116IM35*	L6116MM35*
25 ns		" " 25*		" " 25*	" " 25*
20 ns		" " 20*		" " 20*	" " 20*
15 ns		" " 15*		" " 15*	" " 15*
12 ns		" " 12*		" " 12*	" " 12*
-55°C to +125°C — MIL-STD-883 COMPLIANT					
35 ns		L6116CMB35*		L6116IMB35*	L6116MMB35*
25 ns		" " 25*		" " 25*	" " 25*
20 ns		" " 20*		" " 20*	" " 20*
15 ns		" " 15*		" " 15*	" " 15*
12 ns		" " 12*		" " 12*	" " 12*

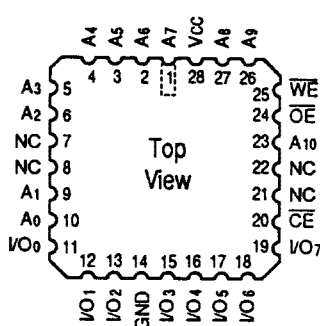
*The Low Power version is specified by adding the "L" suffix after the speed grade (i.e., L6116CMB35L).

ORDERING INFORMATION

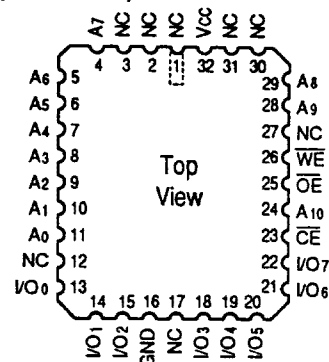
24-pin — SOJ



28-pin — LCC (450 x 450)



32-pin — LCC (450 x 550)



Speed	Plastic SOJ (.300" — W1)	Ceramic Leadless Chip Carrier (K1)	Ceramic Leadless Chip Carrier (K7)
0°C to +70°C — COMMERCIAL SCREENING			
35 ns	L6116WC35*	L6116KC35*	L6116TC35*
25 ns	" " 25*	" " 25*	" " 25*
20 ns	" " 20*	" " 20*	" " 20*
15 ns	" " 15*	" " 15*	" " 15*
12 ns	" " 12*	" " 12*	" " 12*
10 ns	" " 10*	" " 10*	" " 10*
-55°C to +125°C — COMMERCIAL SCREENING			
35 ns		L6116KM35*	L6116TM35*
25 ns		" " 25*	" " 25*
20 ns		" " 20*	" " 20*
15 ns		" " 15*	" " 15*
12 ns		" " 12*	" " 12*
-55°C to +125°C — MIL-STD-883 COMPLIANT			
35 ns		L6116KMB35*	L6116TMB35*
25 ns		" " 25*	" " 25*
20 ns		" " 20*	" " 20*
15 ns		" " 15*	" " 15*
12 ns		" " 12*	" " 12*

*The Low Power version is specified by adding the "L" suffix after the speed grade (i.e., L6116KMB35L).