Green-mode PFC/Flyback-PWM Controller **SG6902**

FEATURES

- Green-mode PFC and PWM operation
- No switching of PFC at light loads for the best power saving
- Low start-up and operating current
- Innovative *Switching-Charge®* multiplier-divider
- Multi-vector control for improved PFC output transient response
- Interleaved PFC/PWM switching
- Programmable two-level PFC output voltage
- Average-current-mode control for PFC
- Cycle-by-cycle current limiting for PFC/PWM
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Brownout protection
- Over-temperature protection

APPLICATIONS

- Switching Power Suppliers with Active PFC
- High-Power Adaptors

DESCRIPTION

The highly integrated SG6902 is specially designed for power supplies consist of boost PFC and Flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections. It is available in 20-pin SOP and SSOP packages.

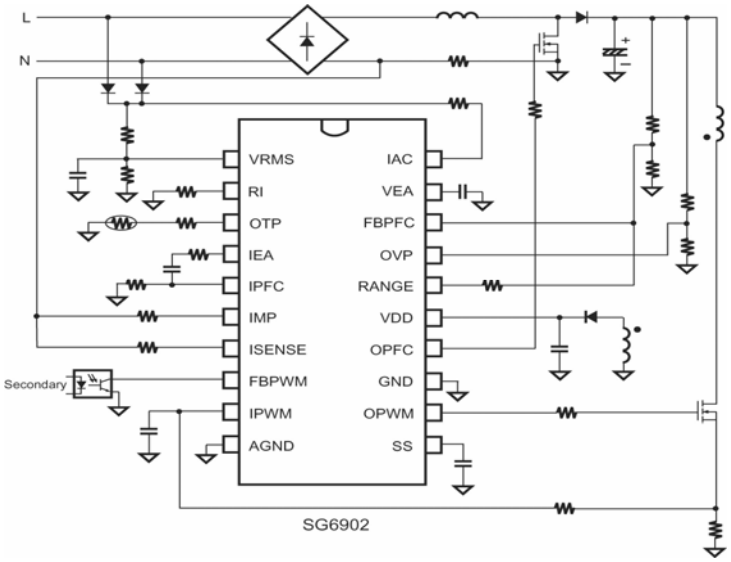
The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is further reduced, the PFC stage is turned off to further reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6902 will shut off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control will reduce the PFC output voltage at low line input to increase the efficiency of the power supply.

For the Flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6902 provides complete protection functions such as brownout protection and RI pin open/short protections.

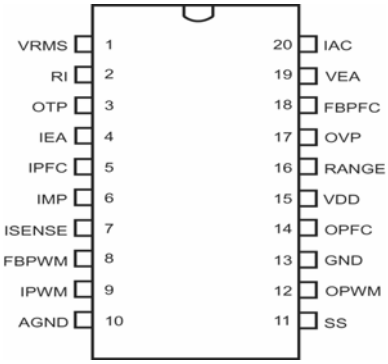
TYPICAL APPLICATION



MARKING DIAGRAM

T: S= SOP ,R = SSOP
P : Z =Lead Free
+ ROHS Compatible
Null=regular package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



ORDERING INFORMATION

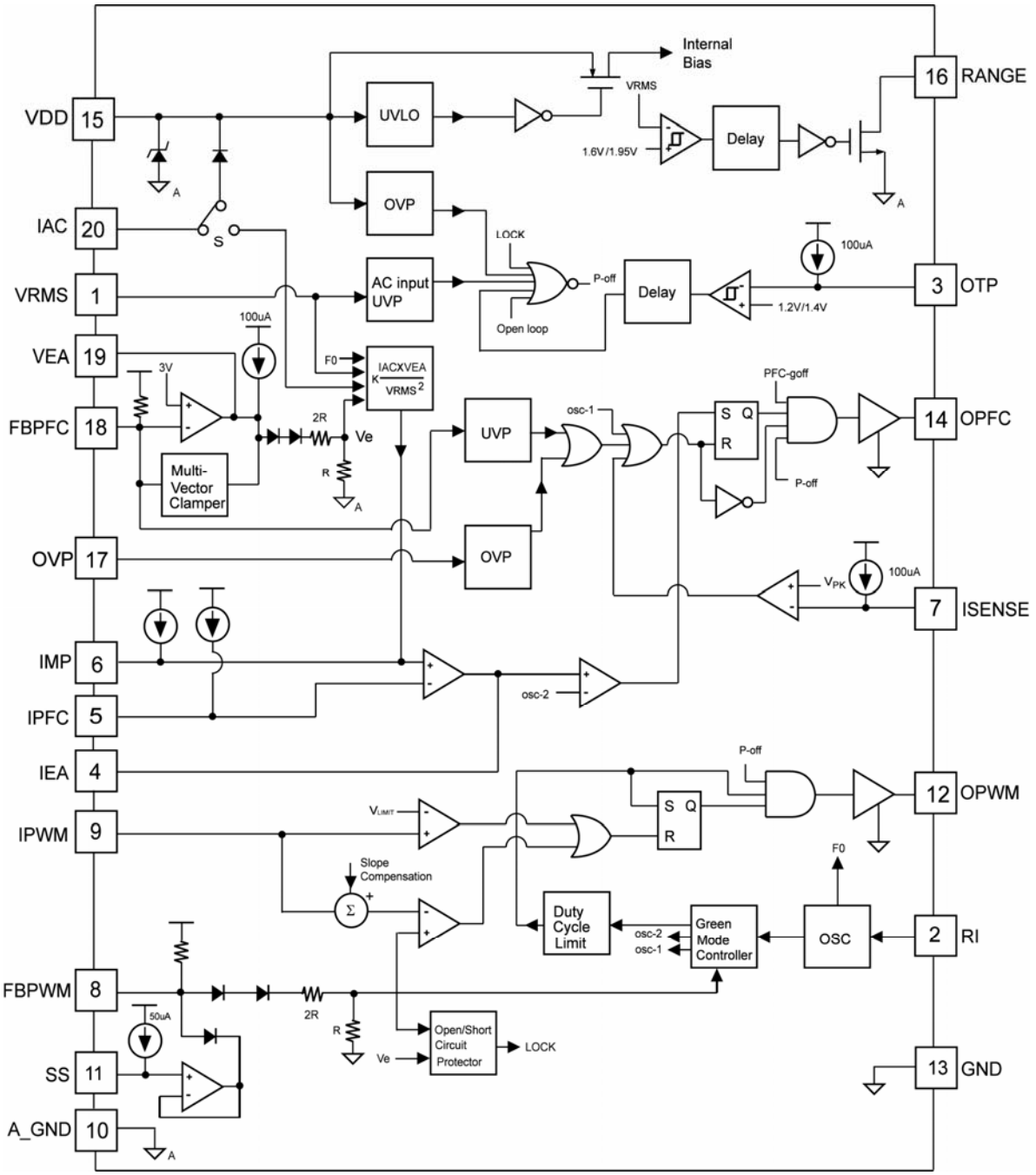
Part Number	Package
SG6902SZ	20-pin SOP(Lead Free)
SG6902RZ	20-pin SSOP(Lead Free)

PIN DESCIRPTIONS

Name	Pin No.	Type	Function
VRMS	1	Line-voltage Detection	Line-voltage detection. The pin is used for PFC multiplier, RANGE control of PFC output voltage, brownout protection .For brownout protection, the controller will be disabled after a delay time when the VRMS voltage drops below a threshold.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and AGND determines the switching frequency. The switching frequency is equal to [1560 / RI] kHz, where RI is in kΩ. For example, if RI is equal to 24kΩ, then the switching frequency will be 65 kHz.
OTP	3	Over Temperature Protection	This pin supplies an over-temperature protection signal. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6902 will be disabled.
IEA	4	Output for PFC Current Amplifier	This is the output of the PFC current error amplifier. The signal from this pin will be compared with an internal saw-tooth and hence determine the pulse width for PFC gate drive.
IPFC	5	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current error amplifier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
IMP	6	Non-inverting Input for PFC Current Amplifier	The non-inverting input of the PFC current amplifier and also the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
ISENSE	7	Peak Current Limit Setting for PFC	The peak-current setting for PFC.

FBPWM	8	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a resistor. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
IPWM	9	PWM Current Sense	The current-sense input for the Flyback PWM. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
AGND	10	Ground	Signal Ground
SS	11	PWM Soft Start	During startup, the SS pin will charge an external capacitor with a 50uA (RI=24kΩ) constant current source. The voltage on FBPWM will be clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.
OPWM	12	PWM Gate Drive	The totem-pole output drive for the Flyback PWM MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
GND	13	Ground	Power Ground
OPFC	14	PFC Gate Drive	The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
VDD	15	Supply	The power supply pin.
RANGE	16	PFC Output-voltage Control	Two-level output voltage setting for PFC. The PFC output voltage at low line can be reduced to improve efficiency. The RANGE pin is of high impedance while the VRMS voltage is lower than a threshold.
OVP	17	PFC Over Voltage Input	The PFC stage over voltage input. The comparator will disable the PFC output driver if the voltage at this input exceeds a threshold. This pin can be connected to FBPFC or it can be connected to the PFC boost output through a divider network.
FBPFC	18	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amp. This pin is connected to the PFC output through a divider network.
VEA	19	Error-Amp Output for PFC Voltage Feedback Loop	The error-amp output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value will result in a narrow bandwidth and hence improve the power factor.
IAC	20	Input AC Current	Before start-up, this input is used to provide startup current for VDD. For normal operation, this input is used to provide current reference for the multiplier.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{DD}	DC Supply Voltage*	25		V
I_{AC}	Input AC Current	2		mA
V_{HIGH}	OPWM, OPFC, IAC	-0.3 to +25V		V
V_{LOW}	Others	-0.3 to +7V		V
P_D	Power Dissipation At T_A < 50°C	SOP	1.15	W
		SSOP	0.8	
T_J	Operating Junction Temperature	-40 to +125		℃
T_{STG}	Storage Temperature Range	-55 to +150		℃
$R_{\theta j\text{-}C}$	Thermal resistance (Junction to Case)	SOP	23.64	℃/W
		SSOP	39.6	
T_L	Lead Temperature (Wave soldering or IR, 10seconds)	260		℃
ESD	ESD capability, HBM model	4.5		KV
	ESD capability, Machine model	250		V

*All voltage values, except differential voltages, are given with respect to GND pin.

*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Operating Ambient Temperature*	-30 to +85	℃

*For proper operation

ELECTRICAL CHARACTERISTICS (V_{DD}=15V,T_A=25°C UNLESS NOTED)

VDD Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$I_{DD\text{-}ST}$	Start-up Current	$V_{TH\text{-}ON}$ –0.16V		10	25	uA
$I_{DD\text{-}OP}$	Operating Current	OPFC, OPWM Open, RI = 24kΩ		6	10	mA
$V_{TH\text{-}ON}$	Start Threshold Voltage		15	16	17	V
$V_{DD\text{-}MIN}$	Minimum Operating Voltage		9	10	11	V
$V_{DD\text{-}OVP}$	VDD OVP Threshold		23.5	24.5	25.5	V
$T_{VDD\text{-}OVP}$	Debounce Time of VDD OVP	RI = 24kΩ	8		25	uS
$V_{DD\text{-}TH\text{-}G}$	VDD Low-Threshold Voltage to Exit Green-OFF Mode		$V_{DD\text{-}MIN}$ +0.9	$V_{DD\text{-}MIN}$ +1.5	$V_{DD\text{-}MIN}$ +2.1	V

Oscillator & Green-Mode Operation

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RI}	RI Voltage		1.176	1.2	1.224	V
F_{OSC}	PWM Frequency	RI = 24kΩ	62	65	68	KHz
$F_{OSC-MINFREQ}$	Minimum Frequency in Green Mode	RI = 24kΩ	18	20	22.5	KHz
RI	RI Pin Resistance Range		15		47	KΩ
RI_{OPEN}	RI Pin Open Protection If RI> RI_{open} , SG6902 will turn Off			200		KΩ
RI_{SHORT}	RI Pin Short Protection If RI< RI_{short} , SG6902 will turn Off			2		KΩ

VRMS for UVP and RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under Voltage Protection Threshold (with T_{UVP} delay)		0.75	0.8	0.85	V
$V_{RMS-UVP-2}$	Recovery level on VRMS		$V_{RMS-UVP-1}$+0.16V	$V_{RMS-UVP-1}$+0.18V	$V_{RMS-UVP-1}$+0.2V	V
T_{D-PWM}	When UVP Occurs ,The interval from PFC off to PWM off	RI = 24kΩ	$T_{UVP-Min}$ +9		$T_{UVP-Min}$ +14	mS
T_{UVP}	Under Voltage Protection Delay Time (No delay for startup)	RI = 24kΩ	150	195	240	mS
V_{RMS-H}	High V_{RMS} Threshold for RANGE Comparator		1.9	1.95	2.0	V
V_{RMS-L}	Low V_{RMS} Threshold for RANGE Comparator		1.55	1.6	1.65	V
T_{RANGE}	Range-enable Delay Time	RI = 24kΩ	145	170	200	mS
V_{OL}	Output Low Voltage of RANGE Pin	I_o = 1mA			0.5	V
I_{OH}	Output High Leakage Current of RANGE Pin	RANGE = 5V			50	nA

PFC STAGE

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3	3.05	V
Av_{-PFC} *1	Open-loop Gain			60		dB
Z_O *1	Output Impedance			110		KΩ
OVP_{PFC}	PFC Over Voltage Protection (OVP pin)		3.2	3.25	3.3	V
$\triangle OVP_{PFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$T_{OVP-PFC}$	Debounce Time of PFC OVP	RI = 24kΩ	40	70	120	uS
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.1	3.15	3.2	V
$G_{FBPFC-H}$ *1	Clamp-High Gain			0.5		mA/V
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.9	V
$G_{FBPFC-L}$ *1	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2		mA

$I_{FBPFC-H}$	Maximum Sink Current		70	110		uA
UVP_{FBPFC}	PFC Feedback Under Voltage Protection		0.35	0.4	0.45	V
V_{FBHIGH}	FB Open Voltage		6	7	8	V
$T_{UVP-PFC}$	Debounce Time of PFC UVP	RI = 24kΩ	40	70	120	uS

Note[*1]: Not tested in production test;

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage			8		mV
A_I[*1]	Open-loop Gain			60		dB
BW[*1]	Unit Gain Bandwidth			1.5		MHz
CMRR[*1]	Common-mode Rejection Ratio	V_{CM} = 0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	RI = 24kΩ (I_{MR} = 20+I_{RI}*0.8)	50		70	uA
I_L	Maximum Source Current			3		mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	RI = 24kΩ	90	100	110	uA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	VRMS = 1.05V	0.15	0.2	0.25	V
		VRMS = 3V	0.35	0.4	0.45	V
T_{PD-PFC}	Propagation Delay				200	nS
$T_{BNK-PFC}$	Leading-Edge Blanking Time		270	350	450	nS

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	uA
V_{DROP}	Voltage Drop from the IAC pin to VDD	I_{AC} = 240uA			3.5	V
I_{MO-MAX}[*1]	Maximum Multiplier Current Output	RI = 24 kΩ		250		uA
I_{MO-1}	Multiplier Current Output (low-line, high-power)	V_{RMS} = 1.05V; I_{AC} = 90uA; VEA = 7.5V;RI = 24 kΩ	200	250	280	uA
I_{MO-2}	Multiplier Current Output (high-line, high-power)	V_{RMS} = 3V; I_{AC} = 264uA; V_{EA} = 7.5V;RI = 24 kΩ	65	85		uA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Z-PFC}	Output Voltage Maximum (Clamp)	V_{DD} = 20V		16	18	V
T_{PFC}	The Interval of OPFC Lags Behind OPWM at Startup	RI = 24kΩ	9	11.5	14	mS
V_{OL-PFC}	Output Voltage Low	V_{DD} = 15V; I_O = 100mA			1.5	V
V_{OH-PFC}	Output Voltage High	V_{DD} = 13V; I_O = 100mA	8			V
T_{R-PFC}	Rising Time	V_{DD} = 15V; C_L = 5nF; OPFC = 2V to 9V	40	70	120	nS
T_{F-PFC}	Falling Time	V_{DD} = 15V; C_L = 5nF; OPFC = 9V to 2V	40	60	110	nS
$DC_{MAX-PFC}$	Maximum Duty Cycle		93		98	%

PWM STAGE

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
A_{v-PWM}	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB} *1	Input Impedance		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN-LOOP}$	PWM Open Loop Protection Threshold		4.2	4.5	4.8	V
$T_{OPEN-PWM}$	PWM Open Loop Protection Delay Time	RI = 24kΩ	45	56	70	mS
$V_{PFC-OFF1}$	PFC off Voltage at FBPWM	RANGE = Ground		V_G+0.2 V		V
$V_{PFC-OFF2}$	PFC off Voltage at FBPWM	RANGE = Open		V_G+0.2 V		V
$T_{PFC-OFF}$	PFC off Delay Time	RI = 24kΩ	500	650	800	mS
$V_{PFC-ON\ 1.6}$	PFC on Voltage at FBPWM	RANGE = Ground Vrms =1.6V		V_G+0.35V		V
$V_{PFC-ON\ 2.85}$	PFC on Voltage at FBPWM	RANGE = Ground Vrms =2.85V		V_G+0.35V		V
$V_{PFC-ON\ 0.8}$	PFC on Voltage at FBPWM	RANGE = Open Vrms =0.8V		V_G+0.85V		V
$V_{PFC-ON\ 1.95}$	PFC on Voltage at FBPWM	RANGE = Open Vrms =1.95V		V_G+0.5 V		V
V_N	Frequency Reduction Threshold on FBPWM	RANGE = Ground	1.9	2.1	2.3	V
S_G *1	Green-Mode Modulation Slope		60	75	90	Hz/V
V_G	Voltage on FBPWM at Fs = 20KHz		1.35	1.6	1.75	V

PWM-Current Sense

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{PD-PWM}	Propagation Delay to Output		60		120	nS
$V_{LIMIT-1}$	Peak Current Limit Threshold Voltage1	RANGE = Open	0.65	0.7	0.75	V
$V_{LIMIT-2}$	Peak Current Limit Threshold Voltage2	RANGE = Ground	0.6	0.65	0.7	V
$T_{BNK-PWM}$	Leading-Edge Blanking Time		270	350	450	nS
$\triangle V_{SLOPE}$	Slope Compensation $\triangle V_S = \triangle V_{SLOPE} \times (T_{on}/T)$ $\triangle V_S$: Compensation Voltage Added to Current Sense		0.45	0.5	0.55	V

PWM Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Z-PWM}	Output Voltage Maximum (Clamp)	V_{DD} = 20V		16	18	V
V_{OL-PWM}	Output Voltage Low	V_{DD} = 15V; I_O = 100mA			1.5	V
V_{OH-PWM}	Output Voltage High	V_{DD} = 13V; I_O = 100mA	8			V
T_{R-PWM}	Rising Time	V_{DD} = 15V; C_L = 5nF; OPWM = 2V to 9V	30	60	120	nS
T_{F-PWM}	Falling Time	V_{DD} = 15V; C_L = 5nF; OPWM = 9V to 2V	30	50	110	nS
$DC_{MAX-PWM}$	Maximum Duty Cycle		73	78	83	%

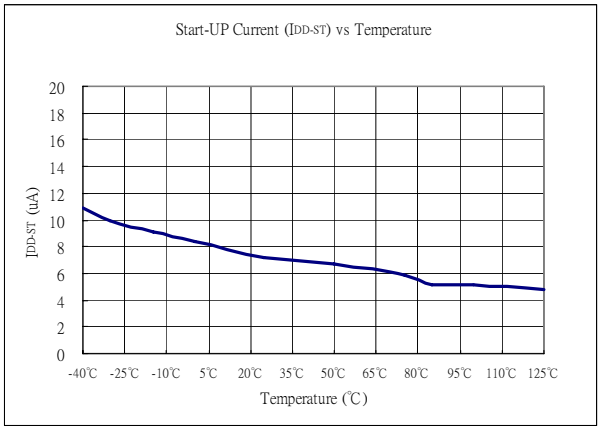
OTP section

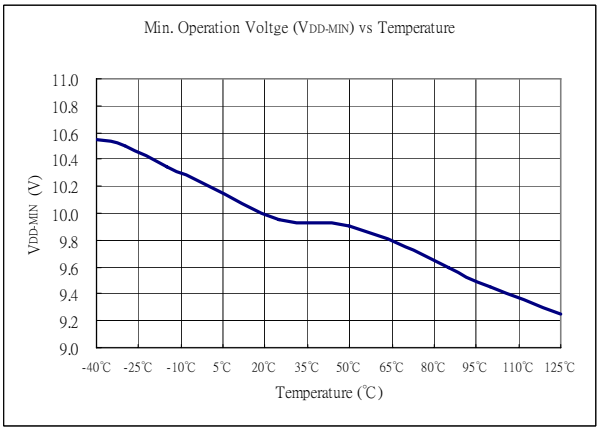
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OTP}	OTP Pin Output Current	RI = 24kΩ	90	100	11	uA
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.2	1.25	V
V_{OTP-ON}	Recovery Level on OTP		1.35	1.4	1.45	V
T_{OTP}	OTP Debounce Time	RI = 24kΩ	8		25	uS

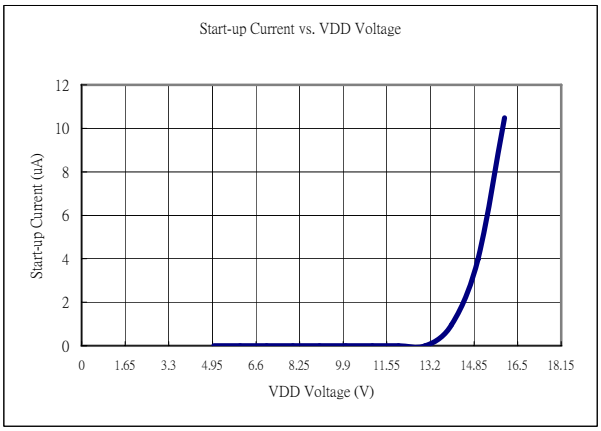
Soft Start section

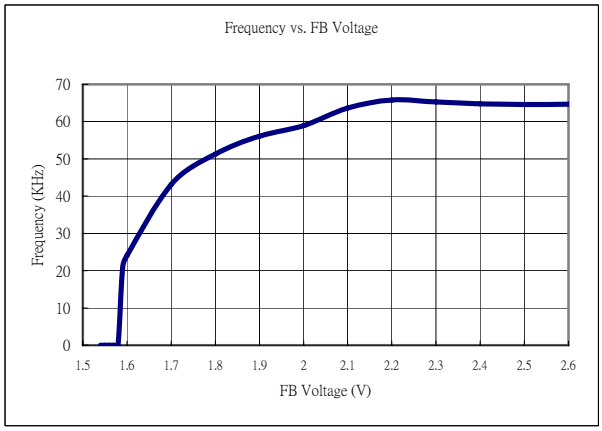
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Constant Current Output for Soft Start	RI = 24kΩ	44	50	56	uA
R_D *1	Discharge Rdson			470		Ω

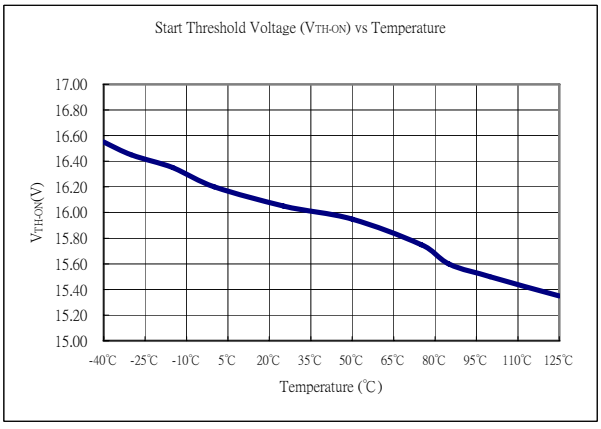
TYPICAL CHARACTERISTICS

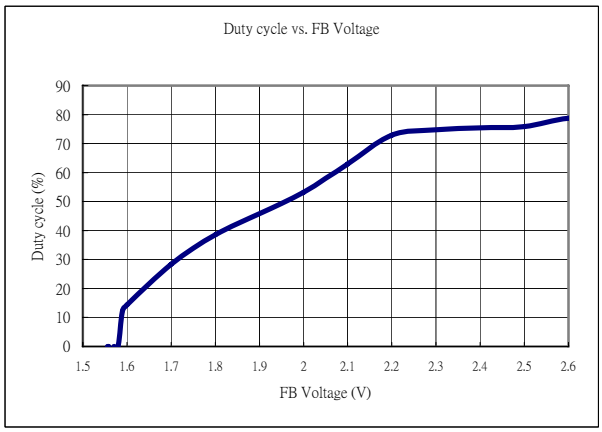


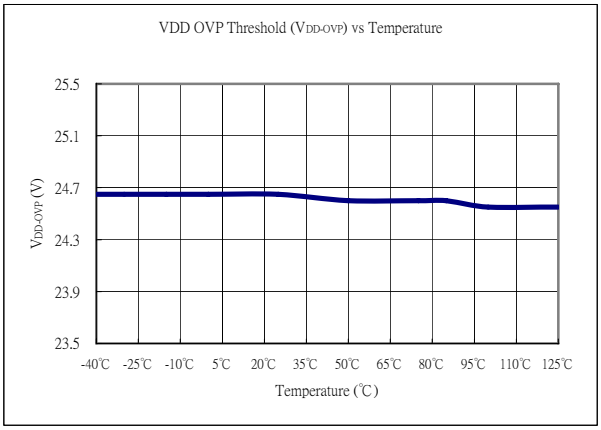


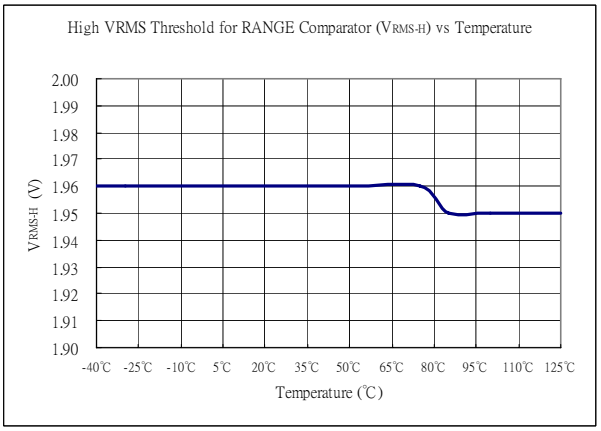


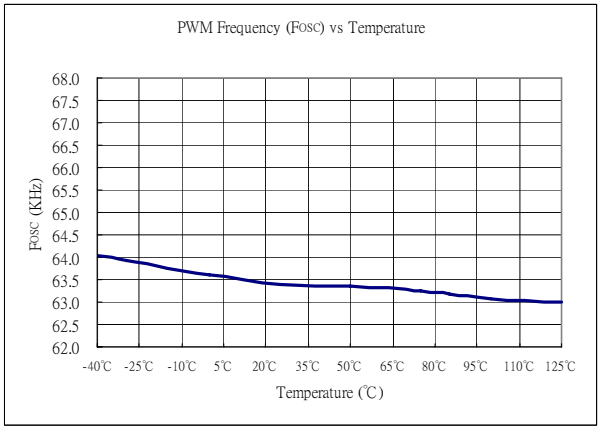


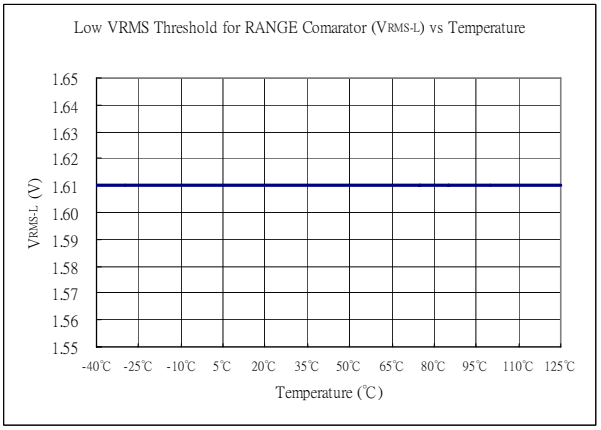


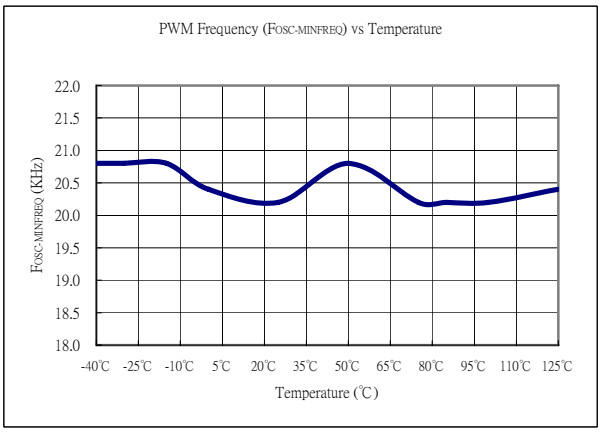


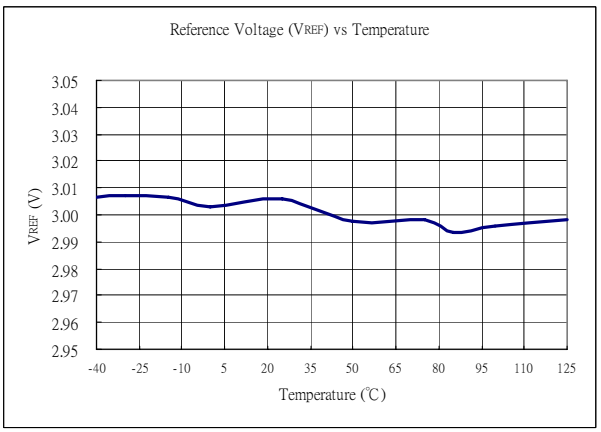

VDD OVP Threshold (VDD-OVP) vs Temperature
VDD-OVP (V)
25.5
25.1
24.7
24.3
23.9
23.5
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

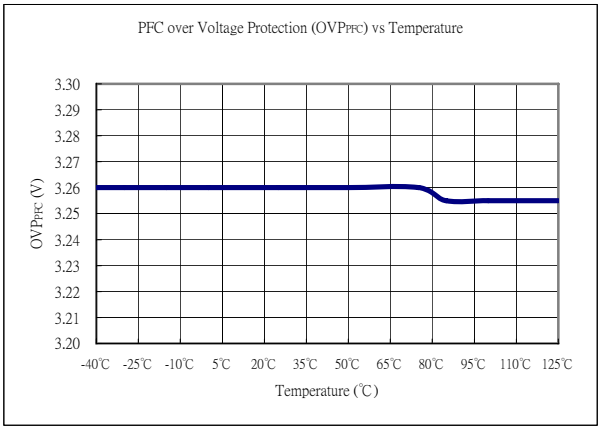

High VRMS Threshold for RANGE Comparator (VRMS-H) vs Temperature
VRMS-H (V)
2.00
1.99
1.98
1.97
1.96
1.95
1.94
1.93
1.92
1.91
1.90
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

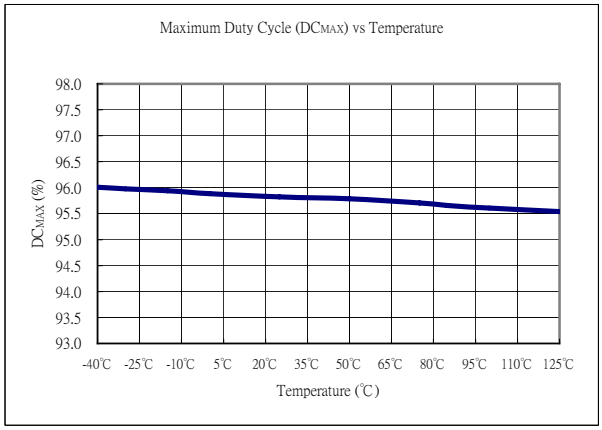

PWM Frequency (FOSC) vs Temperature
FOSC (KHz)
68.0
67.5
67.0
66.5
66.0
65.5
65.0
64.5
64.0
63.5
63.0
62.5
62.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

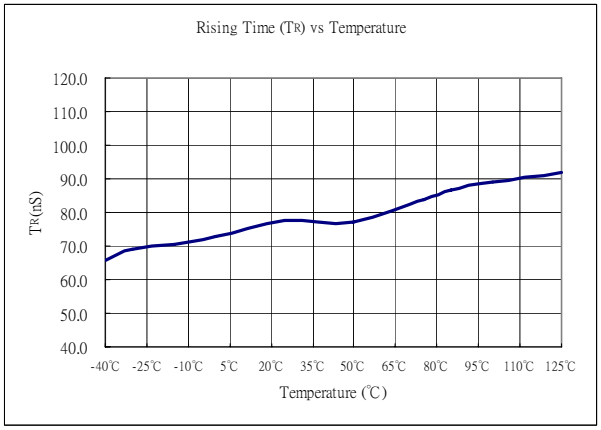

Low VRMS Threshold for RANGE Comarator (VRMS-L) vs Temperature
VRMS-L (V)
1.65
1.64
1.63
1.62
1.61
1.60
1.59
1.58
1.57
1.56
1.55
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

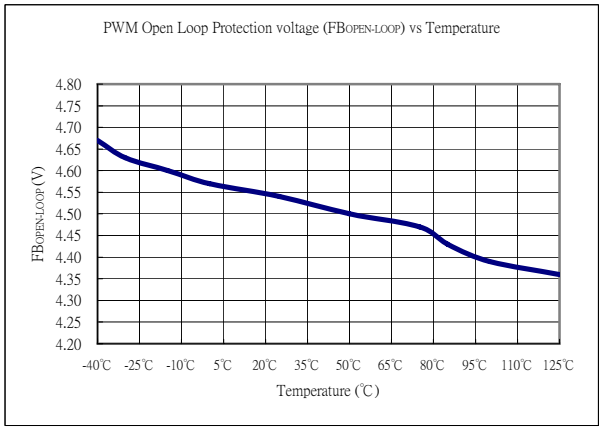

PWM Frequency (FOSC-MINFREQ) vs Temperature
FOSC-MINFREQ (KHz)
22.0
21.5
21.0
20.5
20.0
19.5
19.0
18.5
18.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

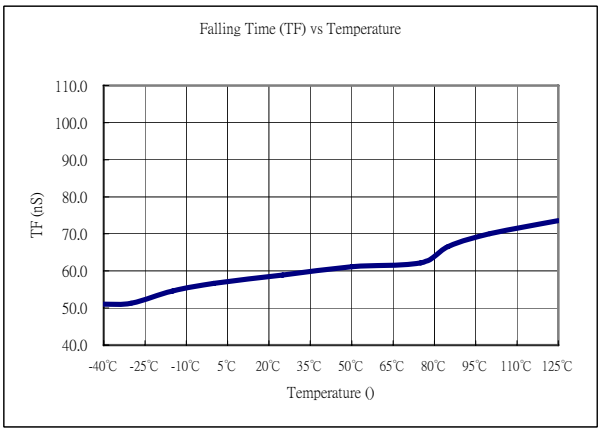

Reference Voltage (VREF) vs Temperature
VREF (V)
3.05
3.04
3.03
3.02
3.01
3.00
2.99
2.98
2.97
2.96
2.95
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

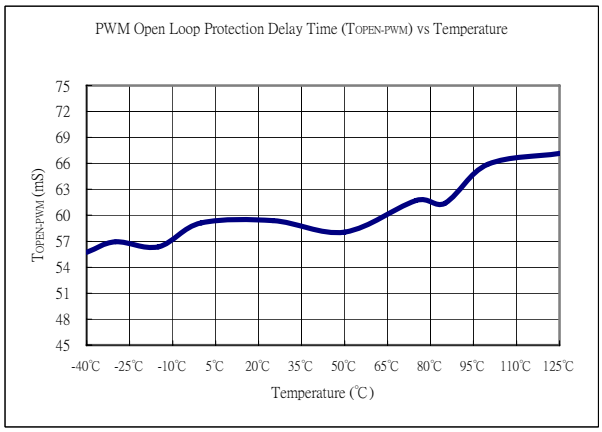

PFC over Voltage Protection (OVPPFC) vs Temperature
OVPPFC (V)
3.30
3.29
3.28
3.27
3.26
3.25
3.24
3.23
3.22
3.21
3.20
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

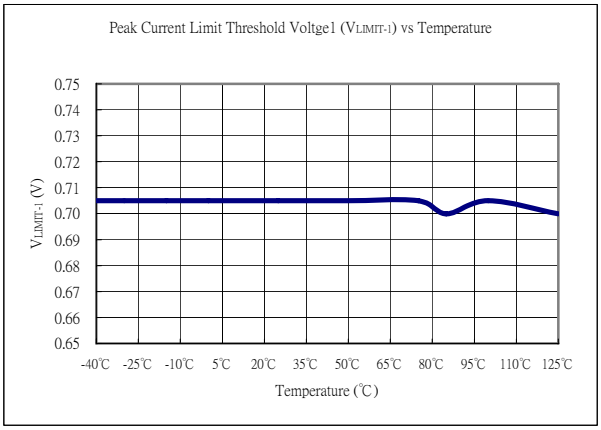

Maximum Duty Cycle (DCMAX) vs Temperature
DCMAX (%)
98.0
97.5
97.0
96.5
96.0
95.5
95.0
94.5
94.0
93.5
93.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

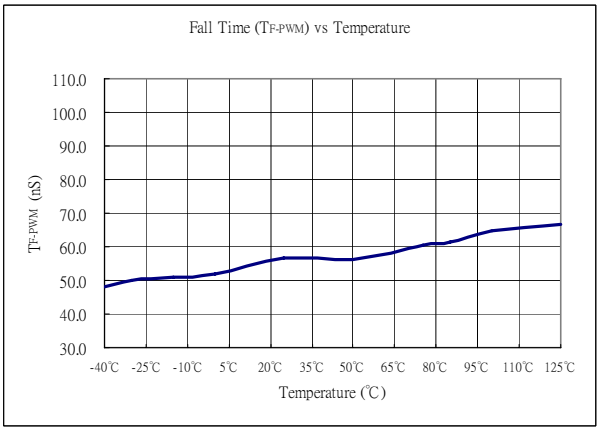

Rising Time (TR) vs Temperature
TR(nS)
120.0
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

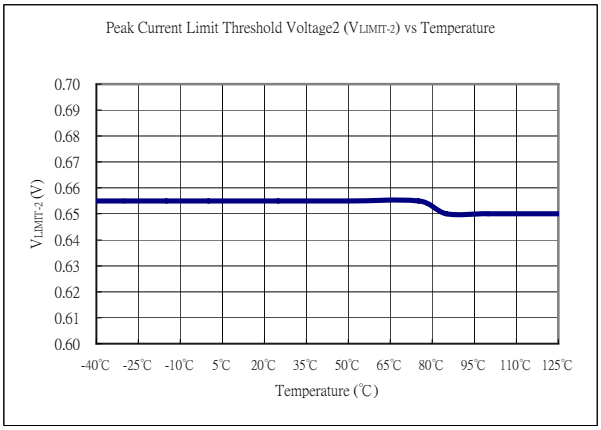

PWM Open Loop Protection voltage (FBOPEN-LOOP) vs Temperature
FBOPEN-LOOP (V)
4.80
4.75
4.70
4.65
4.60
4.55
4.50
4.45
4.40
4.35
4.30
4.25
4.20
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

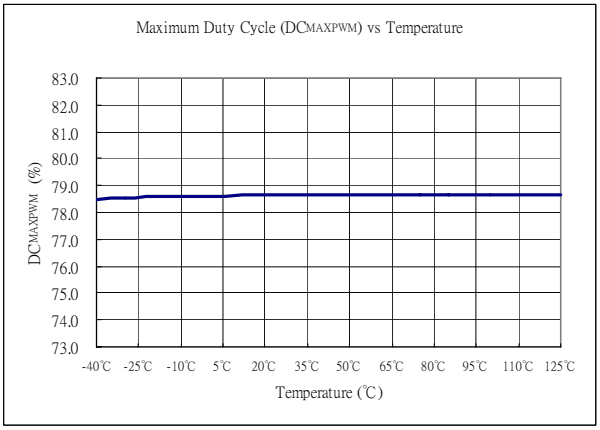

Falling Time (TF) vs Temperature
TF (nS)
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature ()

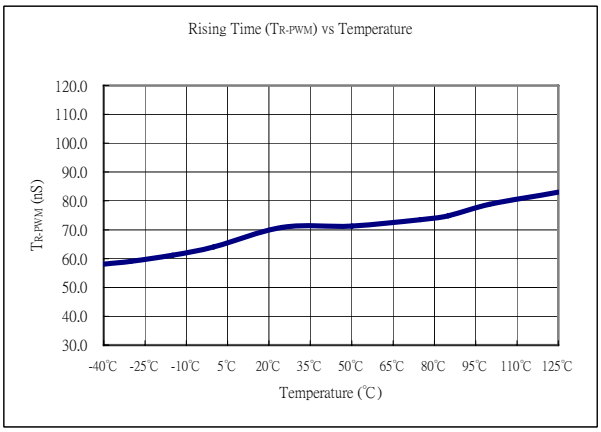

PWM Open Loop Protection Delay Time (TOPEN-PWM) vs Temperature
TOPEN-PWM (mS)
75
72
69
66
63
60
57
54
51
48
45
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

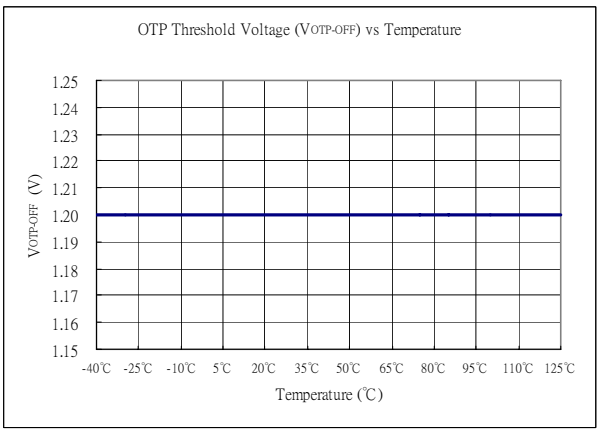

Peak Current Limit Threshold Voltge1 (VLIMIT-1) vs Temperature
VLIMIT-1 (V)
0.75
0.74
0.73
0.72
0.71
0.70
0.69
0.68
0.67
0.66
0.65
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Fall Time (TF-PWM) vs Temperature
TF-PWM (nS)
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Peak Current Limit Threshold Voltage2 (VLIMIT-2) vs Temperature
VLIMIT-2 (V)
0.70
0.69
0.68
0.67
0.66
0.65
0.64
0.63
0.62
0.61
0.60
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Maximum Duty Cycle (DCMAXPWM) vs Temperature
DCMAXPWM (%)
83.0
82.0
81.0
80.0
79.0
78.0
77.0
76.0
75.0
74.0
73.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


Rising Time (TR-PWM) vs Temperature
TR-PWM (nS)
120.0
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)


OTP Threshold Voltage (VOTP-OFF) vs Temperature
VOTP-OFF (V)
1.25
1.24
1.23
1.22
1.21
1.20
1.19
1.18
1.17
1.16
1.15
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

OPERATION DESCRIPTION

The highly integrated SG6902 is specially designed for power supply with boost PFC and Flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections/ compensation.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is further reduced, the PFC stage is turned off to further reduce power consumption.

The PFC function is implemented by average-current-mode control. The patented Switching-Charge® multiplier-divider provides a high-degree noise immunity for the PFC circuit. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6902 will shut off PFC to prevent extra-high voltage on output. Programmable two level output voltage control will reduce the PFC output voltage at low line input to increase the efficiency of the power supply.

For the Flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. Built-in line-voltage compensation maintains constant output power limit. Hiccup operation during output overloading is also guaranteed. To prevent the power supply from drawing large current during start-up, the start-up for PFC stage will be delayed 11.5ms after the operation of PWM stage.

In addition, SG6902 provides complete protection functions such as brownout protection, over-voltage and RI Pin open/short protections.

Start Up

Figure 1 shows the start up circuit of the SG6902. A resistor R_{AC} is utilized to charge V_{DD} capacitor through S1. The turn-on and turn-off threshold of SG6902 are fixed internally at 16V/10V. During start-up, the hold-up capacitor must be charged to 16V through the start-up resistor so that SG6902 will be enabled. The hold-up capacitor will continue to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during start-up. Since SG6902 consumes less than 25uA startup current, the value of R_{AC} can be large to reduce power consumption. One 10uF capacitor should hold enough energy for successful start-up. After start-up, S1 will switch so that the current I_{AC} will be the input for PFC multiplier. This helps reduce circuit complexity and power consumption.

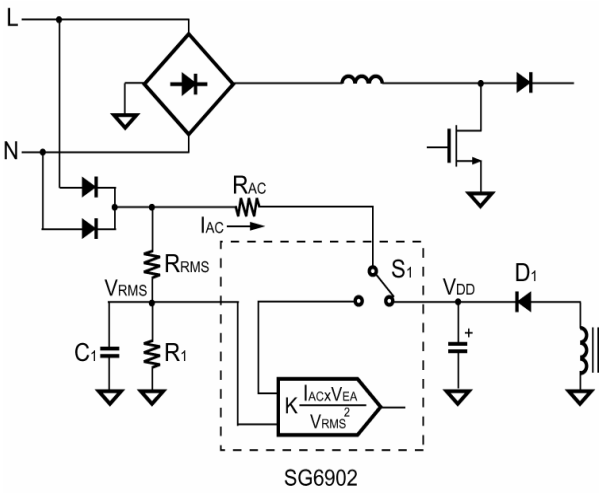


FIG.1 Start up circuit of the SG6902

Switching Frequency and Current Sources

The switching frequency of SG6902 can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$F_{OSC} = \frac{1560}{R_I\ (k\Omega)}\ (kHz) \text{ ---------- (1)}$$

For example, a 24kΩ resistor R_I results in a 65 kHz switching frequency. Accordingly, a constant Current I_T will flow through R_I.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}\ (mA) \text{ ---------- (2)}$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 2 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, range control.

For brownout protection, the SG6902 is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and range control, please refer to below sections for more details.

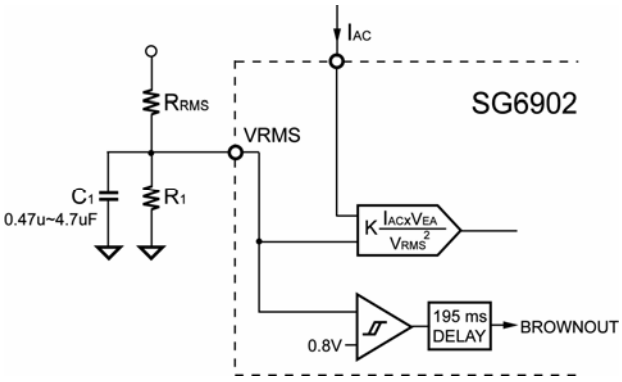


FIG.2 Line voltage detection circuit

PFC Output Voltage Control (RANGE)

For an universal input(90VAC ~ 264VAC) power supply applying active boost PFC and Flyback as a second stage, the output voltage of PFC is usually designed around 250V at low line while it is 390V at high line. This is to improve efficiency at low-line input. In SG6902, the RANGE pin (open-drain structure) is used for the two-level output voltage setting.

Figure 3 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground when the V_{RMS} voltage exceeds 1.95V while it is of high impedance (open) whenever the V_{RMS} voltage drops below 1.6V. The output voltages can be designed using below equations.

$$\text{Range} = \text{Open} \Rightarrow V_O = \frac{R_A + R_B}{R_B} \times 3V$$
$$\text{Range} = \text{Ground} \Rightarrow V_O = \frac{R_A + (R_B // R_C)}{(R_B // R_C)} \times 3V \quad \text{---- (3)}$$

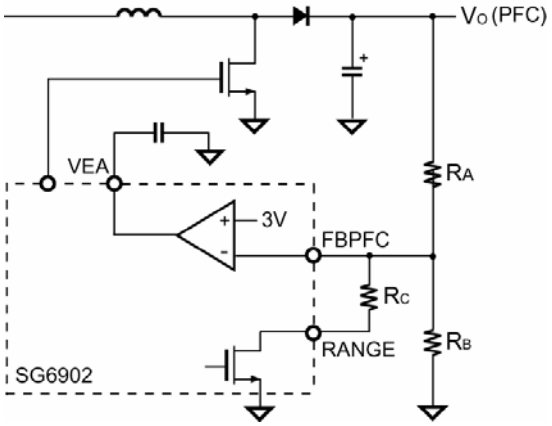


FIG.3 Range control two level output voltage

Interleave Switching and Green mode Operation

The SG6902 uses interleaved switching to synchronize the PFC and Flyback stages. This reduces switching noise and spreads the EMI emissions. Figure 4 shows that an off-time T_{OFF} is inserted in between the turn-off of the PFC gate drive and the turn-on of the PWM.

The off-time T_{OFF} is increased in response to the decreasing of the voltage level of FBPWM. Therefore, the PWM switching frequency is continuously decreased to reduce switching losses. To further reduce power losses under extra light-load conditions, the PFC stage is turned off with a 650ms delay time.

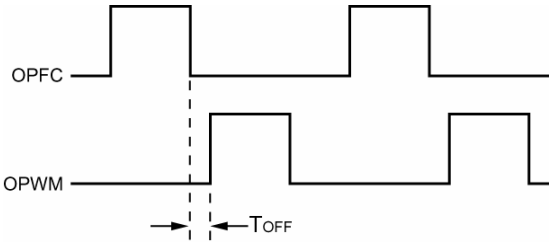


FIG.4 Interleaved switching pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase will follow that of the input voltage. Using SG6902, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and *Switching Charge®* multiplier/divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 5 shows the total control loop for the average-current-mode control circuit of SG6902.

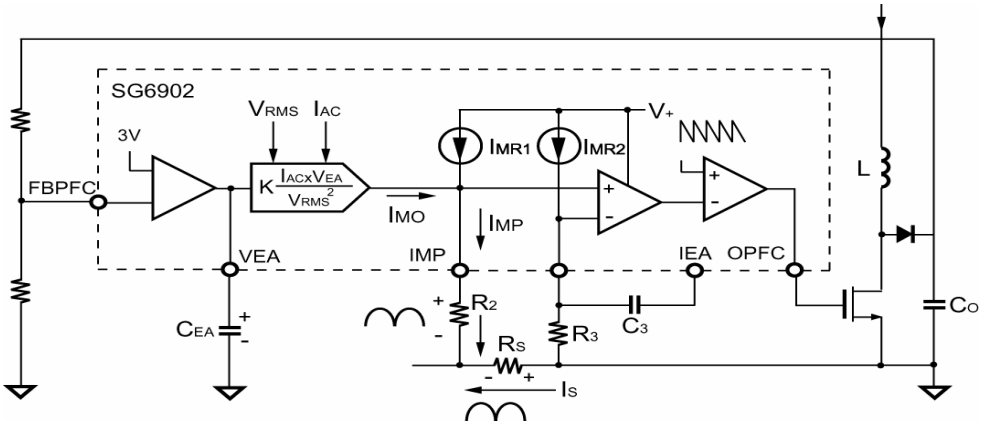


FIG.5 Average current mode control loop

The current source output from the *Switching Charge®* multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (uA) \quad \text{---------- (4)}$$

I_{MP}, the current output from IMP pin, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed current sources. R_2 and R_3 are also identical. They are used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. The constant current sources I_{MR1} and I_{MR2} are typically 60uA.

Through the differential amplification of the signal across Rs, better noise immunity is achieved. The output of IEA will be compared with an internal sawtooth and hence the pulse width for PFC is determined. Through the average current-mode control loop, the input current Is will be proportional to I_{MO}.

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{---------- (5)}$$

According to equation (5), the minimum value of R2 and maximum of Rs can be determined since I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor Rs. The value of Rs should be small to reduce power consumption, but it should be large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC as possible according to equation (4). In other words, good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The trans-conductance error amplifier has output impedance Z_O (>90kΩ) and a capacitor C_{EA} (1uF ~ 10uF)should be connected to ground (Fig. 5). This establishes a dominant pole f1 (equation 6) for the voltage loop.

$$f_1 = \frac{1}{2\pi \times R_0 \times C_{EA}} \quad \text{---------- (6)}$$

The average total input power can be expressed as:

$$Pin = Vin(rms) \times Iin(rms)$$
$$\propto V_{RMS} \times I_{MO}$$
$$\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{2}} \quad \text{---------- (7)}$$
$$\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^{2}}$$
$$= \sqrt{2} \times \frac{V_{EA}}{R_{AC}}$$

From equation (7), V_{EA}, the output of the voltage error amplifier, actually controls the total input power and hence the power delivered to the load.

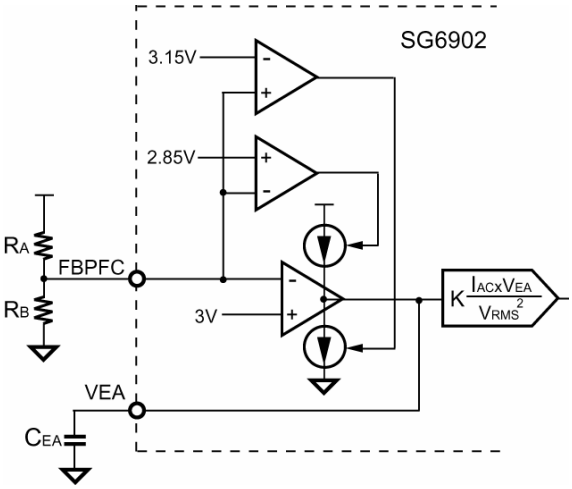


FIG.6 Multi-vector error amplifier

Multi-vector Error Amplifier

The voltage-loop error amplifier of SG6902 is trans-conductance, which has high output impedance (> 90kΩ). A capacitor C_{EA} (1uF ~ 10uF) connected from VEA to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative *Multi-Vector Error Amplifier* provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 6 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ± 5% of the reference voltage, the trans-conductance error amplifier will adjust its output impedance to increase the loop response. If R_A is opened, SG6902 will shut off immediately to prevent extra-high voltage on the output capacitor.

PFC Over-voltage Protection

When the OVP feedback voltage exceeds the over-voltage threshold, the SG6902 will inhibit the PFC switching signal. This protection also prevents the PFC power converter from operating abnormally while the FBPFC pin is open.

Cycle-by-cycle Current Limiting

SG6902 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 7 shows the peak current limit for the PFC stage. The PFC gate drive will be terminated once the voltage on ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and VRMS is also shown in Figure 7.

The amplitude of the constant current I_P is determined by the internal current reference I_T, according to the following equation:

$$I_P = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad \text{---------- (8)}$$

Therefore the peak current of the I_S is given by (V_{RMS}<1.05V),

$$I_{S\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{---------- (9)}$$

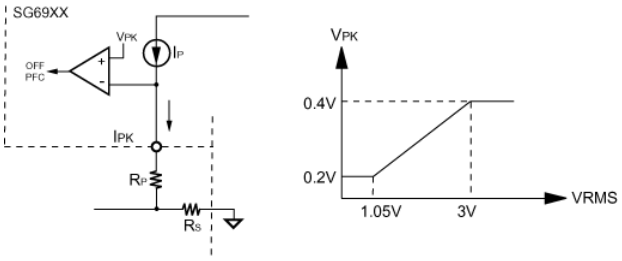


FIG.7 VRMS controlled current limiting

Flyback PWM and Slope Compensation

As shown in Fig.8, peak-current-mode control is utilized for Flyback PWM. The SG6902 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous current-mode operation.

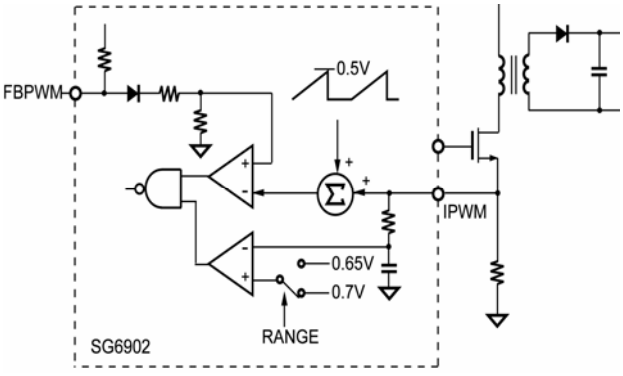


FIG.8 Peak current control loop

When the IPWM voltage, across the sense resistor, reaches the threshold voltage, 0.65V or 0.7V selected by RANGE, the OPWM will be turned off after a small propagation delay T_{PD-PWM}. This propagation delay will introduce an additional current proportional to T_{PD-PWM}*V_{PFC}/Lp, where V_{PFC} is the output voltage of PFC and Lp is the magnetized inductance of Flyback transformer. Since the propagation delay is nearly constant, higher V_{PFC} will result in a larger additional current and hence the output power limit is also higher than that under low V_{PFC}. To compensate this variation, the peak current threshold is modulated by the RANGE output. When RANGE is shorted to GND, the PFC output voltage is high and the corresponding threshold is 0.65V. When RANGE is opened, the PFC output voltage is low and the corresponding threshold is 0.7V.

Limited Power Control

Every time when the output of power supply is shorted or over loaded, the FBPWM voltage will increase. If the FB voltage is higher than a designed threshold, 4.5V, for longer than 56mS, the OPWM will then be turned off. As OPWM is turned off, the supply voltage VDD will also begin decreasing.

When V_{DD} is lower than the turn-off threshold such as 10V, SG6902 will be totally shut down. Due to the start up resistor, V_{DD} will be charged up to the turn-on threshold voltage 16V until SG6902 is enabled again. If the over loading condition still exists, the protection will take place repeatedly. This will prevent the power supply from being overheated under over loading condition.

Over-temperature Protection

SG6902 provides an OTP pin for over-temperature protection. A constant current is output from this pin. If RI is equal to 24kΩ, then the magnitude of the constant current will be 100uA. An external NTC thermistor must be connected from this pin to ground shown as Fig.9. When the OTP voltage drops below 1.2V, SG6902 will be disable. Until OTP voltage exceeds 1.4V.

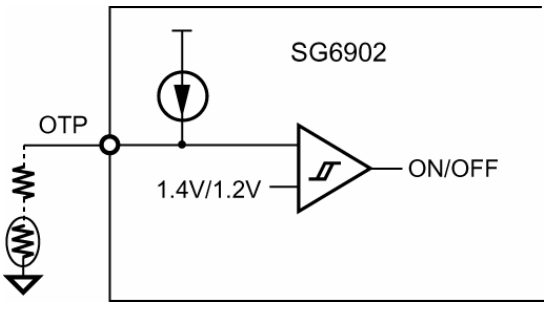


Fig.9 OTP function

Soft Start

During startup of PWM stage, the SS pin will charge an external capacitor with a constant current source. The voltage on FBPWM will be clamped by SS voltage during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.

Gate Drivers

SG6902 output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET.

PCB Layout

Note that SG6902 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6902. A resistor (5 ~ 20Ω) is recommended connecting in series from the OPFC and OPWM to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure10 shows an example of the PCB layout. The *ground trace* connected from the AGND pin of SG6902 to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 1* provides a signal ground. It should be connected directly to the decoupling capacitor V_{DD} and/or to the AGND pin of the SG6902. The *ground trace* 2 shows that the AGND pins should connect to the PFC output capacitor C_O independently. The *ground trace 3* is independently tied from the PGND to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. In order to provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (Beware that it may incorrectly be connected to the ground trace 2). The IMP and ISENSE pins should also be connected directly via the resistors R_2 and R_P to another terminal of R_S. Due to the *ground trace 4 and 5* is PFC and PWM stages Current loop, which should be as short as possible.

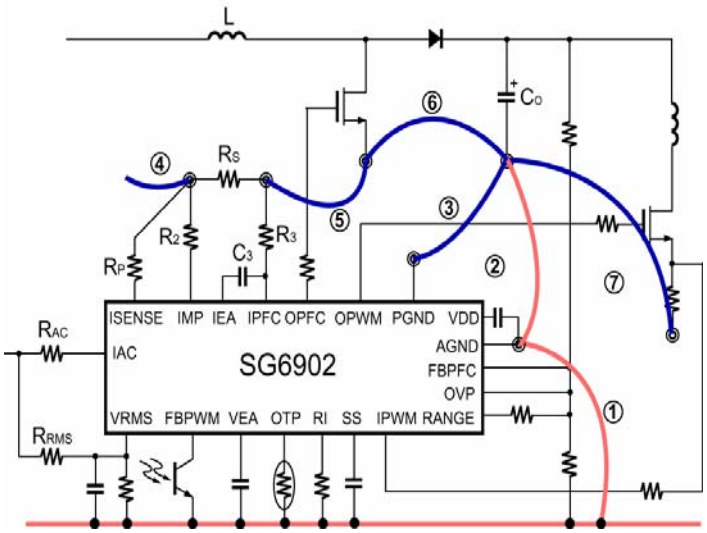
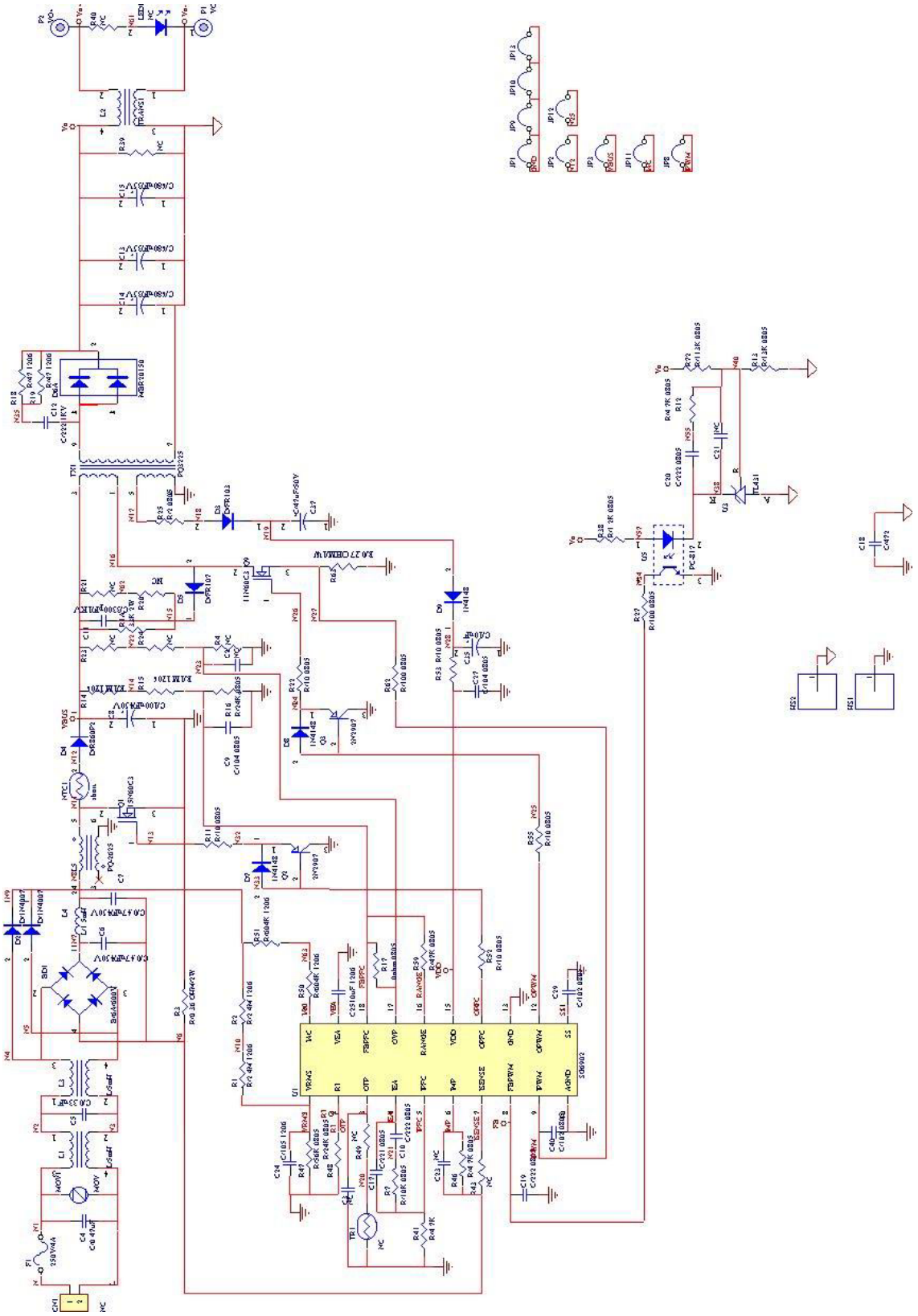


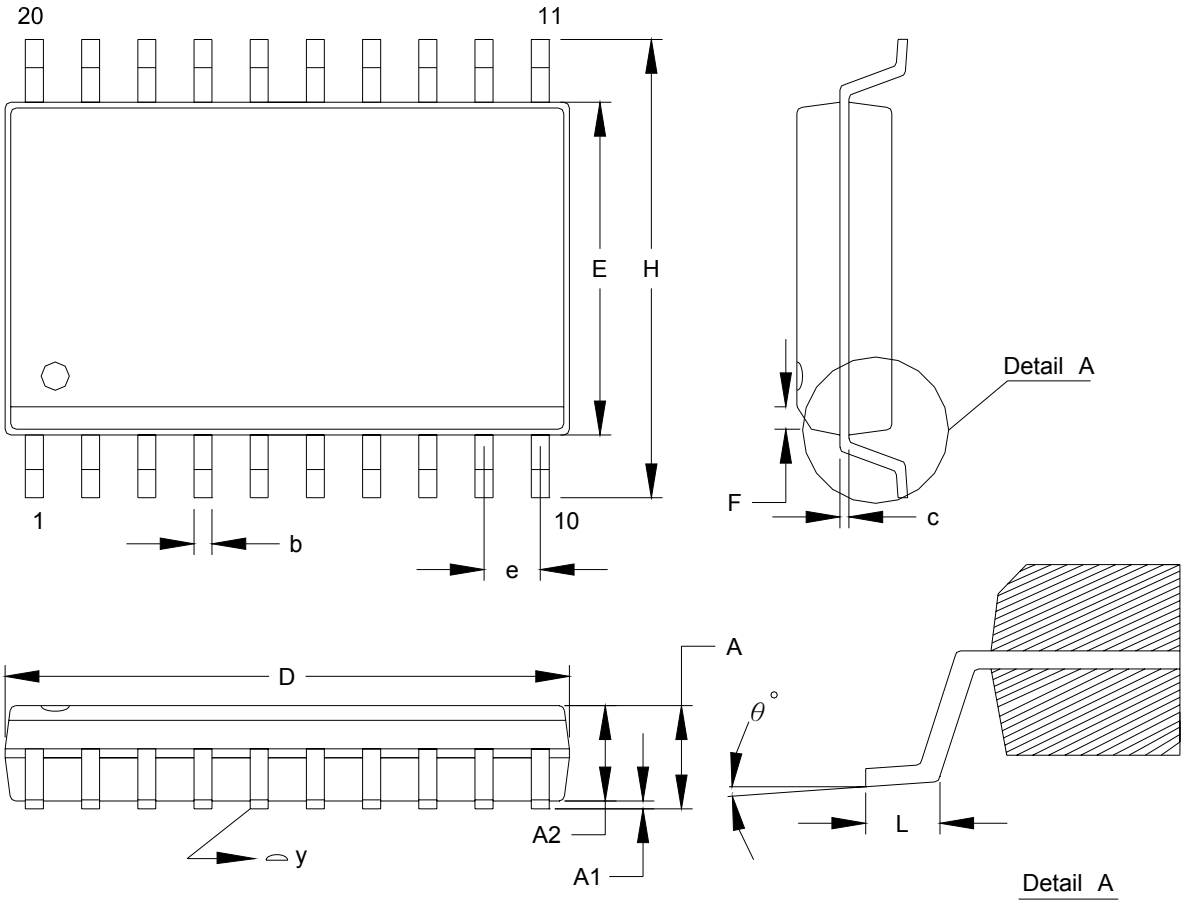
Fig.10 Layout considerations

REFERENCE CIRCUIT



PACKAGE INFORMATION

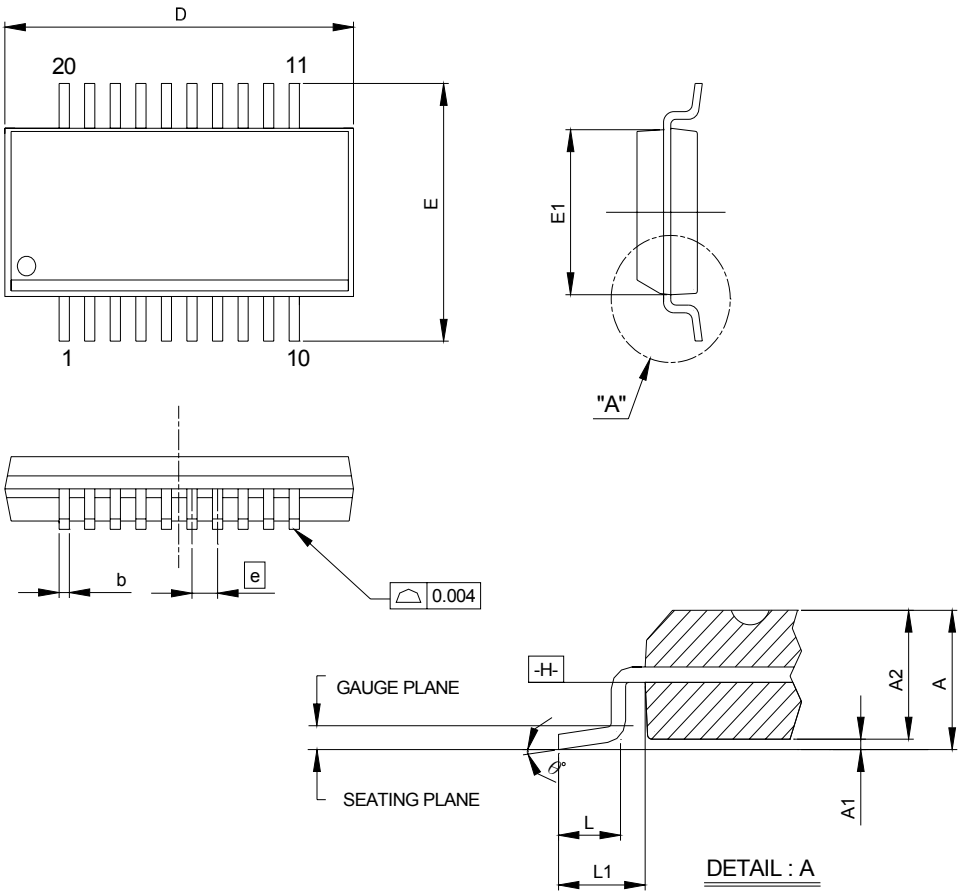
20 PINS – PLASTIC SOP (S)



Dimension:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362		2.642	0.093		0.104
A1	0.101		0.305	0.004		0.012
A2	2.260		2.337	0.089		0.092
b		0.406			0.016	
c		0.203			0.008	
D	12.598		12.903	0.496		0.508
E	7.391		7.595	0.291		0.299
e		1.270			0.050	
H	10.007		10.643	0.394		0.419
L	0.406		1.270	0.016		0.050
F		0.508X45°			0.020X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

20 PINS – SSOP (R)



Dimension

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053	0.064	0.069
A1	0.102		0.254	0.004	0.006	0.010
A2			1.499			0.059
b	0.203		0.305	0.008		0.012
C	0.178		0.254	0.007		0.010
D	8.560	8.661	8.738	0.337	0.341	0.344
E	5.791	5.994	6.198	0.228	0.236	0.244
E1	3.810	3.912	3.988	0.150	0.154	0.157
e	0.635 BASIC			0.025 BASIC		
L	0.406	0.635	1.270	0.016	0.025	0.050
L1	1.041 BASIC			0.041 BASIC		
θ°	0°		8°	0°		8°

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