

Octal bus transceiver with direction pin; 3-state

74LVC245

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- Direct interface with TTL levels
- CMOS low power consumption
- Output drive capability 50 Ω transmission lines @ 85 °C

DESCRIPTION

The 74LVC245 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '245' features an output enable (\overline{OE}) input for easy cascading and a send/receive (DIR) input for direction control. \overline{OE} controls the outputs so that the buses are effectively isolated.

The '245' is identical to the '640' but has true (non-inverting) outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
\overline{OE}	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^\circ\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; B_n to A_n	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	4.1	ns
C_i	input capacitance		5.0	pF
$C_{i/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

where:

f_i = input frequency in MHz; C_L = output load capacity in pF;

f_o = output frequency in MHz; V_{CC} = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC245D	20	SO	plastic	SOT163-1
74LVC245DB	20	SSOP	plastic	SOT339-1
74LVC245PW	20	TSSOP	plastic	SOT360-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	\overline{OE}	output enable input (active LOW)
20	V_{CC}	positive supply voltage

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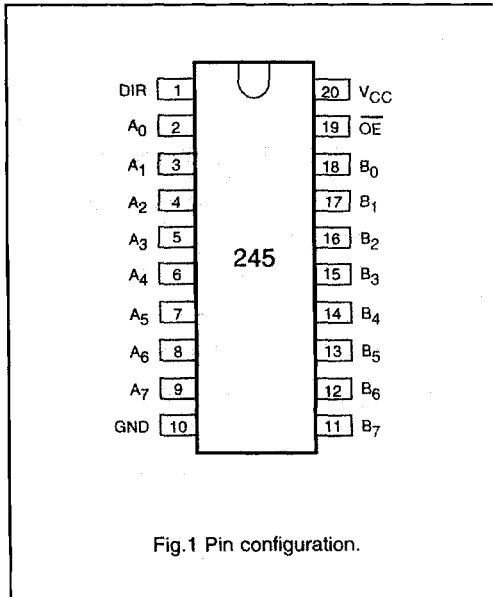


Fig.1 Pin configuration.

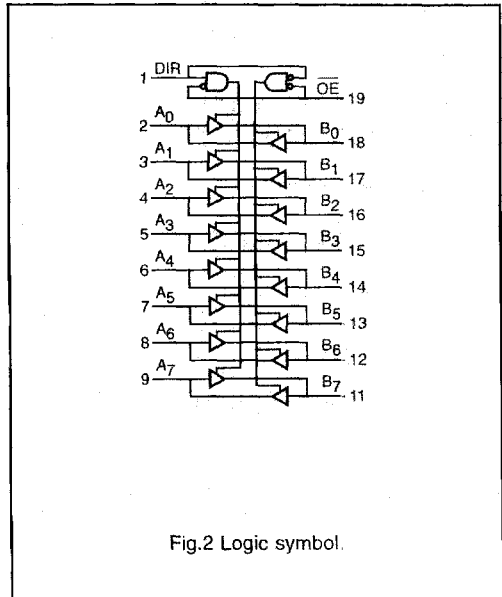


Fig.2 Logic symbol.

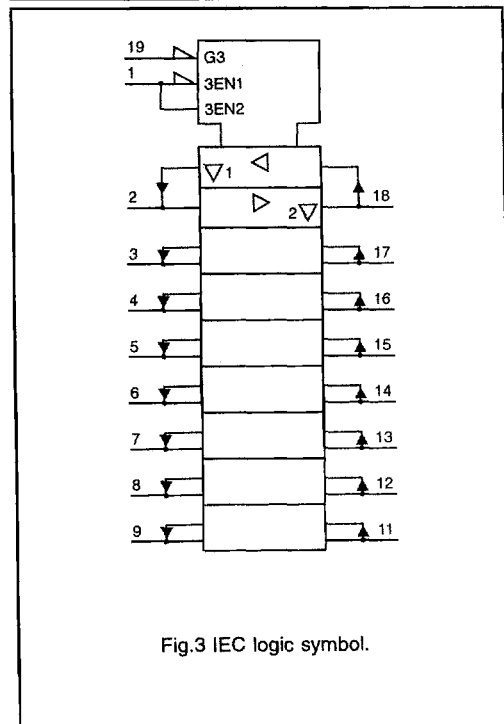


Fig.3 IEC logic symbol.

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DC CHARACTERISTICS FOR 74LVC245

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

 I_{CC} category: MSI**AC CHARACTERISTICS FOR 74LVC245**GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

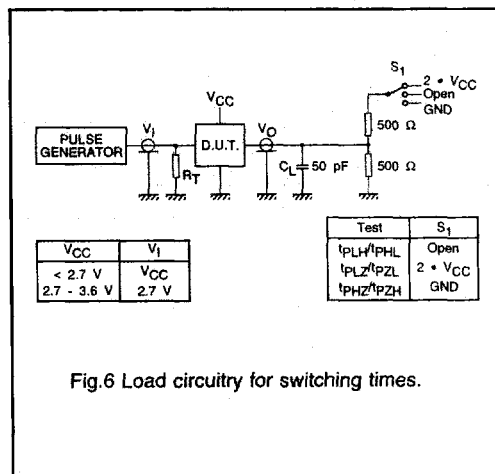
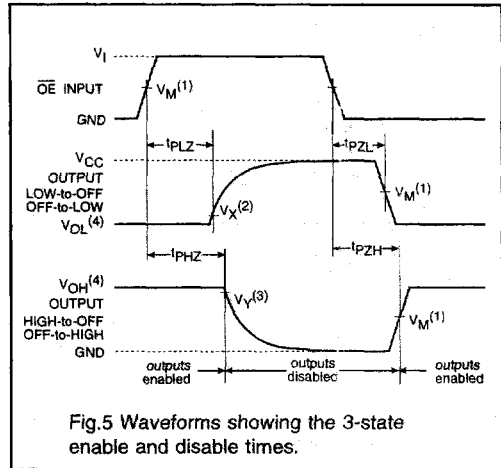
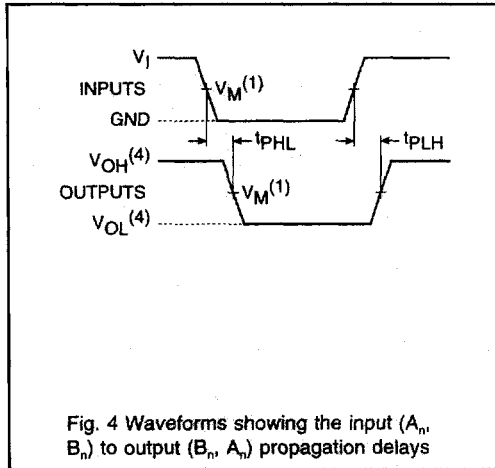
SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	21	–	ns	1.2	Figs 4, 6
	A_n to B_n ; B_n to A_n	1.5	4.6	8.0		2.7	
t_{PZH}/t_{PZL}	3-state output enable time	–	25	–	ns	1.2	Figs 5, 6
	\overline{OE} to A_n ; \overline{OE} to B_n	1.5	5.3	10.0		2.7	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	8.0	–	ns	1.2	Figs 5, 6
	\overline{OE} to A_n ; \overline{OE} to B_n	1.5	4.3	9.0		2.7	
		1.5	4.0*	8.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.* Typical values are measured at $V_{CC} = 3.3$ V.

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AC WAVEFORMS



- Notes:
- $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
 - $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.