Low Distortion, Precision Wide Bandwidth Op Amp

AD9618

1.1 Scope.

This specification covers the requirements for a low distortion, wide bandwidth operational amplifier. Consult the commercial data sheet for theory and applications information.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD9618S(X)/883B
−2	AD9618T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8	8-Pin Ceramic DIP
Z	Z-8	8-Pin Ceramic Flatpack (Gull Wing)

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continous Output Current* . . . . . 70 mA
Junction Temperature . . . . . +175°C
Operating Temperature Range (Case) . . . . . −55°C to +125°C
Storage Temperature Range (Case) . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

*Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA} = 120°C/W for Flatpack
θ_{JC} = 20°C/W for Flatpack
θ_{JA} = 110°C/W for Ceramic DIP
θ_{JC} = 20°C/W for Ceramic DIP

AD9618—SPECIFICATIONS

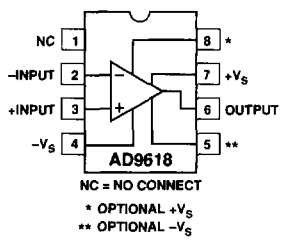
Table 1.

Test	Symbol	Device	Design Limit[1]	Sub Group 1	Sub Group 2	Sub Group 3	Sub Group 4, 6	Sub Group 5	Test Condition[2]	Units
Input Offset Voltage	V_{OS}	−1		−1.1/+2.2					Measured in Respect to Inverting Input	V/°C min/max
		−2		0.0/+1.1						
Offset Voltage TC	V_{OS} TC	All		−4/+25						µV/°C min/max
Input Bias Current Inverting	I_B	−1		−50/+50						µA/°C min/max
Noninverting		−1		−25/+35						
Inverting		−2		−25/+25						
Noninverting		−2		−15/+20						
Input Bias Current TC Inverting	I_B TC	All		−50/+130						nA/°C min/max
Noninverting		All		−50/+125						
Common-Mode Input Range	CMIR	All		±1.4	±1.0	±1.4			A_V = 1	V min
Common-Mode Rejection Ratio	CMRR	All					48, 50	44	V_{IN} = ±0.25 V	dB min
Power Supply Rejection Ratio	PSRR	All					50	50	ΔV_S = ±5%	dB min
Output Current	I_{OUT}	All		60	60	50			50 Ω Load	mA min
Output Voltage Swing	V_{OUT}	All		−3.4	−3.4	−3.4				V max
				+3.4	+3.4	+3.4				V min
Small Signal Bandwidth	SSBW	All					130	130	$V_{OUT} \leq$ 2 V p-p	MHz min
Large Signal Bandwidth	LSBW	All	120						V_{OUT} = 5 V p-p	MHz min
Output Peaking		All					0.4		<50 MHz; T = T_{MIN} to +25°C	dB max
								0.7	<50 MHz; T = T_{MAX}	
							0.6		>50 MHz; T = T_{MIN} to +25°C	
								1.2	>50 MHz; T = T_{MAX}	
Output Rolloff		All					1.2	1.2	<75 MHz	dB max
Second Harmonic Distortion	HD_2	All	−75						V_{OUT} = 2 V p-p, F = 4.3 MHz	dBc max
			−55						V_{OUT} = 2 V p-p, F = 20 MHz	dBc max
							−43	−43	V_{OUT} = 2 V p-p, F = 60 MHz	dBc max
Third Harmonic Distortion	HD_3	All	−77						V_{OUT} = 2 V p-p, F = 4.3 MHz	dBc max
			−62						V_{OUT} = 2 V p-p, F = 20 MHz	dBc max
							−54	−54	2 V p-p; 60 MHz	dBc max
Slew Rate	t_{SR}	All	1400						V_{OUT} = 4 V Step	V/µs min
Rise/Fall Time	$t_{R/F}$	All	2.6						V_{OUT} = 2 V Step	ns max
			2.8						V_{OUT} = 5 V Step, +25°C to T_{MAX}	ns max
			3.1						V_{OUT} = 5 V Step, T = T_{MIN}	ns max
Overshoot Amplitude		All	10						V_{OUT} = 2 V Step	% max

Test	Symbol	Device	Design Limit[1]	Sub Group 1	Sub Group 2	Sub Group 3	Sub Group 4, 6	Sub Group 5	Test Condition[2]	Units
Settling Time	t_{SL}	All	15						2 V Step; to 0.1%	ns max
			23						2 V Step; to 0.02%	nsmax
			16						4 V Step; to 0.1%	ns max
			24						4 V Step; to 0.02%	ns max
V_{CC} Supply Current	$+I_S$	All		43	43	43			V_{CC} = +5 V	mA max
V_{EE} Supply Current	$-I_S$	All		43	43	43			V_{EE} = −5 V	mA max

NOTES
[1]Indicates specification which is guaranteed but not tested. Value shown is over full temperature range.
[2]Unless otherwise noted, A_V = +10; $\pm V_S$ = ±5 V; R_F = 1,000 Ω; R_{LOAD} = 100 Ω.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).