



# 4-Bit Up/Down Counter (with Asynchronous Clear)

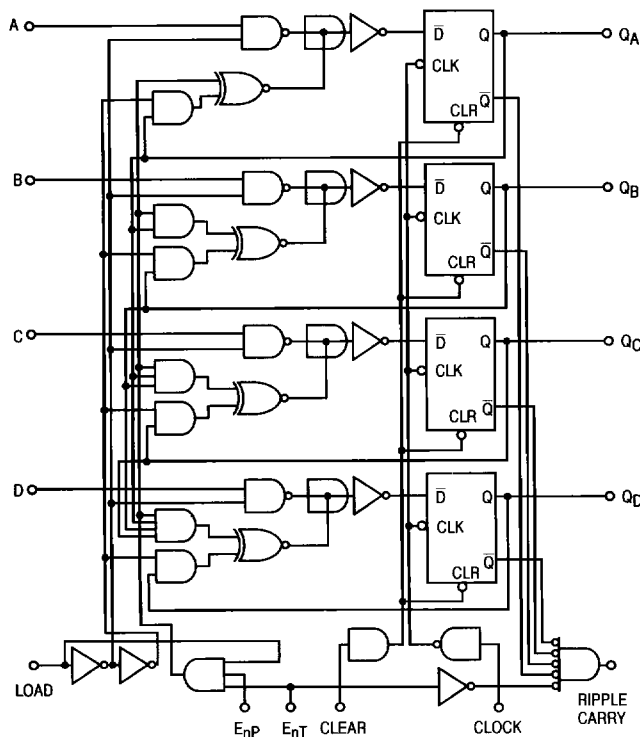
ELECTRICALLY TESTED PER:  
MIL-M-38510/31504

The 'LS161A is a high-speed 4-bit synchronous counter. It is edge-triggered, synchronously presettable, and cascadable with MSI building blocks for counting, memory addressing, frequency division and other applications. The 'LS161A can count modulo 10 (BCD).

The 'LS161A has an asynchronous Master Reset (Clear) input that overrides, and is independent of the clock and all other control inputs.

- Synchronous Counting and Loading
- Two Count Enable Inputs For High-Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Typical Count Rate of 35 MHz

LOGIC DIAGRAM



## Military 54LS161A



AVAILABLE AS:

- 1) JAN: JM38510/31504BXA
- 2) SMD: 7600801
- 3) 883: 54LS161A/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
CLR	1	1	2	GND
CLK	2	2	3	VCC
A	3	3	4	VCC
B	4	4	5	VCC
C	5	5	7	VCC
D	6	6	8	VCC
E <sub>nP</sub>	7	7	9	VCC
GND	8	8	10	GND
Ld	9	9	12	VCC
E <sub>nT</sub>	10	10	13	VCC
Q <sub>D</sub>	11	11	14	OPEN
Q <sub>C</sub>	12	12	15	OPEN
Q <sub>B</sub>	13	13	17	OPEN
Q <sub>A</sub>	14	14	18	OPEN
RC	15	15	19	OPEN
VCC	16	16	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

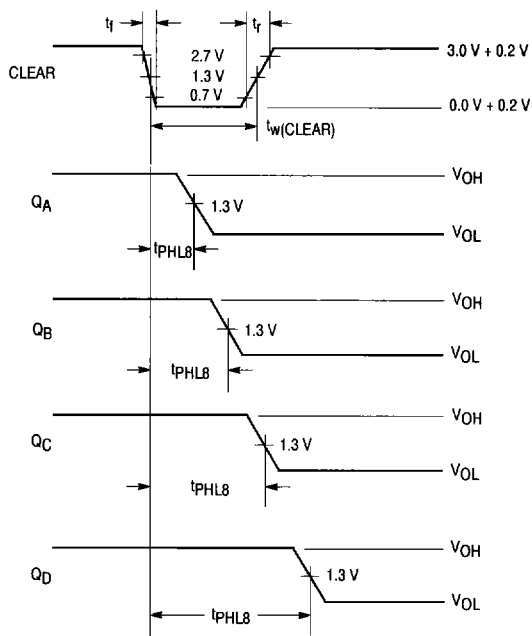
### MODE SELECT TABLE

Ld	E <sub>nT</sub>	E <sub>nP</sub>	Action on the Rising Clock Edge (↑)
X	X	X	Reset (Clear)
L	X	X	Load (D <sub>n</sub> -Q <sub>n</sub> )
H	H	H	Count (Increment)
H	L	X	No Change (Hold)
H	X	L	No Change (Hold)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

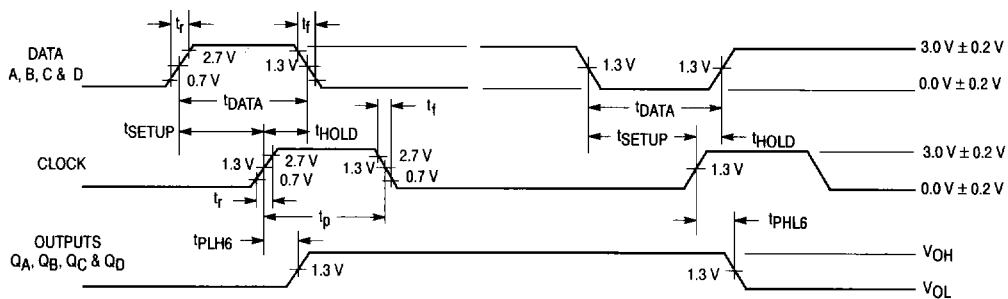
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VOLTAGE WAVEFORM 1

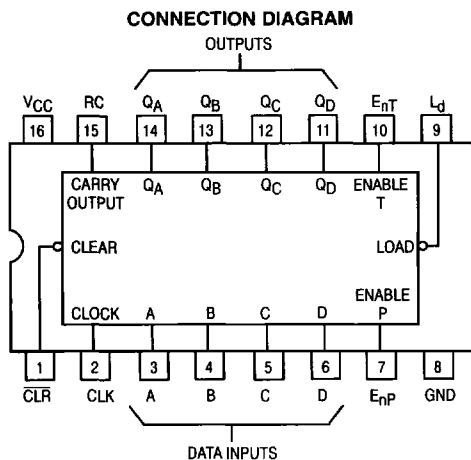
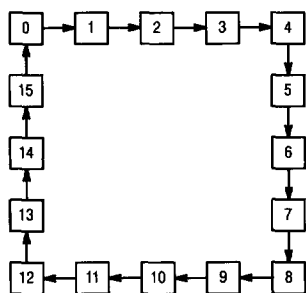
**NOTE:**

The Clear pulse generator has the following characteristics:  
 $V_{gen} = 3.0\text{ V}$ ,  $t_r \leq 15\text{ ns}$ ,  $t_f \leq 6.0\text{ ns}$ ,  $t_w(\text{Clear}) = 20\text{ ns}$ .

VOLTAGE WAVEFORM 2

**NOTE:**

The data pulse generator has the following characteristics:  
 $V_{gen} = 3.0\text{ V}$ ,  $t_r \leq 15\text{ ns}$ ,  $t_f \leq 6.0\text{ ns}$ ,  $t_{DATA} = 30\text{ ns}$ ,  $t_{SETUP} = 20\text{ ns}$ ,  
 $t_{HOLD} = 10\text{ ns}$ .

**STATE DIAGRAM****LOGIC EQUATIONS**

Count Enable =  $E_{nP} \cdot E_{nT} \cdot L_d$   
 RC for 'LS161A =  $E_{nT} \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$   
 Preset =  $L_d \cdot CLK + (\text{rising clock edge})$   
 Reset =  $\overline{CLR}$

Pin Names		Loading (Note b)	
		HIGH	LOW
Load	Parallel Enable (Active LOW)	1.0 U.L.	0.5 U.L.
A-D	Parallel Inputs (Data Inputs)	0.5 U.L.	0.25 U.L.
$E_{nP}$	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
$E_{nT}$	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CLK	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{CLR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.25 U.L.
$Q_A$ - $Q_D$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
RC	Terminal Count (Ripple Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

**NOTES:**

- a. One TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

**FUNCTIONAL DESCRIPTION**

The 'LS161A is a 4-bit synchronous counter with a synchronous Parallel Enable (Load) feature. The counter consists of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CLK). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs – Parallel Enable ( $L_d$ ), Count Enable Parallel ( $E_{nP}$ ) and Count Enable Trickle ( $E_{nT}$ ) – select the mode of operation as shown in the table below. The Count Mode is enabled when the  $E_{nP}$ ,  $E_{nT}$ , and  $L_d$  inputs are HIGH. When the  $L_d$  is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the  $E_{nP}$  or  $E_{nT}$  can be used to inhibit the count sequence. With the  $L_d$  held HIGH, a LOW on either the  $E_{nP}$  or  $E_{nT}$  inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing

output states to be retained. The AND feature of the two Count Enable inputs ( $E_{nP} \cdot E_{nT}$ ) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

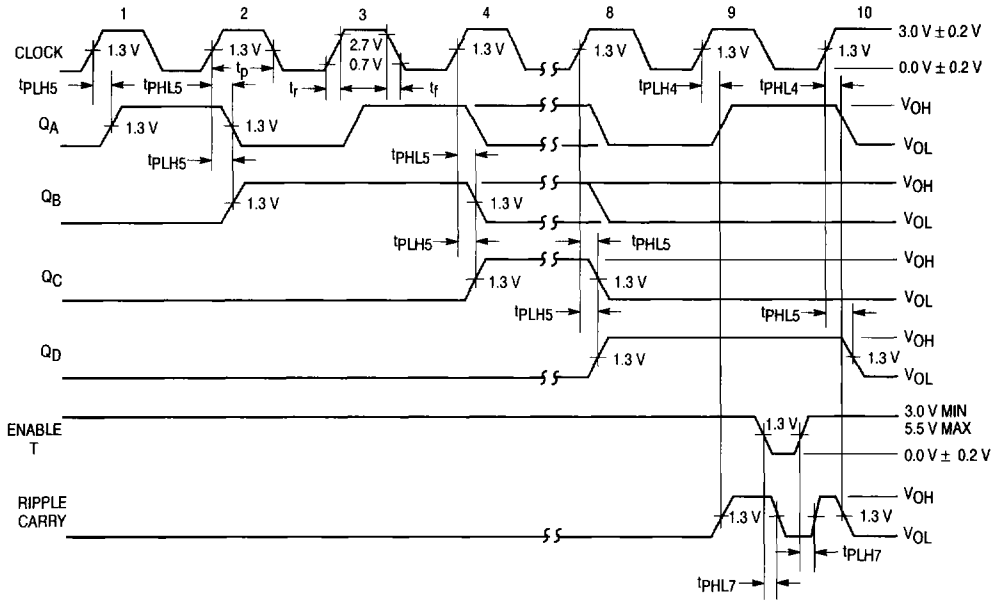
The Terminal Count (RC) output is HIGH when the Counter Enable Trickle ( $E_{nT}$ ) input is HIGH while the counter is in its maximum count state (HLLH for BCD counters, HHHH for Binary counters). Note that RC is fully decoded and will, therefore, be HIGH only for one count state.

The 'LS161A can count modulo 16 following a binary sequence. It can generate an RC when the  $E_{nT}$  input is HIGH while the counter is in the state 15 (HHHH). From this state it can increment to state 0 (LLLL).

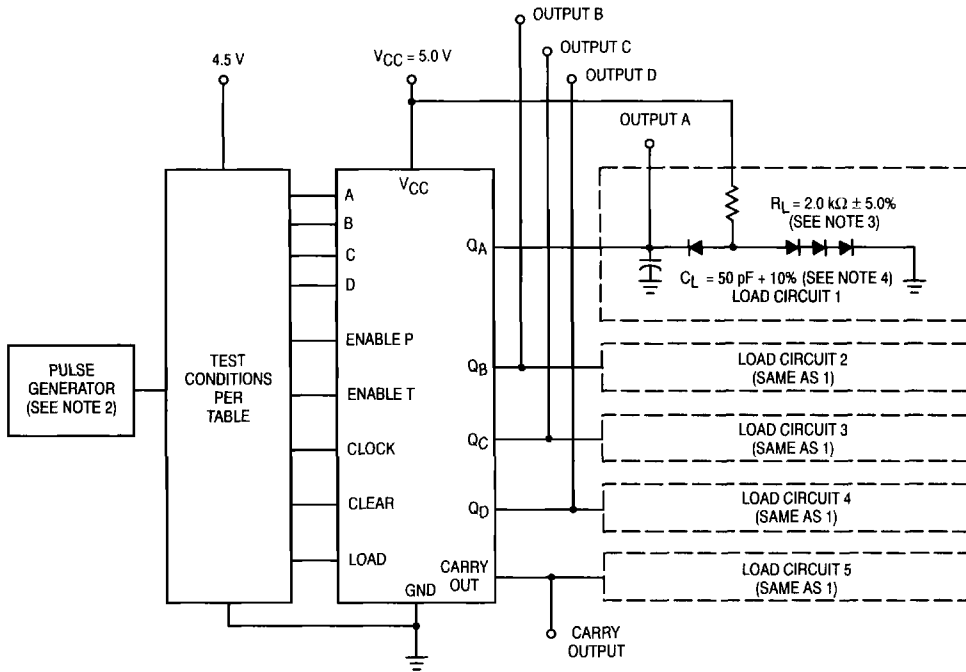
The Master Reset ( $\overline{MR}$ ) of the 'LS161A is asynchronous. When the  $\overline{MR}$  is LOW, it overrides all other input conditions and sets the outputs LOW. The  $\overline{MR}$  pin should never be left open. If not used, the  $\overline{MR}$  pin should be tied through a resistor to  $V_{CC}$  or to a gate output which is permanently set to a HIGH logic level.

54LS161A

VOLTAGE WAVEFORM 3



TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-186

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## 54LS161A

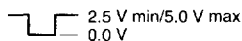
Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, CR = 4.5 V, E <sub>NP</sub> = open, CLK = (See Note 7), V <sub>IH</sub> = 2.0 V, E <sub>NT</sub> = 2.0 V, L <sub>d</sub> = GND.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IL</sub> = 0.7 V, L <sub>d</sub> = GND, CLK = (See Note 7), CR = 4.5 V, E <sub>NP</sub> = open, E <sub>NT</sub> = 0.7 V.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, (other inputs are open).
I <sub>IH</sub>	Logical "1" Input Current		40		40		40	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V (other inputs are open), (CLK, E <sub>NT</sub> & L <sub>d</sub> ) are open.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V (other inputs are open), (CLK, E <sub>NT</sub> & L <sub>d</sub> ) are open.
I <sub>IHH</sub>	Logical "1" Input Current		200		200		200	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V (other inputs are open).
I <sub>IL</sub>	Logical "0" Input Current	-150	-380	-150	-380	-150	-380	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, L <sub>d</sub> /E <sub>NT</sub> = 4.5 V (other inputs are open).
I <sub>ILL</sub>	Logical "0" Input Current	0	-100	0	-100	0	-100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V (other inputs are open), L <sub>d</sub> = GND or open.
I <sub>IL</sub>	Logical "0" Input Current	-160	-400	-160	-400	-160	-400	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V (other inputs are open), E <sub>NP</sub> /E <sub>NT</sub> = 4.5 V.
I <sub>ILL</sub>	Logical "0" Input Current	-300	-760	-300	-760	-300	-760	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, L <sub>d</sub> & E <sub>NP</sub> = 4.5 V, other inputs are open.
I <sub>OS</sub>	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V (other inputs are open), L <sub>d</sub> = GND, V <sub>OUT</sub> = GND, CLK = (See Note 7), CR = 4.5 V, E <sub>NP</sub> /E <sub>NT</sub> = open.
I <sub>CCH</sub>	Power Supply Current Off		31		31		31	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs), L <sub>d</sub> = 5.5 V or GND.
I <sub>CCL</sub>	Power Supply Current Off		32		32		32	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs), CLK = GND or 5.5 V.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.

## 54LS161A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL4</sub> t <sub>PHL4</sub>	Propagation Delay /Data-Output Clock to Carry Out	3.0 —	40 35	3.0 —	56 51	3.0 —	56 51	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH4</sub> t <sub>PLH4</sub>	Propagation Delay /Data-Output Clock to Carry Out	3.0 —	40 35	3.0 —	56 51	3.0 —	56 51	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL5</sub> t <sub>PHL5</sub>	Propagation Delay /Data-Output Clock to Q <sub>n</sub>	3.0 —	32 27	3.0 —	45 40	3.0 —	45 40	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH5</sub> t <sub>PLH5</sub>	Propagation Delay /Data-Output Clock to Q <sub>n</sub>	3.0 —	29 24	3.0 —	41 36	3.0 —	41 36	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL6</sub> t <sub>PHL6</sub>	Propagation Delay /Data-Output Clock to Q <sub>n</sub>	3.0 —	32 27	3.0 —	48 43	3.0 —	48 43	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH6</sub> t <sub>PLH6</sub>	Propagation Delay /Data-Output Clock to Q <sub>n</sub>	3.0 —	29 24	3.0 —	42 37	3.0 —	42 37	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL7</sub> t <sub>PHL7</sub>	Propagation Delay /Data-Output E <sub>nT</sub> to Carry Out	3.0 —	19 14	3.0 —	28 23	3.0 —	28 23	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PLH7</sub> t <sub>PLH7</sub>	Propagation Delay /Data-Output E <sub>nT</sub> to Carry Out	3.0 —	19 14	3.0 —	28 23	3.0 —	28 23	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
t <sub>PHL8</sub> t <sub>PHL8</sub>	Propagation Delay /Data-Output Clear to Q <sub>n</sub>	3.0 —	33 28	3.0 —	46 41	3.0 —	46 41	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.
f <sub>MAX</sub> f <sub>MAX</sub>	Maximum Clock Frequency	22 25		22		22		MHz	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF.

## NOTES:

- Voltage measurements are made with respect to ground terminal.
- The pulse generator has the following characteristics:  
V<sub>GEN</sub> = 3.0 V, t<sub>r</sub> = 6.0 ns, t<sub>f</sub> = 6.0 ns, t<sub>p</sub> = 0.5 μs, PRR ≤ 1.0 MHz, Z<sub>OUT</sub> = 50 Ω.
- All diodes are 1N3064 or equivalent.
- C<sub>L</sub> = 50 pF ± 10%, including scope probe and jig capacitance.
- f<sub>MAX</sub>: t<sub>r</sub> = t<sub>f</sub> ≤ 6.0 ns.
- The limits specified for C<sub>L</sub> = 15 pF are guaranteed but not tested.
- Apply one pulse prior to measurement as follows:



or

