# TC554161FTL/TRL-70/85/10

**PRELIMINARY**

## SILICON GATE CMOS

## 262,144 WORD x 16 BIT STATIC RAM

### Description

The TC554161FTL/TRL is a 4,194,304 bit CMOS static random access memory organized as 262,144 words by 16 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 100μA (max.). The TC554161FTL/TRL has two control inputs. A chip enable input ($\overline{CE}$) allows for device selection and data retention control, while an output enable input ($\overline{OE}$) provides fast memory access. Byte access is supported by upper and lower byte controls. The TC554161FTL/TRL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required. The TC554161FTL/TRL is offered in a 54-pin thin small outline plastic package (forward type, reverse type).

### Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 100μA (max.)
- Single 5V power supply
- Access time (max.)

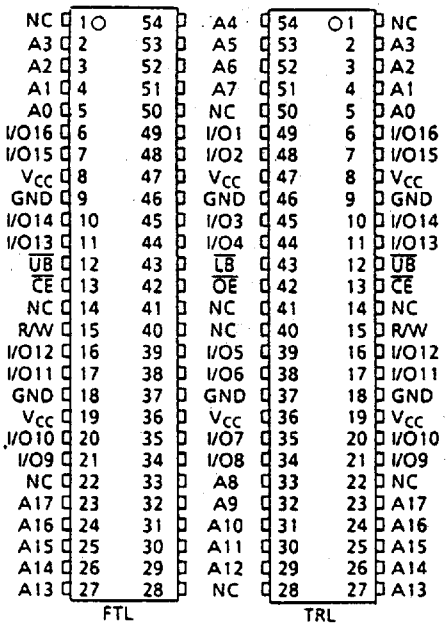
| | TC554161FTL/TRL | | |
|---|---|---|---|
| | -70 | -85 | -10 |
| Access Time | 70ns | 85ns | 100ns |
| $\overline{CE}$ Access Time | 70ns | 85ns | 100ns |
| $\overline{OE}$ Access Time | 35ns | 45ns | 50ns |

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package TC554161FTL : TSOP54-P-400
  TC554161TRL : TSOP54-P-400A

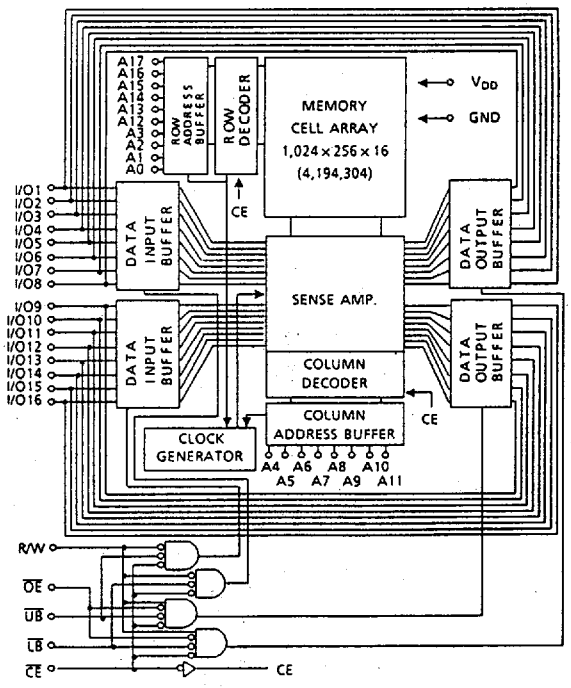
### Pin Names

| | |
|---|---|
| A0 ~ A17 | Address Inputs |
| I/O1 ~ I/O16 | Data Input/Output |
| $\overline{CE}$ | Chip Enable Input |
| R/W | Read/Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{LB}$, $\overline{UB}$ | Data Byte Control Input |
| $V_{DD}$ | Power (+5V) |
| GND | Ground |
| NC | No Connection |

### Pin Connection (Top View)



## Block Diagram




## Operating Mode

| MODE \ PIN | CE | OE | R/W | LB | UB | I/O1 ~ I/O8 | I/O9 ~ I/O16 | POWER |
|---|---|---|---|---|---|---|---|---|
| Read | L | L | H | L | L | Output | Output | $I_{DDO}$ |
| | | | | H | L | High Impedance | Output | $I_{DDO}$ |
| | | | | L | H | Output | High Impedance | $I_{DDO}$ |
| Write | L | * | L | L | L | Input | Input | $I_{DDO}$ |
| | | | | H | L | High Impedance | Input | $I_{DDO}$ |
| | | | | L | H | Input | High Impedance | $I_{DDO}$ |
| Output Deselect | L | H | H | * | * | High Impedance | High Impedance | $I_{DDO}$ |
| | L | * | * | H | H | | | |
| Standby | H | * | * | * | * | High Impedance | High Impedance | $I_{DDS}$ |

* H or L

## Maximum Ratings

| SYMBOL | ITEM | RATING | UNIT |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -0.3 ~ 7.0 | V |
| $V_{IN}$ | Input Voltage | -0.3* ~ 7.0 | V |
| $V_{I/O}$ | Input and Output Voltage | -0.5* ~ $V_{DD}$ + 0.5 | V |
| $P_D$ | Power Dissipation | 0.6 | W |
| $T_{SOLDER}$ | Soldering Temperature • Time | 260 • 10 | °C • sec |
| $T_{STRG}$ | Storage Temperature | -55 ~ 150 | °C |
| $T_{OPR}$ | Operating Temperature | 0 ~ 70 | °C |

* -3.0V with a pulse width of 30ns

### DC Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | – | $V_{DD}$ + 0.3 | |
| $V_{IL}$ | Input Low Voltage | -0.3* | – | 0.8 | |
| $V_{DH}$ | Data Retention Supply Voltage | 2.0 | – | 5.5 | |

* -3.0V with a pulse width of 30ns

### DC Characteristics (Ta = 0 ~ 70°C, $V_{DD}$ = 5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 ~ $V_{DD}$ | | | – | – | ±1.0 | μA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE}$ = $V_{IH}$ or R/W = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$<br>$V_{OUT}$ = 0 ~ $V_{DD}$ | | | – | – | ±1.0 | μA |
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | | | -1.0 | – | – | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | | | 2.1 | – | – | mA |
| $I_{DDO1}$ | Operating Current | $\overline{CE}$ = $V_{IL}$, $I_{OUT}$ = 0mA<br>Other Inputs = $V_{IH}/V_{IL}$ | $t_{cycle}$ | Min. | – | – | 100 | mA |
| | | | | 1μs | – | 15 | – | |
| $I_{DDO2}$ | | $\overline{CE}$ = 0.2V, $I_{OUT}$ = 0mA<br>Other Inputs = $V_{IH}/V_{IL}$ | $t_{cycle}$ | Min. | – | – | 90 | |
| | | | | 1μs | – | 10 | – | |
| $I_{DDS1}$ | Standby Current | $\overline{CE}$ = $V_{IH}$, Other Inputs = $V_{IH}/V_{IL}$ | | | – | – | 3 | mA |
| $I_{DDS2}$ | | $\overline{CE}$ = $V_{DD}$ - 0.2V<br>$V_{DD}$ = 2.0V ~ 5.5V | | | – | – | 100 | μA |

### Capacitance* (Ta = 25°C, f = 1.0MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = GND | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = GND | 10 | |

*This parameter is periodically sampled and is not 100% tested.

## AC Characteristics (Ta = 0 ~ 70°C, $V_{DD}$ = 5V±10%)

### Read Cycle

| SYMBOL | PARAMETER | TC554161FTL/TRL | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | -70 | | -85 | | -10 | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{RC}$ | Read Cycle Time | 70 | – | 85 | – | 100 | – | ns |
| $t_{ACC}$ | Address Access Time | – | 70 | – | 85 | – | 100 | |
| $t_{CO}$ | $\overline{CE}$ Access Time | – | 70 | – | 85 | – | 100 | |
| $t_{OE}$ | $\overline{OE}$ Access Time | – | 35 | – | 45 | – | 50 | |
| $t_{BA}$ | $\overline{UB}$, $\overline{LB}$ Access Time | – | 35 | – | 45 | – | 50 | |
| $t_{OH}$ | Output Data Hold Time from Address Change | 10 | – | 10 | – | 10 | – | |
| $t_{COE}$ | Output Enable Time from $\overline{CE}$ | 10 | – | 10 | – | 10 | – | |
| $t_{OEE}$ | Output Enable Time from $\overline{OE}$ | 5 | – | 5 | – | 5 | – | |
| $t_{BE}$ | Output Enable Time from $\overline{UB}$, $\overline{LB}$ | 5 | – | 5 | – | 5 | – | |
| $t_{OD}$ | Output Disable Time from $\overline{CE}$ | – | 25 | – | 30 | – | 35 | |
| $t_{ODO}$ | Output Disable Time from $\overline{OE}$ | – | 25 | – | 30 | – | 35 | |
| $t_{BD}$ | Output Disable Time from $\overline{UB}$, $\overline{LB}$ | – | 25 | – | 30 | – | 35 | |

### Write Cycle

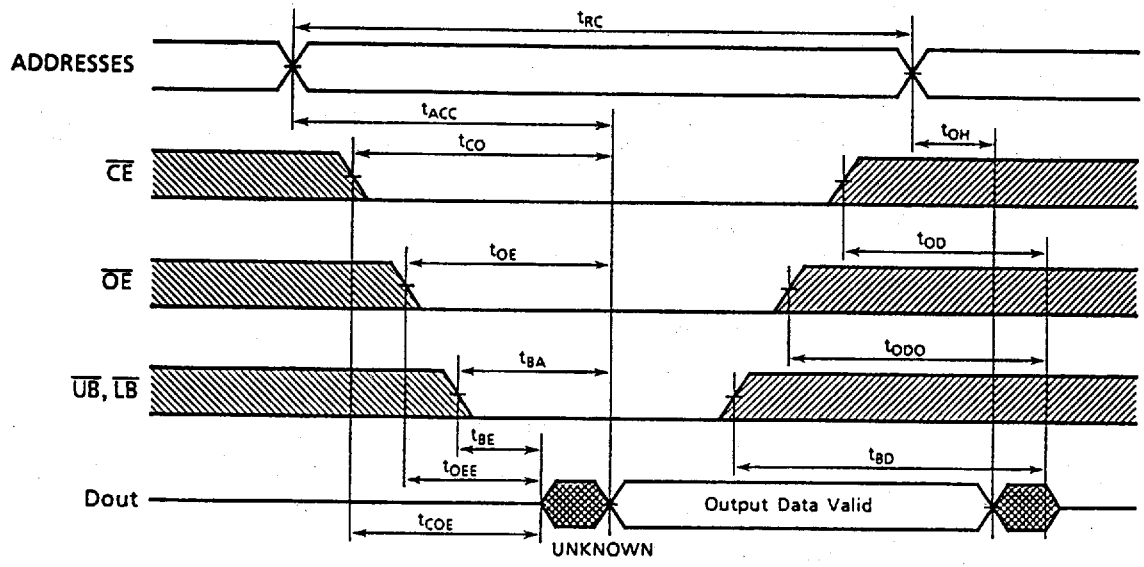
| SYMBOL | PARAMETER | TC554161FTL/TRL | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | -70 | | -85 | | -10 | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{WC}$ | Write Cycle Time | 70 | – | 85 | – | 100 | – | ns |
| $t_{WP}$ | Write Pulse Width | 50 | – | 55 | – | 60 | – | |
| $t_{CW}$ | Chip Enable to End of Write | 60 | – | 70 | – | 80 | – | |
| $t_{BW}$ | $\overline{UB}$, $\overline{LB}$ Enable to End of Write | 50 | – | 55 | – | 60 | – | |
| $t_{AS}$ | Address Setup Time | 0 | – | 0 | – | 0 | – | |
| $t_{WR}$ | Write Recovery Time | 0 | – | 0 | – | 0 | – | |
| $t_{DS}$ | Data Setup Time | 30 | – | 35 | – | 40 | – | |
| $t_{DH}$ | Data Hold Time | 0 | – | 0 | – | 0 | – | |
| $t_{OEW}$ | Output Enable Time from R/W | 5 | – | 5 | – | 5 | – | |
| $t_{ODW}$ | Output Disable Time from R/W | – | 25 | – | 30 | – | 35 | |

### AC Test Conditions

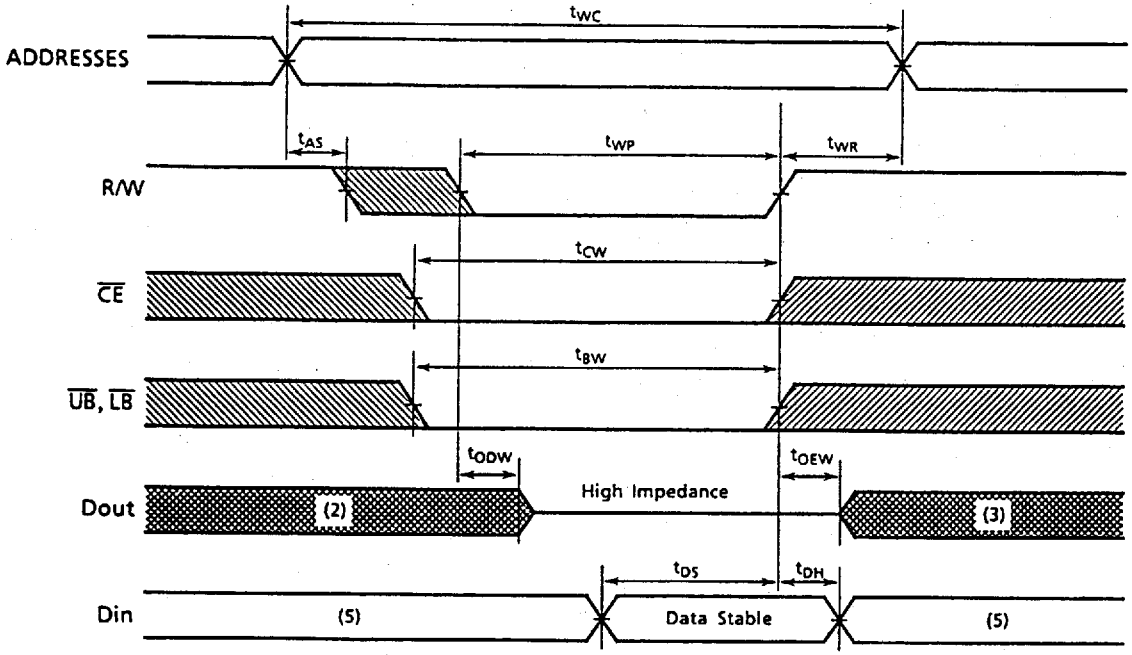
| | |
|---|---|
| Input Pulse Levels | 2.4V/0.6V |
| Input Pulse Rise and Fall Time | 5ns |
| Input Timing Measurement Reference Levels | 1.5V |
| Output Timing Measurement Reference Levels | 1.5V |
| Output Load | 1 TTL Gate and $C_L$ = 100pF |

## Timing Waveforms

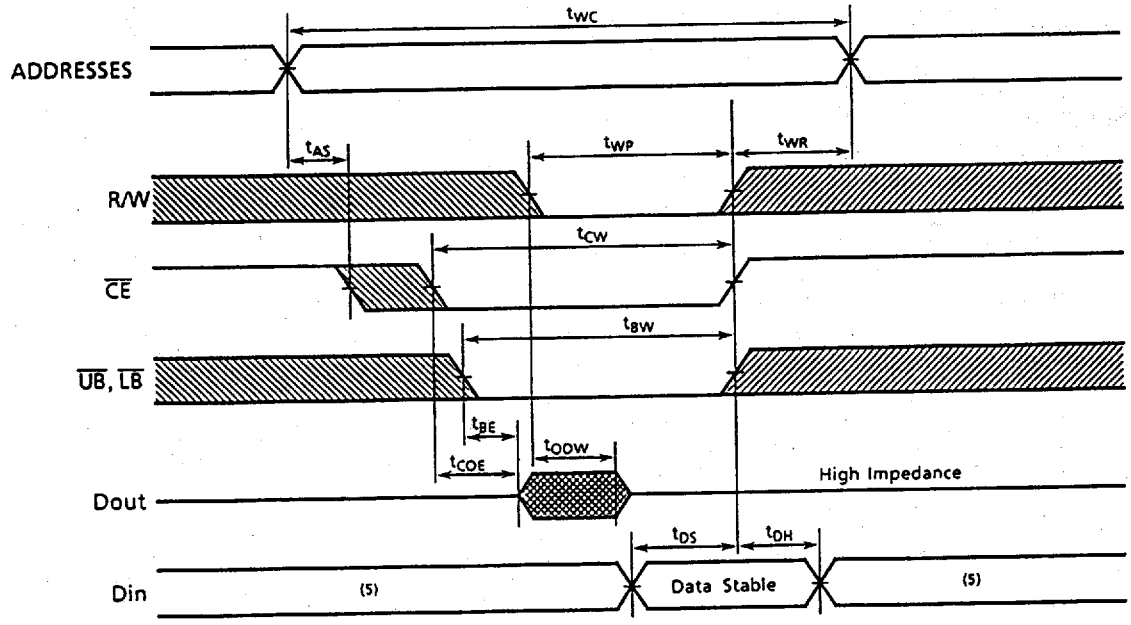
### Read Cycle (1)



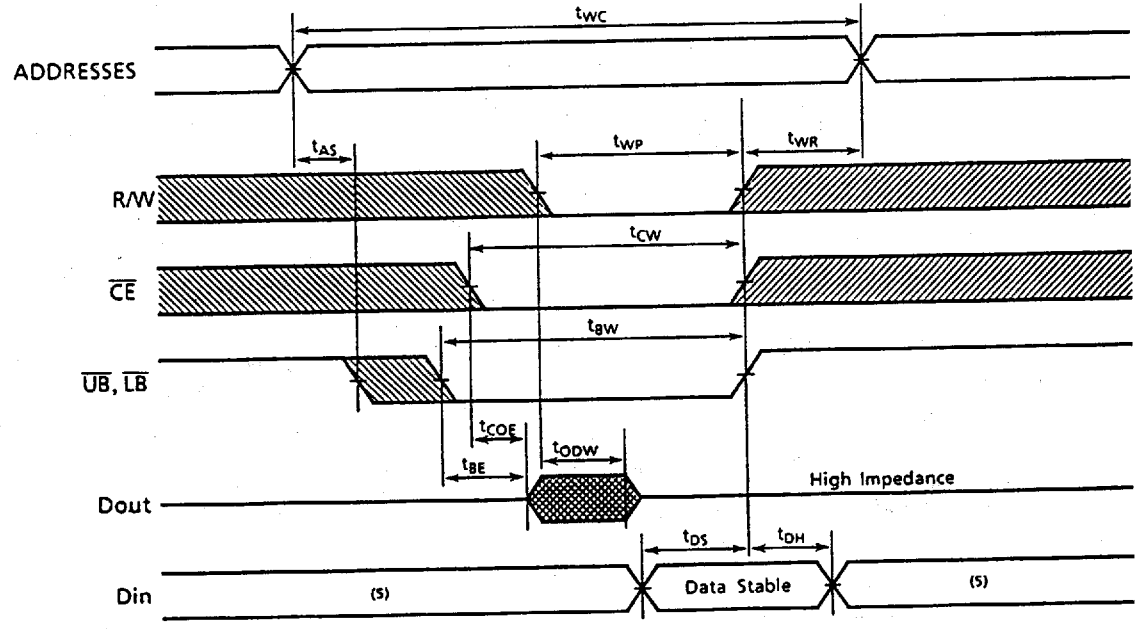

### Write Cycle 1 (4) (R/W Controlled Write)



**Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)**




**Write Cycle 3 [4] ($\overline{UB}$, $\overline{LB}$ Controlled Write)**



Notes:

1. R/W is high for read cycles.

2. If the $\overline{CE}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.

3. If the $\overline{CE}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.

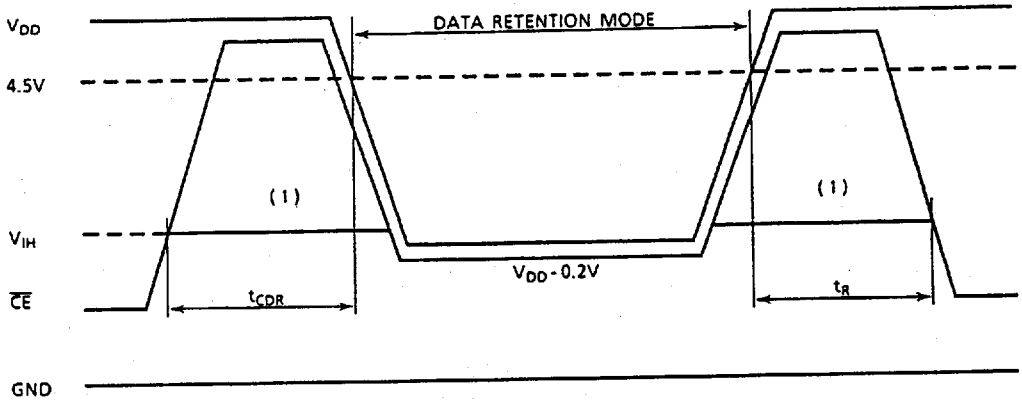
4. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.

5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

**Data Retention Characteristics (Ta = 0 ~ 70°C)**

| SYMBOL | PARAMETER | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DH}$ | Data Retention Supply Voltage | | 2.0 | – | 5.5 | V |
| $I_{DDS2}$ | Standby Current | $V_{DH}$ = 3.0V | – | – | 50 | µA |
| | | $V_{DH}$ = 5.5V | – | – | 100 | |
| $t_{CDR}$ | Chip Deselect to Data Retention Mode | | 0 | – | – | ns |
| $t_R$ | Recovery Time | | 5 | – | – | ms |

**$\overline{CE}$ Controlled Data Retention Mode**




Note:

1. If the $V_{IH}$ of $\overline{CE}$ is 2.2V in operation, during the period that the $V_{DD}$ voltage is going down from 4.5V to 2.4V, $I_{DDS1}$ current flows.