16-BIT 200-KSPS SERIAL CMOS SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **200-kHz Min Sampling Rate**
- **4 V, 5 V, 10 V, ±3.33 V, ±5 V, and ±10 V Input Ranges**
- **86-dB SINAD With 20-kHz Input**
- **±2.0 LSB INL**
- **DNL: 16-Bits No Missing Codes**
- **Six Specified Input Ranges**
- **Serial Output**
- **5-V Supply**
- **Pin-Compatible With ADS7808/09 (Low Speed) and 12-Bit ADS8508**
- **Uses Internal or External Reference**
- **60-mW Typ Power Dissipation at 200 KSPS**
- **20-Pin SO and 28-Pin SSOP Packages**
- **Simple DSP Interface**

APPLICATIONS

- **Industrial Process Control**
- **Data Acquisition Systems**
- **Digital Signal Processing**
- **Medical Equipment**
- **Instrumentation**

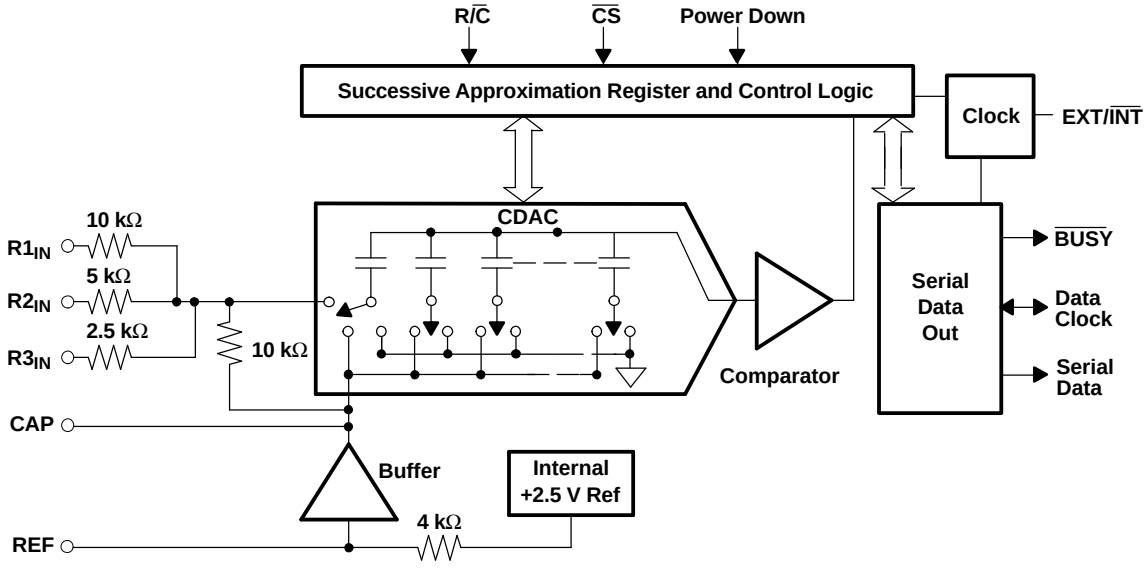
DESCRIPTION

The ADS8509 is a complete 16-bit sampling analog-to-digital (A/D) using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or can be synchronized to an external data clock. The ADS8509 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS8509 is specified at a 200-kHz sampling rate over the full temperature range. Calibrated resistors provide various input ranges including ±10 V and 0 V to 5 V, while the innovative design allows operation from a single +5-V supply with power dissipation under 100 mW.

The ADS8509 is available in 20-pin SO and 28-pin SSOP packages, both fully specified for operation over the industrial -40°C to 85°C temperature range.

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (%FSR)	MINIMUM SINAD (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8509IB	±2	±0.1	86	-40°C to 85°C	SO-20	DW	ADS8509IBDWT	Tube, 38
							ADS8509IBDWR	Tape and Reel, 1000
					SSOP-28	D	ADS8509IBDT	Tube, 38
							ADS8509IBDR	Tape and Reel, 1000
ADS8509I	±3	±0.5	83	-40°C to 85°C	SO-20	DW	ADS8509IDWT	Tube, 38
							ADS8509IDWR	Tape and Reel, 1000
					SSOP-28	D	ADS8509IDT	Tube, 38
							ADS8509IDR	Tape and Reel, 1000

(1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		ADS8509
Analog inputs	$R1_{IN}$	±25 V
	$R2_{IN}$	±25 V
	$R3_{IN}$	±25 V
	CAP	$+V_{ANA}$ + 0.3 V to AGND2 - 0.3 V
	REF	Indefinite short to AGND2, momentary short to V_{ANA}
Ground voltage differences	DGND, AGND2	±0.3 V
	V_{ANA}	7 V
	V_{DIG} to V_{ANA}	0.3 V
	V_{DIG}	7 V
Digital inputs		-0.3 V to $+V_{DIG}$ + 0.3 V
Maximum junction temperature		165°C
Internal power dissipation		700 mW
Lead temperature (soldering, 10s)		300°C

(1) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = -40°C to 85°C, f_s = 200 kHz, $V_{DIG} = V_{ANA}$ = 5 V, using internal reference and fixed resistors (see Figure 4), (unless otherwise specified)

PARAMETER	TEST CONDITIONS	ADS8509I			ADS8509IB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				16			16	Bits
ANALOG INPUT								
Voltage ranges(1)								
Impedance(1)								
Capacitance			50			50		pF
THROUGHPUT SPEED								
Conversion cycle	Acquire and convert			4			4	µs
Throughput rate		200			200			kHz

(1) ±10 V, 0 V to 5 V, etc. (see Table 1)

PRODUCT PREVIEW

PARAMETER	TEST CONDITIONS	ADS8509I			ADS8509IB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY								
Integral linearity error		-3		3	-2		2	LSB(2)
Differential linearity error		-2		2	-1		1	LSB
No missing codes		15			16			Bits
Transition noise(3)			1			1		LSB
Full-scale error(4)(5)	Int. Ref.	0.1		0.1	-0.1		0.1	%FS
Full-scale error drift	Int. Ref.		±7			±7		ppm/°C
Full-scale error(4)(5)	Ext. 2.5-V Ref.	-0.01		0.01	-0.01		0.01	%FS
Full-scale error drift	Ext. 2.5-V Ref.		±2			±2		ppm/°C
Bipolar zero error(4)	Bipolar ranges	-2		2	-2		2	mV
Bipolar zero error drift	Bipolar ranges		±2			±2		ppm/°C
Unipolar zero error(4)	0 V to 10 V ranges	-5		5	-5		5	mV
	0 V to 4 V, 0 V to 5 V ranges	-3		3	-3		3	mV
Unipolar zero error drift	Unipolar ranges		±2				±2	ppm/°C
Recovery to rated accuracy after power down	1-µF Capacitor to CAP		1			1		ms
Power supply sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75 V < VD < +5.25 V	-8		8	-8		8	LSB
AC ACCURACY								
Spurious-free dynamic range	f_I = 20 kHz	90	100		96	100		dB(6)
Total harmonic distortion	f_I = 20 kHz		-100	-90		-100	-94	dB
Signal-to-(noise+distortion)	f_I = 20 kHz	83	88		86	88		dB
	–60-dB Input		30			32		dB
Signal-to-noise ratio	f_I = 20 kHz	83	88		86	88		dB
Full-power bandwidth(7)			500			500		kHz
SAMPLING DYNAMICS								
Aperture delay			40			40		ns
Transient response	FS Step			2			2	µs
Overvoltage recovery(8)			150			150		ns
REFERENCE								
Internal reference voltage	No load	2.48	2.5	2.52	2.48	2.5	2.52	V
Internal reference source current (must use external buffer)			1			1		µA
Internal reference drift			8			8		ppm/°C
External reference voltage range for specified linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
External reference current drain	Ext. 2.5-V Ref.			100			100	µA

(2) LSB means least significant bit. For the ±10-V input range, one LSB is 305 µV.
(3) Typical rms noise at worst case transitions and temperatures.
(4) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.
(5) For bipolar input ranges, full-scale error is the worst case of -full-scale or +full-scale uncalibrated deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.
(6) All specifications in dB are referred to a full-scale ±10-V input.
(7) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

PARAMETER	TEST CONDITIONS	ADS8509I			ADS8509IB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Logic levels								
V_{IL}		-0.3		0.8	-0.3		0.8	V
V_{IH}		2.0		V_D +0.3 V	2.0		V_D +0.3 V	V
I_{IL}	V_{IL} = 0 V			±10			±10	µA
I_{IH}	V_{IH} = 5 V			±10			±10	µA
DIGITAL OUTPUTS								
Data format (Serial 16-bits)								
Data coding (Binary 2s complement or straight binary)								
Pipeline delay (Conversion results only available after completed conversion.)								
Data clock (Selectable for internal or external data clock)								
Internal clock (output only when transmitting data)	EXT/$\overline{INT}$ Low		7			7		MHz
External clock (can run continually)	EXT/$\overline{INT}$ High	0.1		26	0.1		26	MHz
V_{OL}	I_{SINK} = 1.6 mA			0.4			0.4	V
V_{OH}	I_{SOURCE} = 500 µA	4			4			V
Leakage current	Hi-Z state, V_{OUT} = 0 V to V_{DIG}			±5			±	µA
Output capacitance	Hi-Z state			15			15	pF
POWER SUPPLIES								
Specified performance								
V_{DIG}	Must be ≤ V_{ANA}	4.75	5	5.25	4.75	5	5.25	V
V_{ANA}		4.75	5	5.25	4.75	5	5.25	V
I_{DIG}			0.3			0.3	0.5	mA
I_{ANA}			12			12	19.5	mA
POWER DISSIPATION								
PWRD Low	f_S = 200 kHz		60	100		60	100	mW
PWRD High			50			50		µW
TEMPERATURE RANGE								
Specified performance		-40		85	-40		85	°C
Derated performance		-55		125	-55		125	°C
Storage		-65		150	-65		150	°C
THERMAL RESISTANCE (Θ_{JA})								
SSOP			75			75		°C/W
SO			75			75		°C/W

TYPICAL CHARACTERISTICS

INL

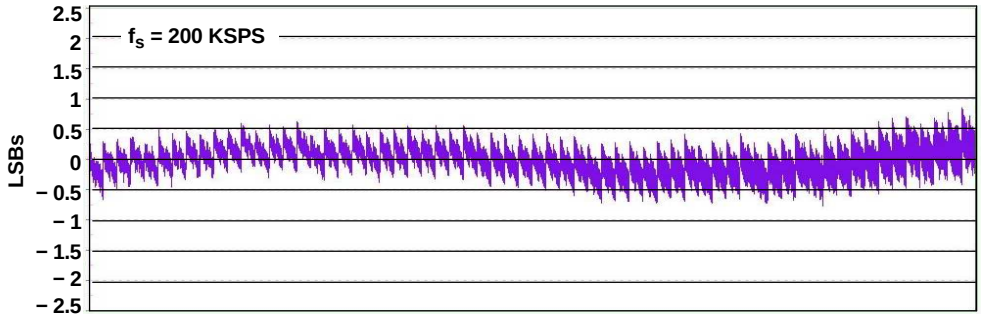


Figure 1.

DNL

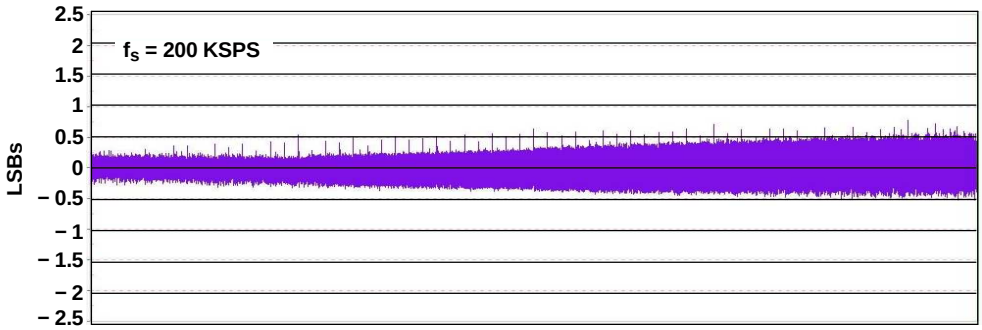
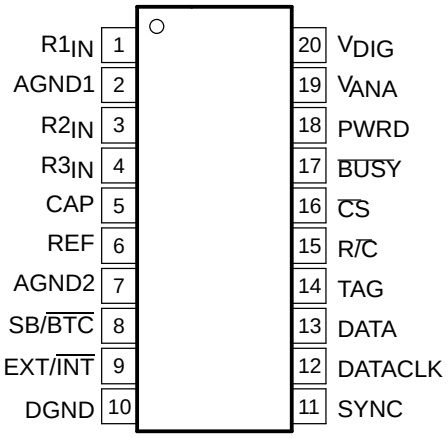
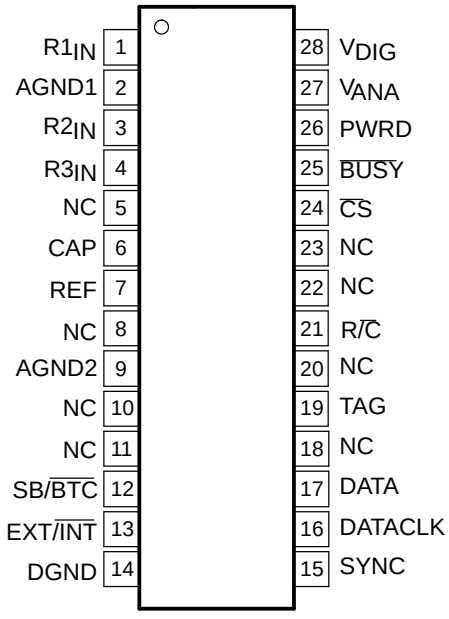


Figure 2.

DW PACKAGE
(TOP VIEW)



D PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

Terminal Functions

TERMINAL			DESCRIPTION
D NO.	DW NO.	NAME	
1	1	$R1_{IN}$	Analog input. See Table 1 and Figure 4 for input range connections.
2	2	AGND1	Analog ground. Used internally as ground reference point. Minimal current flow.
3	3	$R2_{IN}$	Analog input. See Table 1 and Figure 4 for input range connections.
4	4	$R3_{IN}$	Analog input. See Table 1 and Figure 4 for input range connections.
6	5	CAP	Reference buffer capacitor. 2.2-µF tantalum to ground.
7	6	REF	Reference input/output. Outputs internal 2.5-V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2-µF tantalum capacitor.
9	7	AGND2	Analog ground
12	8	SB/$\overline{\text{BTC}}$	Select straight binary or binary 2s complement data output format. If high, data is output in a straight binary format. If low, data is output in a binary 2s complement format.
13	9	EXT/$\overline{\text{INT}}$	Select external or internal clock for transmitting data. If high, data is output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 16-clock pulses output on DATACLK.
14	10	DGND	Digital ground
15	11	SYNC	Synch output. If EXT/$\overline{\text{INT}}$ is high, either a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ low or a falling edge on $\overline{\text{CS}}$ with R/$\overline{\text{C}}$ high outputs a pulse on SYNC synchronized to the external DATACLK.
16	12	DATACLK	Either an input or an output depending on the EXT/$\overline{\text{INT}}$ level. Output data is synchronized to this clock. If EXT/$\overline{\text{INT}}$ is low, DATACLK transmits 16 pulses after each conversion, and then remain low between conversions.
17	13	DATA	Serial data output. Data is synchronized to DATACLK, with the format determined by the level of SB/$\overline{\text{BTC}}$. In the external clock mode, after 16 bits of data, the ADS8509 outputs the level input on TAG as long as $\overline{\text{CS}}$ is low and R/$\overline{\text{C}}$ is high (see Figure 3). If EXT/$\overline{\text{INT}}$ is low, data is valid on both the rising and falling edges of DATACLK, and between conversions DATA stays at the level of the TAG input when the conversion was started.
19	14	TAG	Tag input for use in external clock mode. If EXT/$\overline{\text{INT}}$ is high, digital data input on TAG is output on DATA with a delay of 16 DATACLK pulses as long as $\overline{\text{CS}}$ is low and R/$\overline{\text{C}}$ is high. See Figure 3.
21	15	R/$\overline{\text{C}}$	Read/convert input. With $\overline{\text{CS}}$ low, a falling edge on R/$\overline{\text{C}}$ puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/$\overline{\text{INT}}$ is low, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{\text{INT}}$ is high, a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ low, or a falling edge on $\overline{\text{CS}}$ with R/$\overline{\text{C}}$ high, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
24	16	$\overline{\text{CS}}$	Chip select. Internally ORed with R/$\overline{\text{C}}$
25	17	$\overline{\text{BUSY}}$	Busy output. Falls when a conversion is started, and remains low until the conversion is completed and the data is latched into the output shift register. $\overline{\text{CS}}$ or R/$\overline{\text{C}}$ must be high when $\overline{\text{BUSY}}$ rises, or another conversion starts without time for signal acquisition.
26	18	PWRD	Power down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
27	19	V_{ANA}	Analog supply input. Nominally +5 V. Connect directly to pin 20, and decouple to ground with 0.1-µF ceramic and 10-µF tantalum capacitors.
28	20	V_{DIG}	Digital supply input. Nominally +5 V. Connect directly to pin 19. Must be ≤ V_{ANA}.
5, 8, 10, 11, 18, 20, 22, 23	-	NC	No connect

PRODUCT PREVIEW

Table 1. Input Range Connections (see Figure 4 for complete information)

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200 Ω TO	CONNECT $R2_{IN}$ VIA 100 Ω TO	CONNECT R3 TO	IMPEDANCE
±10 V	V_{IN}	AGND	CAP	11.5 kΩ
±5 V	AGND	V_{IN}	CAP	6.7 kΩ
±3.33 V	V_{IN}	V_{IN}	CAP	5.4 kΩ
0 V to 10 V	AGND	V_{IN}	AGND	6.7 kΩ
0 V to 5 V	AGND	AGND	V_{IN}	5.0 kΩ
0 V to 4 V	V_{IN}	AGND	V_{IN}	5.4 kΩ

Table 2. Conversion and Data Timing, T_A = –40°C to 85°C

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert pulse width	40			ns
t_2	$\overline{BUSY}$ delay		6	20	ns
t_3	$\overline{BUSY}$ low			3.2	µs
t_4	$\overline{BUSY}$ delay after end of conversion		5		ns
t_5	Aperture delay		5		ns
t_6	Conversion time			3.2	µs
t_7	Acquisition time	1.8			µs
$t_6 + t_7$	Throughput time				µs
t_8	R/$\overline{C}$ Low to DATACLK delay		270		ns
t_9	DATACLK period		135		ns
t_{10}	Data valid to DATACLK high delay	15	35		ns
t_{11}	Data valid after DATACLK low delay	20	35		ns
t_{12}	External DATACLK	35			ns
t_{13}	External DATACLK high	15			ns
t_{14}	External DATACLK low	15			ns
t_{15}	DATACLK high setup time	15		t_{12} + 5	ns
t_{16}	R/$\overline{C}$ to $\overline{CS}$ setup time	10			ns
t_{17}	SYNC delay after DATACLK high	3		35	ns
t_{18}	Data valid delay	2		20	ns
t_{19}	$\overline{CS}$ to rising edge delay	10			ns
t_{20}	Data available after $\overline{CS}$ low	2			µs
t_{21}	BUSY to external DATACLK setup time	5			ns
t_{22}	BUSY falling edge to final external DATACLK			1.2	µs
t_{23}	TAG valid setup time	0			ns
t_{24}	TAG valid hold time	2			ns

PRODUCT PREVIEW

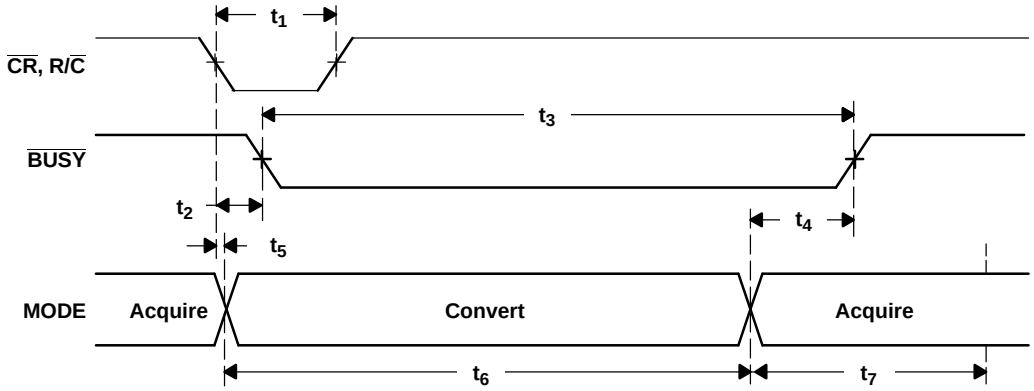


Figure 3. Basic Conversion Timing

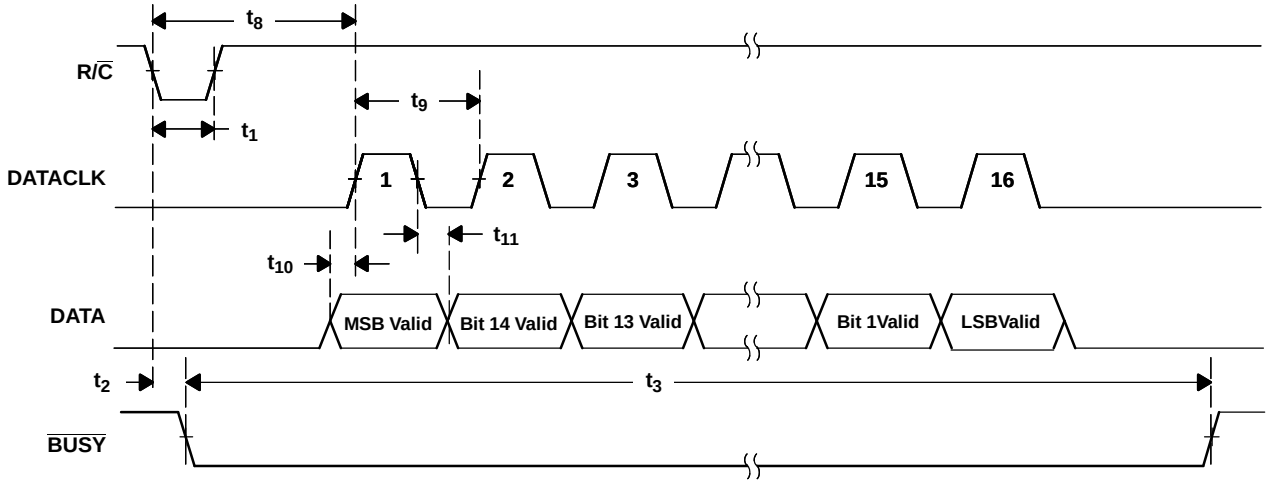


Figure 4. Serial Data Timing Using Internal Clock ($\overline{CS}$, EXT/$\overline{INT}$ and TAG Tied Low)

PRODUCT PREVIEW

Table 3. Control Truth Table

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/INT	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate conversion and output data using internal clock	1 > 0	0	1	0	Output	0	x	Initiates conversion *n*. Data from conversion *n - 1* clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	
Initiate conversion and output data using external clock	1 > 0	0	1	1	Input	0	x	Initiates conversion *n*.
	0	1 > 0	1	1	Input	0	x	Initiates conversion *n*.
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion *n* clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion *n - 1* clocked out synchronized to external DATACLK.(1) Conversion *n* in process.
	0	1 > 0	0	1	Input	0	x	
Incorrect conversions	0	0	0 > 1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
Power down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed..
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting output format	x	x	x	x	x	x	0	Serial data is output in binary 2s complement format.
	x	x	x	x	x	x	1	Serial data is output in straight binary format.

(1) See Figure 3 for constraints on previous data valid during conversion.

Table 4. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY 2s COMPLEMENTS (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-scale range	±10	±5	±3.33 V	0 V to 10 V	0 V to 5 V	0 V to 4 V				
Least significant bit (LSB)	305 µV	153 µV	102 µV	153 µV	76 µV	61 µV				
Full scale (FS - 1LSB)	9.999695 V	4.999847 V	3.333231 V	9.999847 V	4.999924 V	3.999939 V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0 V	0 V	0 V	5 V	2.5 V	2 V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB below midscale	-305 µV	153 µV	±102 µV	4.999847 V	2.499924 V	1.999939 V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
-Full scale	-10 V	-5 V	-3.333333 V	0 V	0 V	0 V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

PRODUCT PREVIEW

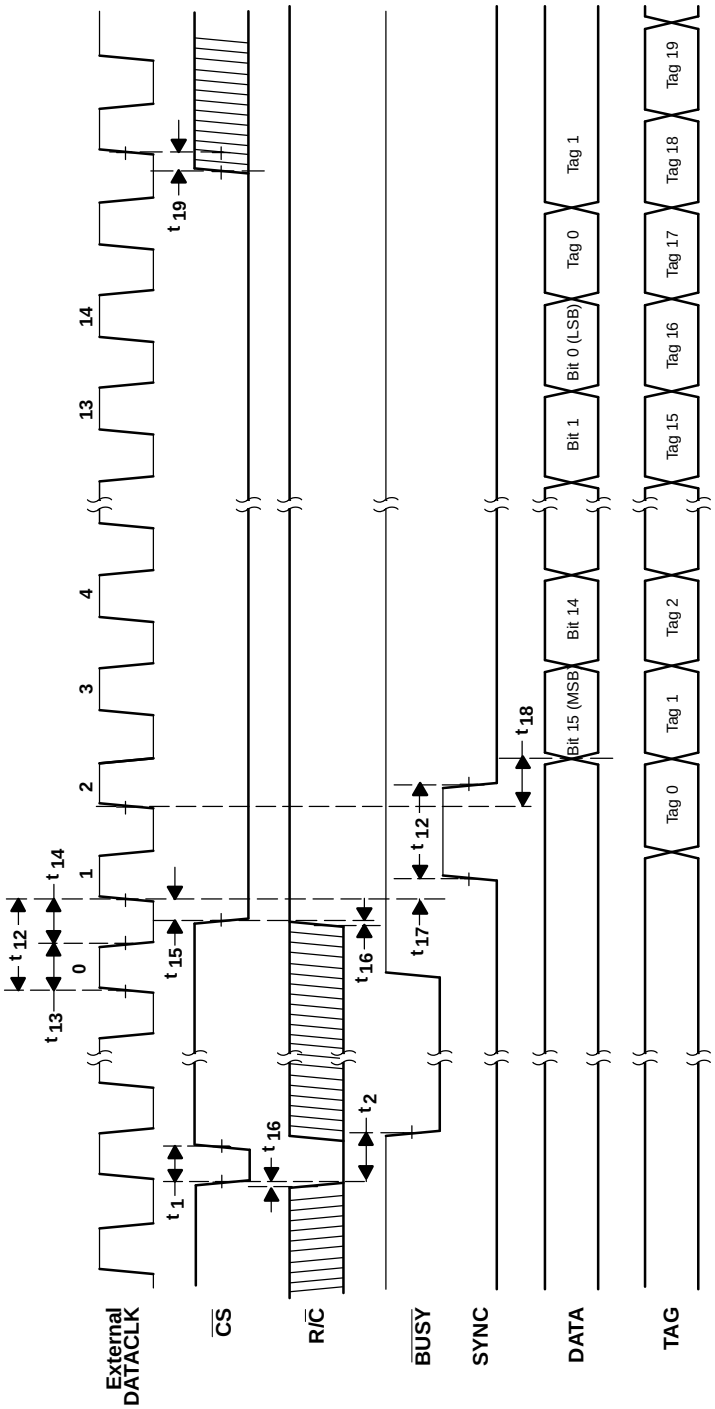


Figure 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied High) Read After Conversions

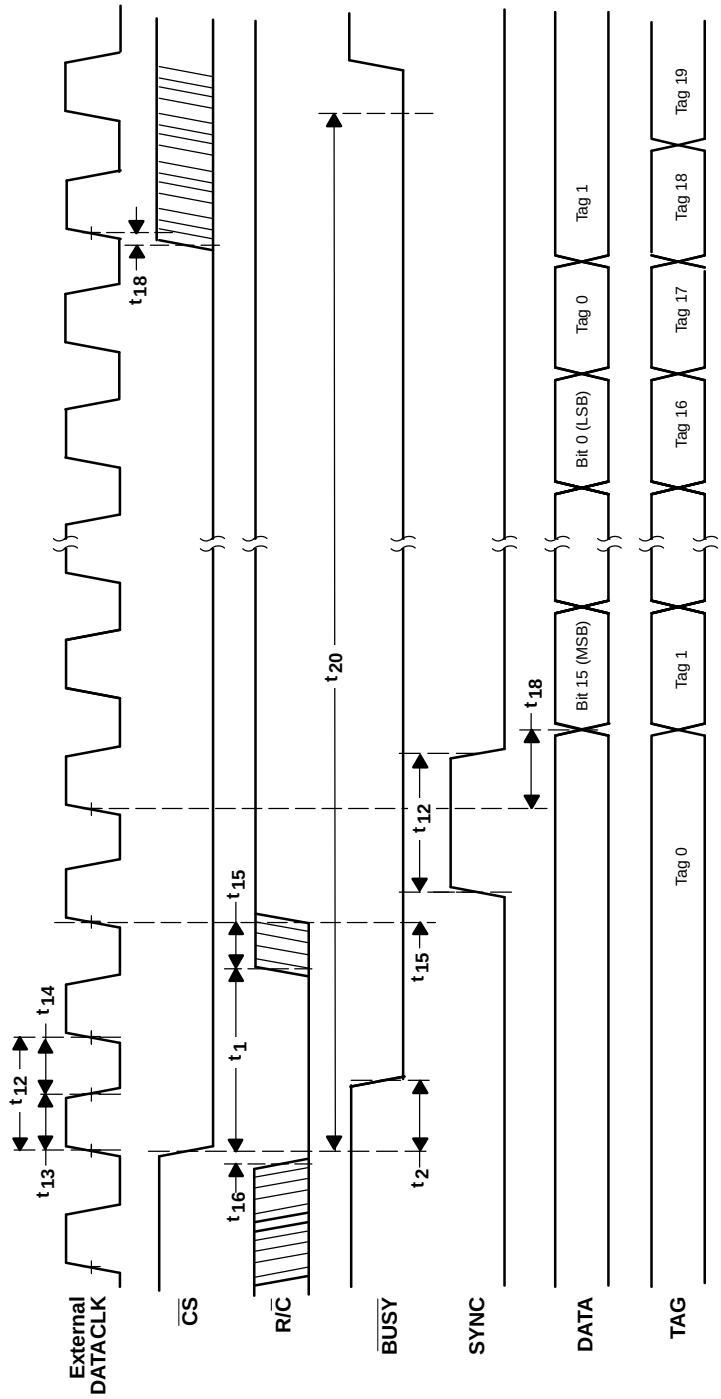


Figure 6. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied High) Read During Conversion (Previous Conversion Results)

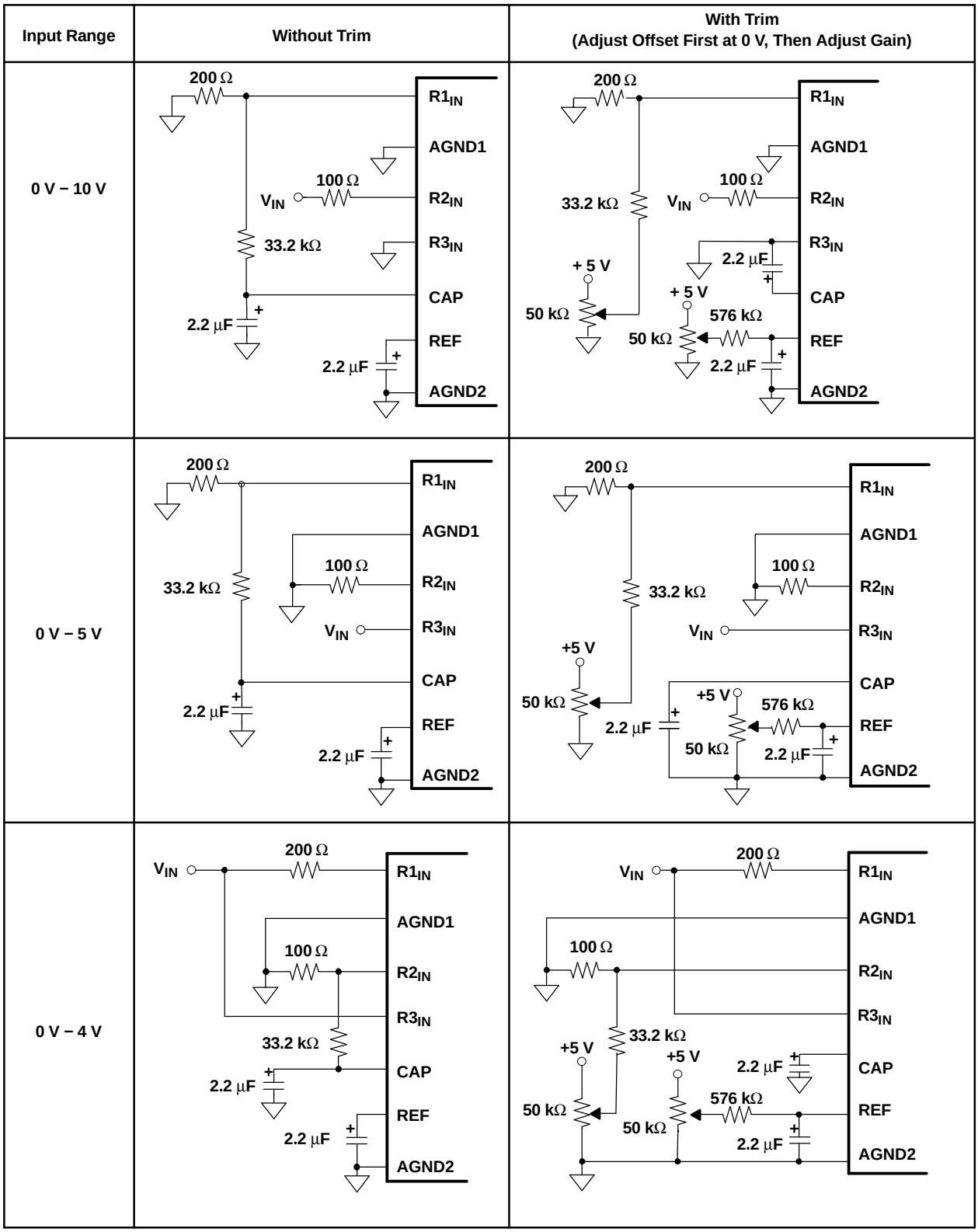


Figure 7. Offset/Gain Circuits for Unipolar Input Ranges

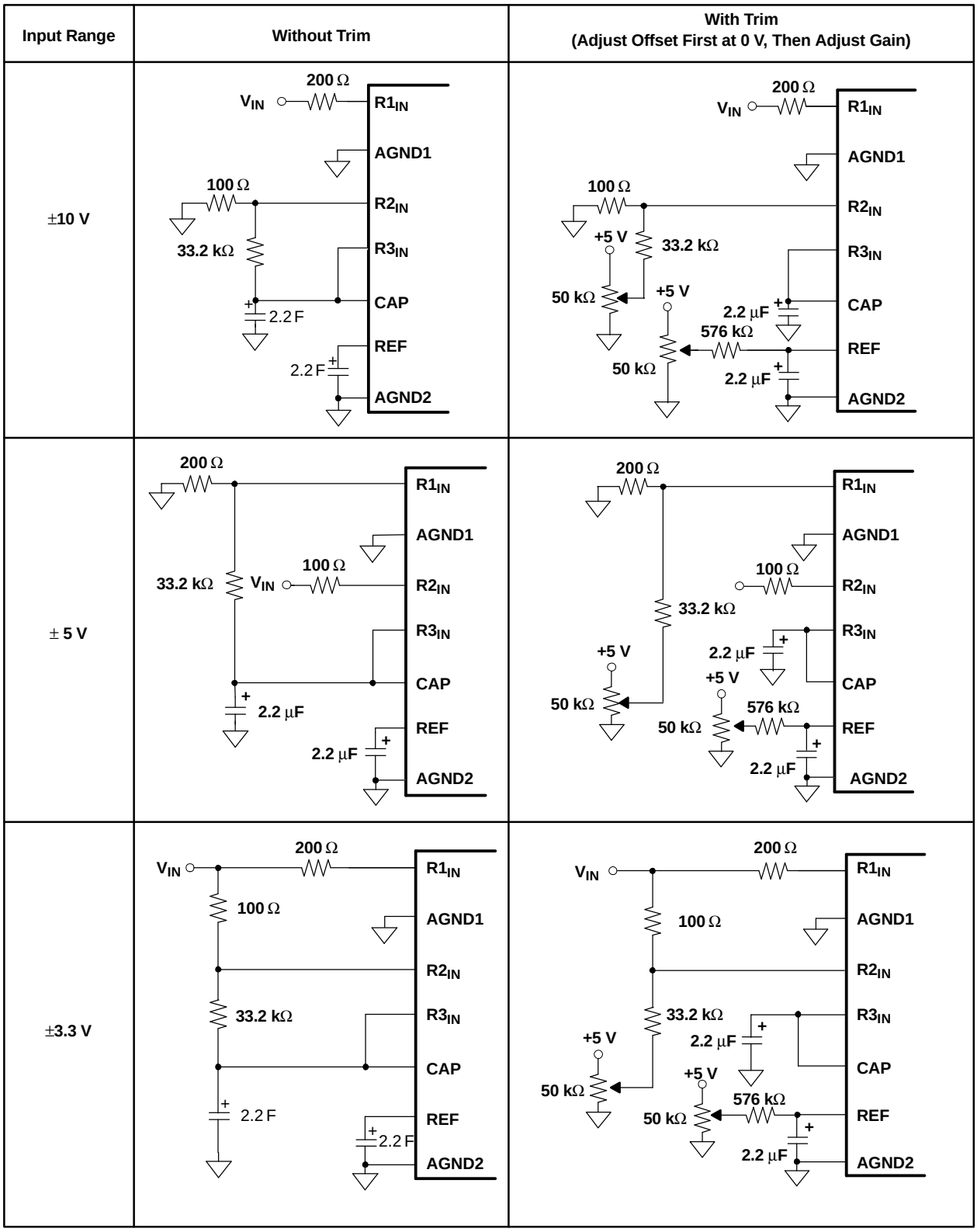
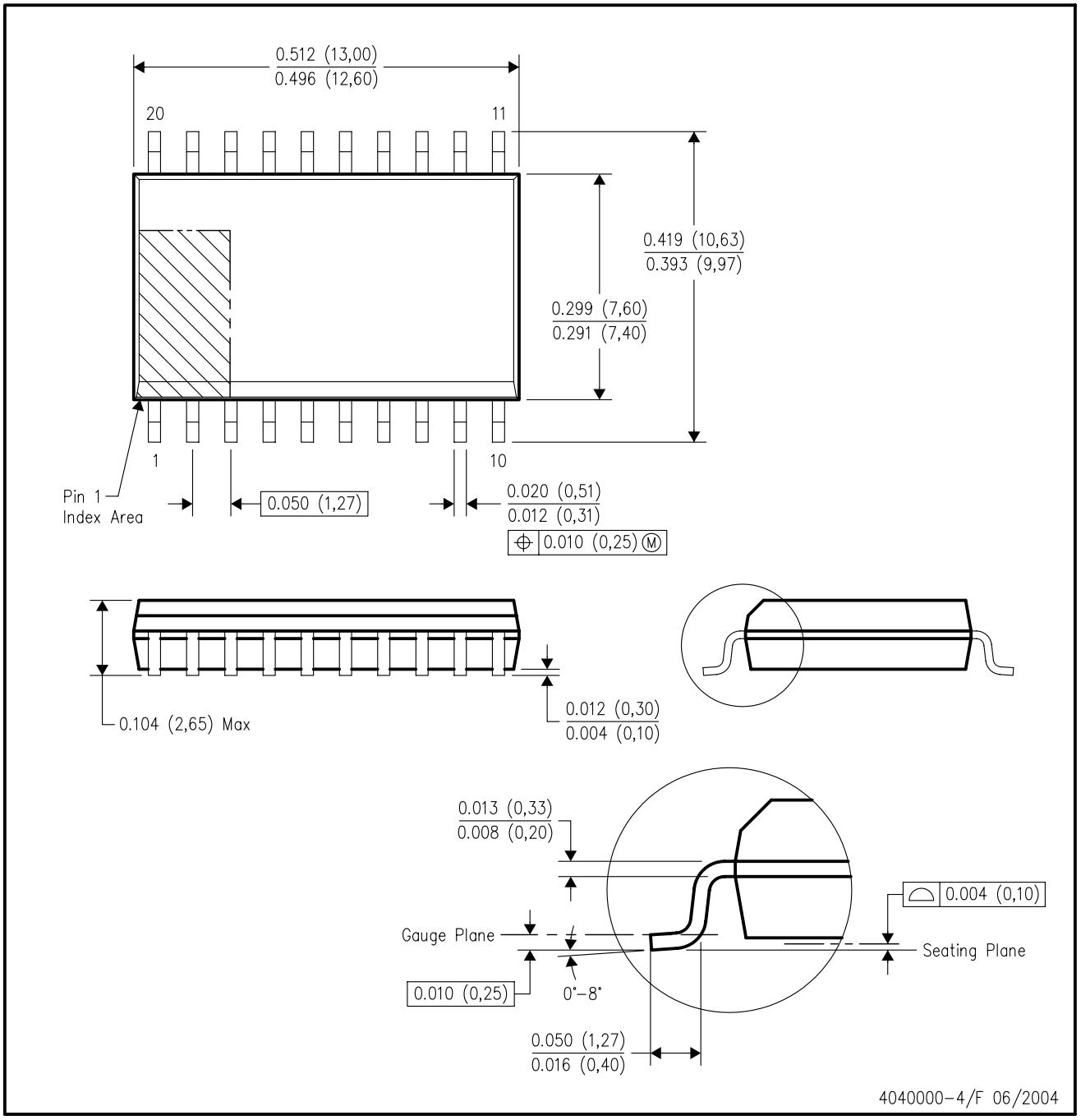


Figure 8. Offset/Gain Circuits for Bipolar Input Ranges

PRODUCT PREVIEW

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

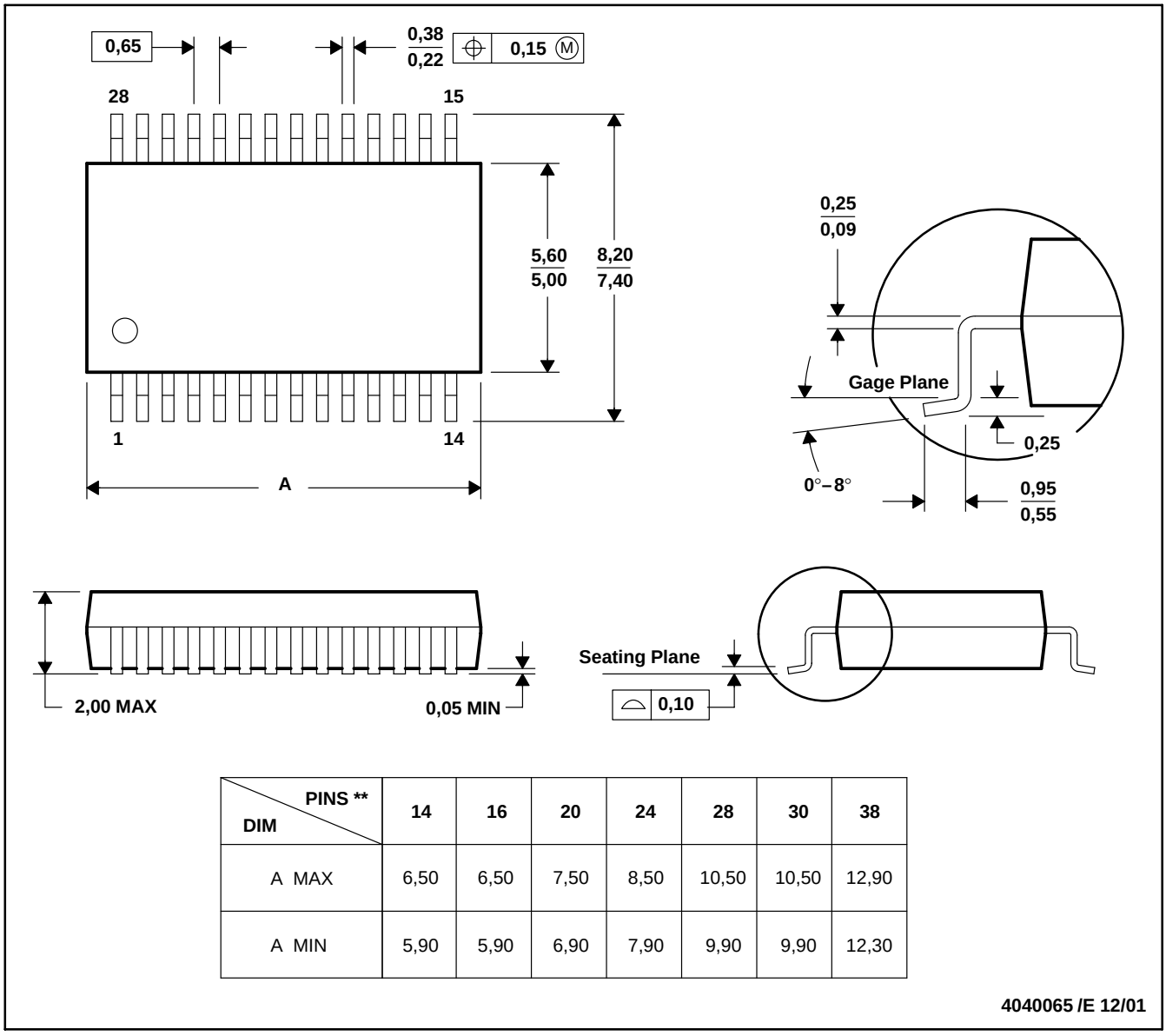


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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