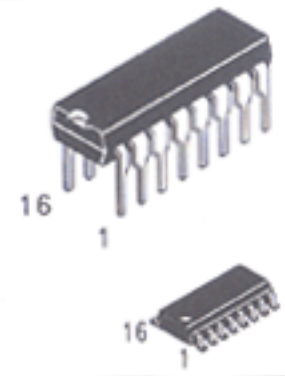
112

Dual JK Negative Edge-Triggered Flip-Flops

DV74LS112A
DV74ALS112A

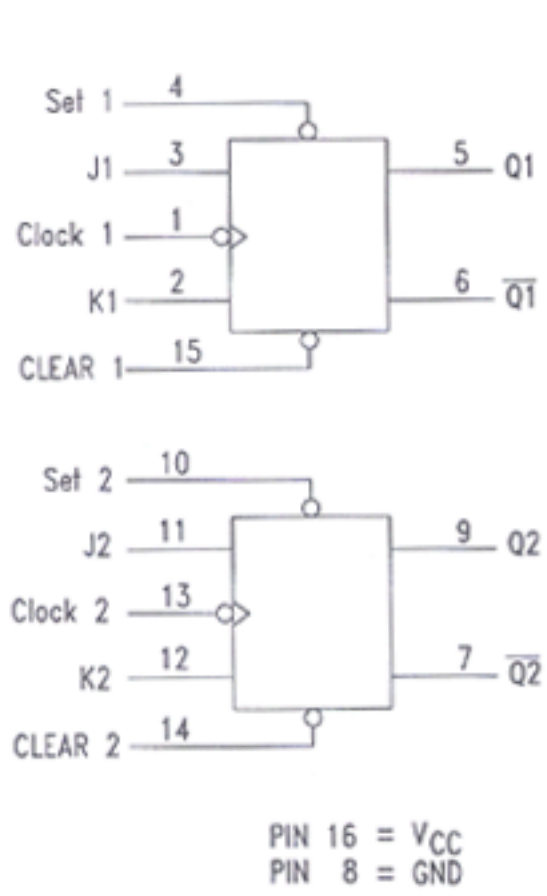


N Suffix
Plastic DIP
AVG-003 Case

D Suffix
Plastic SOP
AVG-004 Case

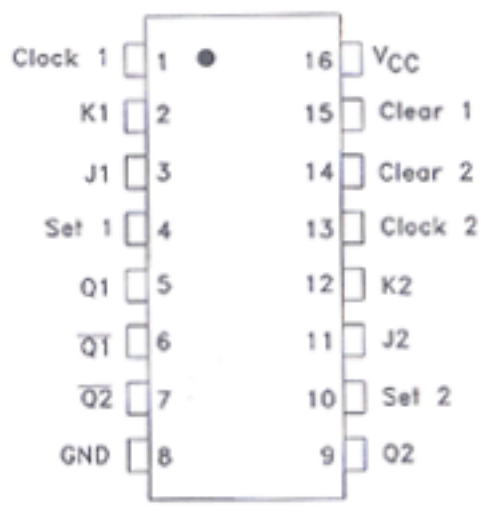
This device contains two individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock pulse goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

- **AVG's LS operates over extended Vcc from 4.5 to 5.5 V**
- **AVG's LS and ALS both have guaranteed DC and AC specification over full temperature and Vcc range**
- **Switching specifications for ALS at 50 pF**
- **AVG's ALS has the lowest speed power product (4pJ per gate typical) of all logic series**



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



TRUTH TABLE

Inputs					Output	
Set	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H=HIGH Voltage Level
L=LOW Voltage Level
X=Immaterial
Q0=Previous Condition of Q
* Outputs are unpredictable if Set and Clear go low simultaneoulsy

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	LS112A	ALS112A	Unit
V_{CC}	Supply Voltage	7.0	7.0	V
V_{IN}	Input Voltage	7.0	7.0	V
T_{STG}	Storage Temperature Range	–65 to+150	–65 to + 150	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	LS112A		ALS112A		Unit
		Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	2.0		2.0		V
V_{IL}	Low Level Input Voltage		0.8		0.8	V
I_{OH}	High Level Output Current		–0.4		–0.4	mA
I_{OL}	Low Level Output Current		8.0		8.0	mA
T_A	Ambient Temperature Range	–10 to +70		–10 to + 70		°C

SWITCHING CHARACTERISTICS

Symbol	Parameter	Condition		LS112A			ALS112A			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC}= min, I_{IN} = -18 mA				–1.5			–1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = min, I_{OH} =max		Vcc-2	3.5		Vcc-2			V
V_{OL}	Low Level Output Voltage	V_{CC}=min	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA		0.35	0.5		0.35	0.5	V
I_{IH}	High Level Input Current J, K Clock Set, Clear	V_{CC}=max, V_{IN}= 2.7V				 20 80 60			 20 20 40	µA
	J, K Clock Set, Clear	V_{CC}=max, V_{IN}= 7V				0.1 0.4 0.3			0.1 0.1 0.2	mA
I_{IL}	Low Level Input Current J, K Clock Set, Clear	V_{CC}=max, V_{IN}=0.4V				 –0.4 –0.8 –0.8			 –0.2 –0.2 –0.4	mA
I_O	Output Short Circuit Current	V_{CC}=max, V_{OUT} =2.25V		–20		–110	–30		–112	mA
I_{CC}	Power Supply Current	V_{CC}=max				6.0		2.5	4.5	mA

Symbol	Parameter	INPUT	OUTPUT	LS112A C_L=15 pF		ALS112A C_L=50pF R_L=500Ω		Unit
				Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency			30		30		MHz
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Clock	Any Q		20	3	15	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Clock	Any Q		20	5	19	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Set or Clear	Any Q		20	3	15	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Set or Clear	Any Q		20	4	18	ns

AC SETUP REQUIREMENTS over full operating conditions

Symbol	Parameter		LS112A		ALS 112A		Units
			MIN	MAX	MIN	MAX	
t_w	Pulse Width	Set or Clear Low Clock High Clock Low	25 20		10 16.5 16.5		ns
t_s	Setup Time		20		22		ns
t_h	Hold Time		0		0		ns
t_{rec}	Clock Recovery Time		25		20		ns

SWITCHING WAVEFORMS