PRELIMINARY

CY7C1360V25
CY7C1362V25

256K x 36 / 512K x 18 Synchronous Pipelined SRAM

Features

- **Supports 200-MHz bus**
- **Fully registered inputs and outputs for pipelined operation**
- **Single 2.5V power supply**
- **Fast clock-to-output times**
  - **— 3.1 ns (for 200-MHz device)**
  - **— 3.5 ns (for 166-MHz device)**
  - **— 4.0 ns (for 133-MHz device**
  - **— 5.0 ns (for 100-MHz device**
- **User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **Available as a 100-pin TQFP or 119 BGA**
- **"ZZ" Sleep Mode option and Stop Clock option**

Functional Description

The CY7C1360V25 and CY7C1362V25 are 2.5V, 256K x 36 and 512K x 18 synchronous-pipelined cache SRAM respectively designed to support zero wait state secondary cache with minimal glue logic.

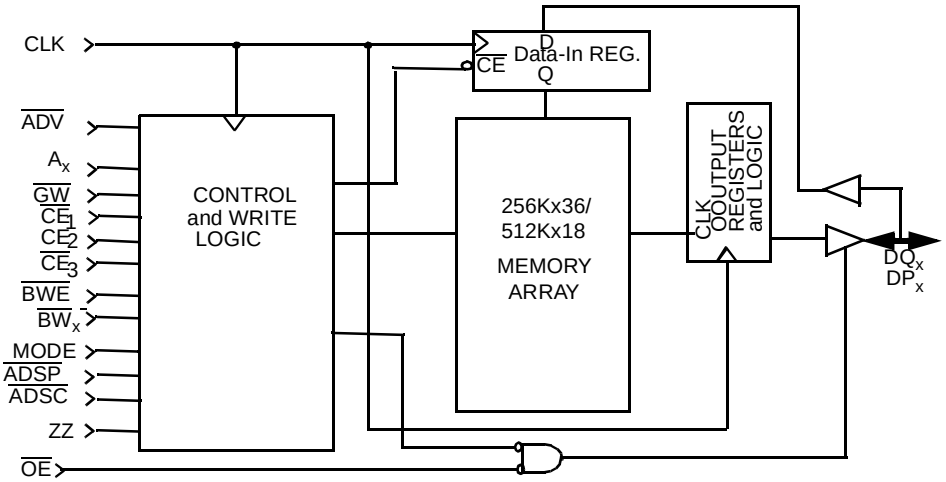
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 3.1 ns (200-MHz device).

The CY7C1360V25/CY7C1362V25 supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC™. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$) at clock rise. Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Select ($\overline{BW}_{a,b,c,d}$ for 1360V25 and $\overline{BW}_{a,b}$ for 1362V25) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.

Logic Block Diagram



	1360V25	1362V25
A_X	$A_{[17:0]}$	$A_{[18:0]}$
DQ_X	$DQ_{a,b,c,d}$	$DQ_{a,b}$
DP_X	$DP_{a,b,c,d}$	$DP_{a,b}$
$\overline{BW}_X$	$\overline{BW}_{a,b,c,d}$	$\overline{BW}_{a,b}$

Pin Configurations

119-Ball BGA

CY7C1360 (256K x 36)

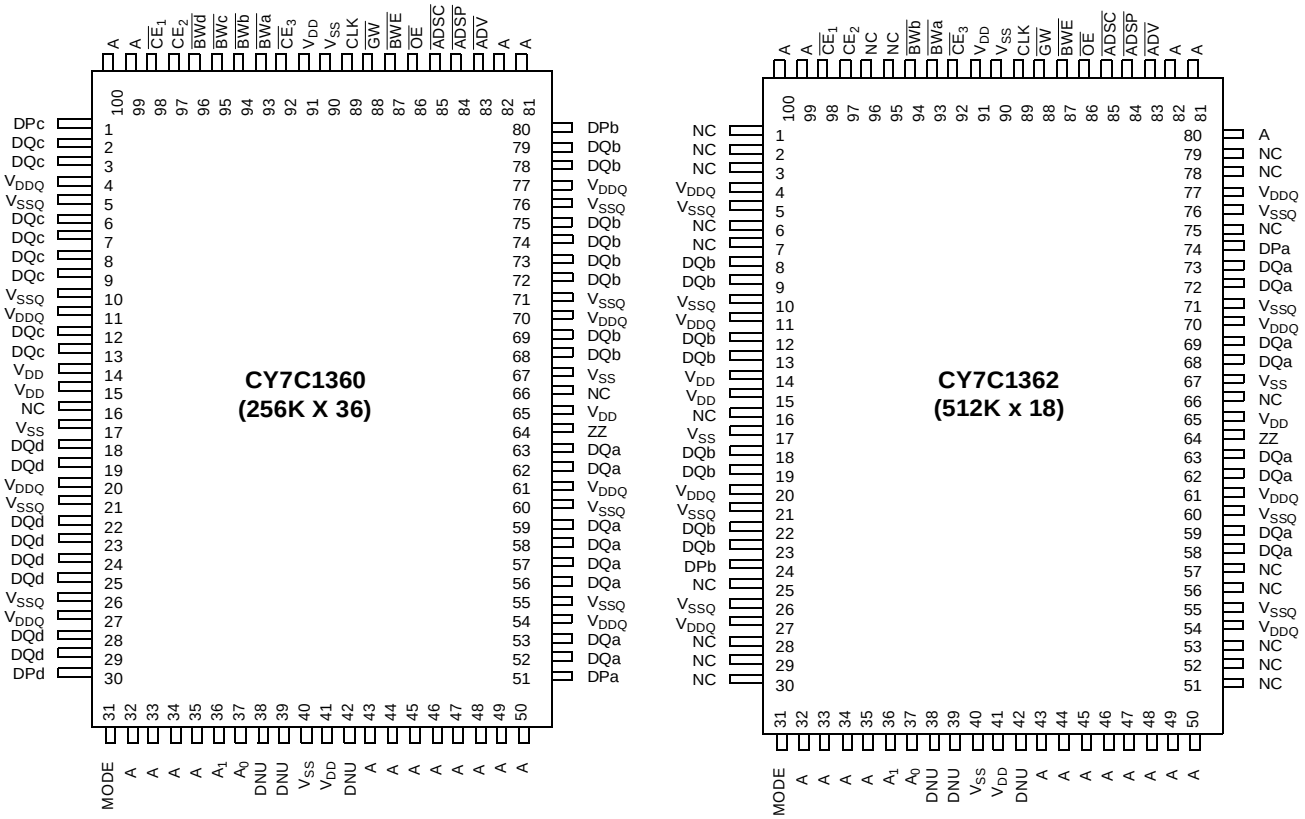
	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE_2	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	NC	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQb	DQc	V_{SS}	$\overline{GW}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	DP0	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BWE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0	V_{SS}	DQPa	DQa
R	NC	A	MODE	V_{DD}	V_{DD}	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1362 (512K x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE_2	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{BWb}$	$\overline{ADV}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQb	NC
J	V_{DDQ}	V_{DD}	NC	DP0	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQd	NC	V_{SS}	NC	$\overline{BWa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A0	V_{SS}	NC	DQa
R	NC	A	MODE	Vdd	V_{DD}	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

100-Pin TQFP



Selection Guide

		7C1360-200 7C1362-200	7C1360-166 7C1362-166	7C1360-133 7C1362-133	7C1360-100 7C1362-100
Maximum Access Time (ns)		3.1	3.5	4.0	5.0
Maximum Operating Current (mA)	Commercial	450	400	350	325
Maximum CMOS Standby Current (mA)		10	10	10	10

Pin Definitions (100-Pin TQFP)

x18 Pin Locations	x36 Pin Locations	Name	I/O	Description
37, 36, 32–25, 43–50, 80–82, 99, 100	37, 36, 32–35, 43–50, 81, 82, 99, 100	A0 A1 A	Input-Synchronous	Address Inputs used to select one of the address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
93, 94	93, 94, 95, 96,	$\overline{BWa}$ $\overline{BWb}$ $\overline{BWc}$ $\overline{BWd}$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	88	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{a,b,c,d}$ and $\overline{BWE}$).
87	87	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	89	CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
98	98	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.
97	97	CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
92	92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
86	86	$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
83	83	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	84	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.

Pin Definitions (100-Pin TQFP) (continued)

x18 Pin Locations	x36 Pin Locations	Name	I/O	Description
85	85	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[x:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
31	31	MODE	Input-Static	Selects Burst Order. When tied to GND selects linear burst sequence. When tied to VDDQ or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
64	64	ZZ	Input-Asynchronous	ZZ “sleep” Input. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved.
(a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12, 13, 18, 19, 22, 23	(a) 52, 53, 56–59, 62, 63 (b) 68, 69, 72–75, 78, 79 (c) 2, 3, 6–9, 12, 13 (d) 18, 19, 22–25, 28, 29	DQa DQb DQc DQd	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQa and DPa are placed in a three-state condition.
74, 24	51, 80, 1, 30	DPa DPb DPc DPd	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQx and DPx are placed in a three-state condition.
15, 41, 65, 91	15, 41, 65, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
17, 40, 67, 90	17, 40, 67, 90	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 2.5V power supply.
5, 10, 21, 26, 55, 60, 71, 76	5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	16, 66	NC	-	No Connects.
38, 39, 42	38, 39	DNU		Do Not Use Pins. These pins should be left floating or tied to V_{SS}

Pin Definitions (119-Ball BGA)

x18 Pin Locations	x36 Pin Locations	Name	I/O	Description
4P, 4N, 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6B, 6T	4P, 4N, 2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6B, 6C, 6R	A0 A1 A	Input-Synchronous	Address Inputs used to select one of the address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
5L, 3G	5L, 5G, 3G, 3L	$\overline{BW}$a $\overline{BW}$b $\overline{BW}$c $\overline{BW}$d	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
4M	4M	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{a,b,c,d}$ and $\overline{BWE}$).
4H	4H	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
4K	4K	CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
4E	4E	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.
97	97	CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
92	92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
4F	4F	$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
4G	4G	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
4A	4A	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.

Pin Definitions (119-Ball BGA)

x18 Pin Locations	x36 Pin Locations	Name	I/O	Description
4B	4B	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[x:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
3R	3R	MODE	Input-Static	Selects Burst Order. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
7T	7T	ZZ	Input-Asynchronous	ZZ “sleep” Input. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved.
(a) 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M	(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_x and DQP_x are placed in a three-state condition.
		TMS		
		TDI		
		TCK		
		TDO		
6D, 2P	6P, 6D, 2D, 2P	DQPa DQPb DQPc DQPd	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQx and DPx are placed in a three-state condition.
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 2.5V power supply.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R	NC	-	No Connects.
2U, 3U, 4U, 5U	2U, 3U, 4U, 5U	DNU		Do Not Use Pins. These pins should be left floating or tied to V_{SS}.

Introduction

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.1 ns (200-MHz device).

The CY7C1360V25/CY7C1362V25 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{a,b,c,d}$ for 1360 and $BW_{a,b}$ for 1362) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.1 ns (200-MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will three-state immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_x$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQx inputs is written into the corresponding address location in the RAM core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}x$ signals. The CY7C1360V25 provides byte write capability that is described in the write cycle description table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW}_{a,b,c,d}$ for 1360 & $\overline{BW}_{a,b}$ for CY7C1362V25) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1360V25/CY7C1362 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will three-state the output drivers. As a safety precaution, DQ are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_x$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented to $A_{[17:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the $DQ_{[x:0]}$ is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1360V25/CYC7C1362 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the $DQ_{[x:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[x:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1360V25/CY7C1362V25 provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		15	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Cycle Descriptions[1, 2, 3]

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	CE_2	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
ZZ “sleep”	None	H	X	X	X	X	X	X	X	Hi-Z	X

Notes:
1. X=”Don't Care”, 1=HIGH, 0=LOW.
2. Write is defined by $\overline{BWE}$, $\overline{BW}_X$, and $\overline{GW}$. See Write Cycle Descriptions table.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

Write Cycle Descriptions[1, 2, 3]

Function (1360)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_d$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{BW}_a$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0-DQ_a	1	0	1	1	1	0
Write Byte 1-DQ_b	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - DQ_c	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - DQ_d	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Function (1362)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_b$	$\overline{BW}_a$
Read	1	1	X	X
Read	1	0	1	1
Write Byte 0 - $DQ_{[7:0]}$ and DP_0	1	0	1	0
Write Byte 1 - $DQ_{[15:8]}$ and DP_1	1	0	0	1
Write All Bytes	1	0	0	0
Write All Bytes	0	X	X	X

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1360/62 incorporates a serial boundary scan Test Access Port (TAP) in the FBGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAP Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller , TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP) - Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The e output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a xx-bit-long register, and the x18 configuration has a yy-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the

SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE / PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE / PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE / PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE / PRELOAD

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant.

When the SAMPLE / PRELOAD instructions loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (TCS and TCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE / PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE / PRELOAD instruction will have the same effect as the Pause-DR command.

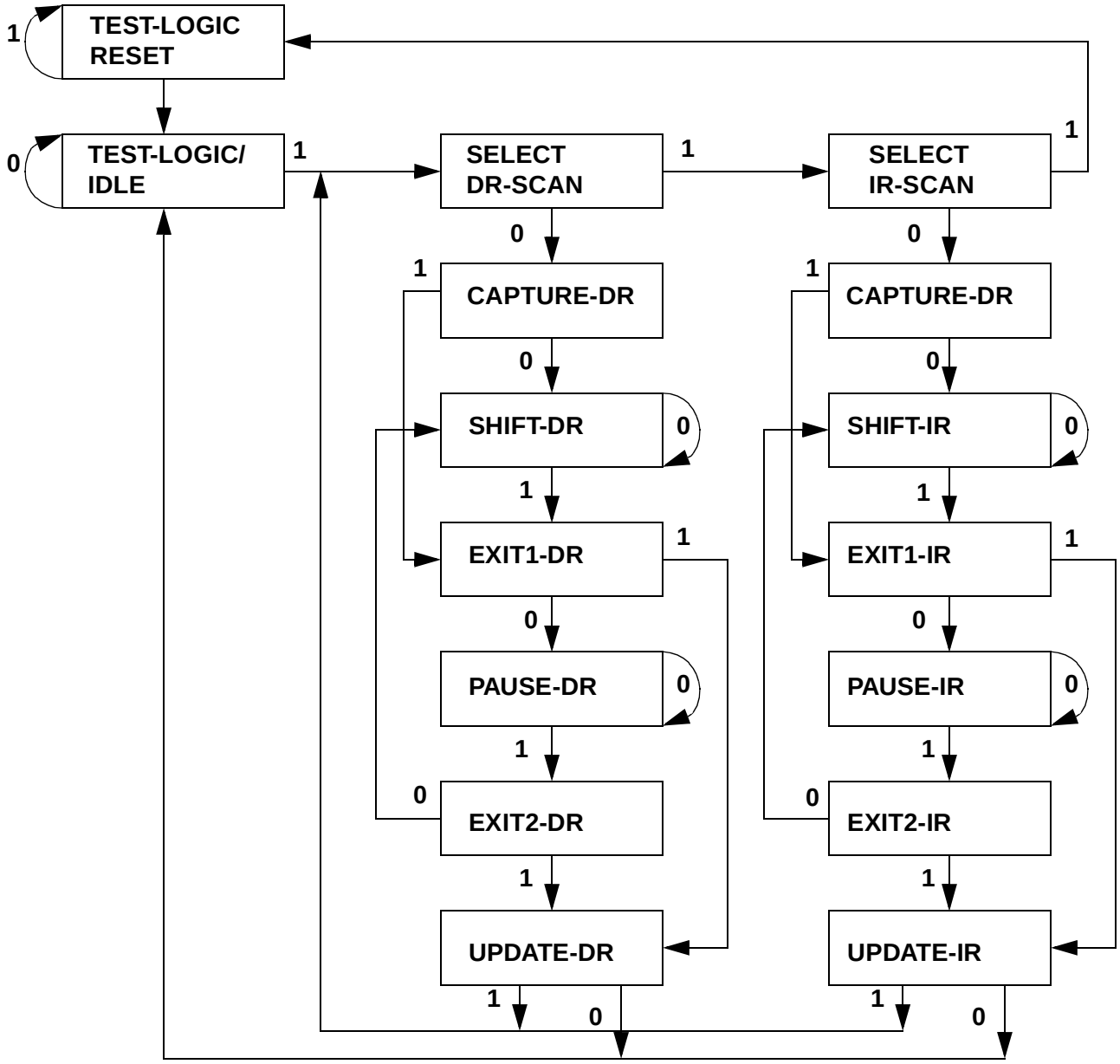
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

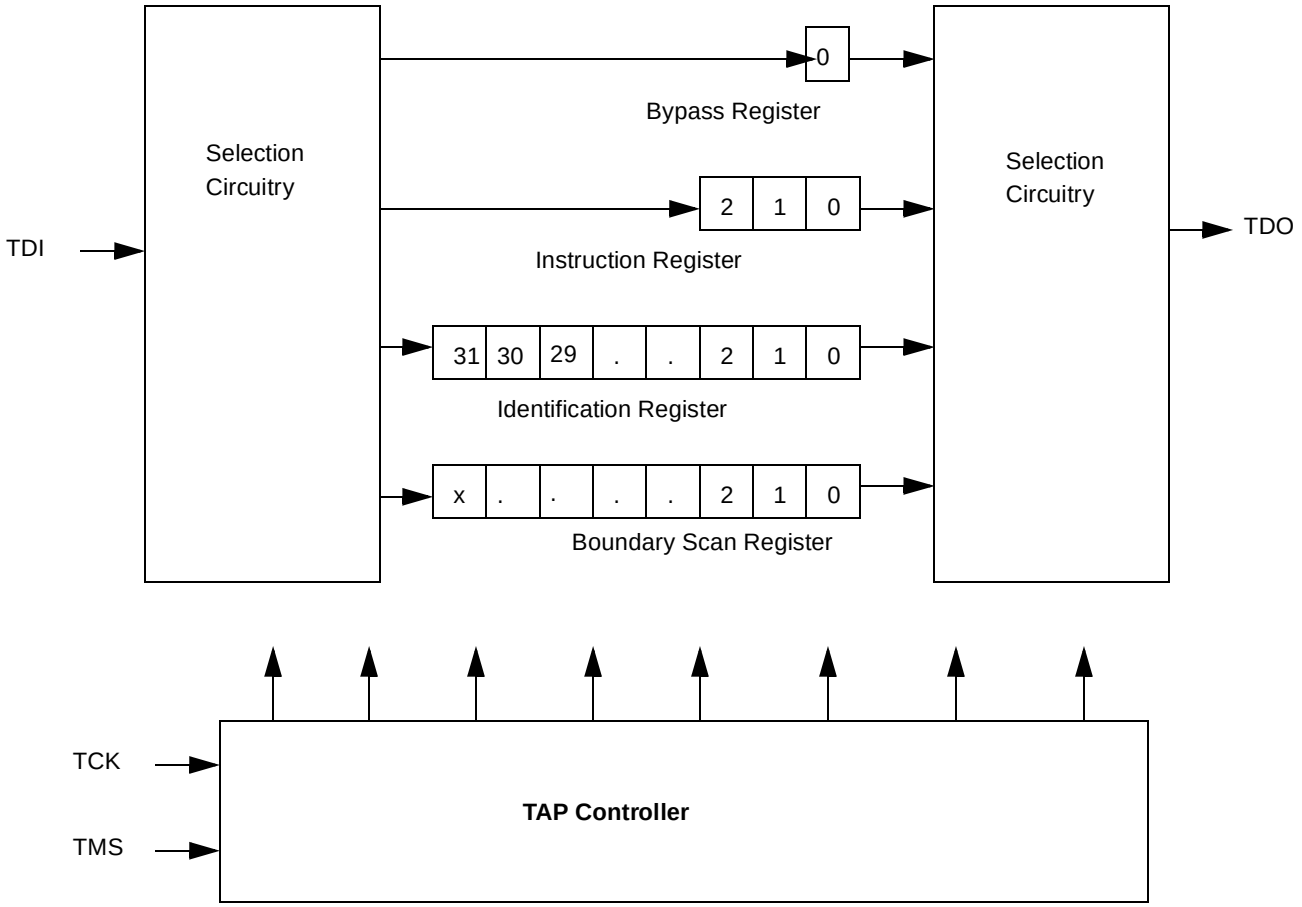
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



Note: The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 mA	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.7	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 mA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	mA

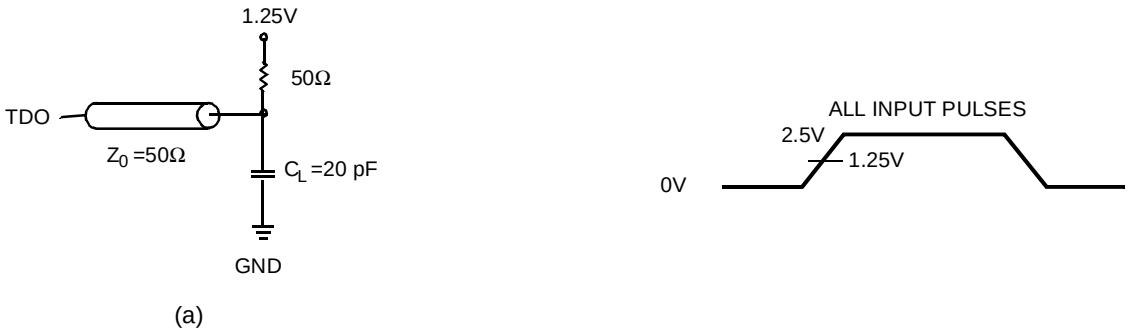
4. All Voltage referenced to Ground.
5. Overshoot: $V_{IH}(AC) \leq V_{DD}+1.5V$ for $t \leq t_{TCYC}/2$, Undershoot: $V_{IL}(AC) \leq 0.5V$ for $t \leq t_{TCYC}/2$, Power-up: $V_{IH} < 2.6V$ and $V_{DD} < 2.4V$ and $V_{DDQ} < 1.4V$ for $t < 200$ ms.

TAP AC Switching Characteristics Over the Operating Range[6, 7]

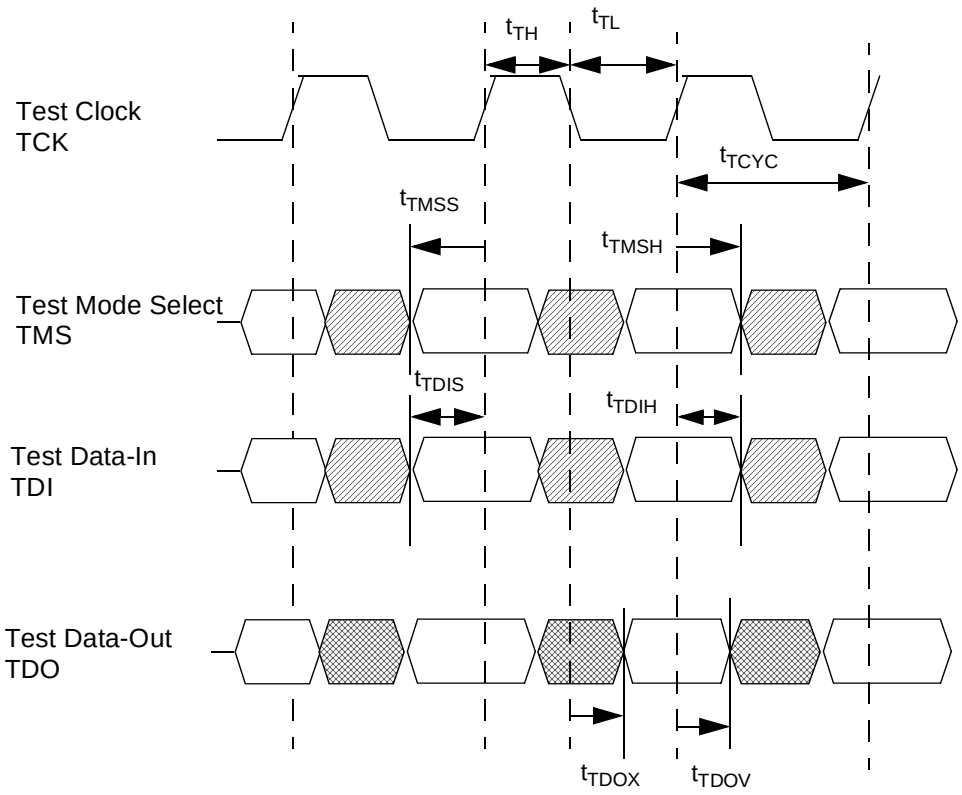
Parameters	Description	Min.	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after Clock Rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

Notes:
6. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
7. Test conditions are specified using the load in TAP AC test conditions. Tr/Tf = 1 ns.

TAP Timing and Test Conditions



(a)



Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	TBD	Reserved for version number.
Device Depth (27:23)	TBD	Defines depth of SRAM.
Device Width (22:18)	TBD	Defines with of the SRAM.
Cypress Device ID (17:12)	TBD	Reserved for future use.
Cypress JEDEC ID (11:1)	TBD	Allows unique identification of SRAM vendor.
ID Register Presence (0)	TBD	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	TBD

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	TBD	TBD	36	TBD	TBD
2	TBD	TBD	37	TBD	TBD
3	TBD	TBD	38	TBD	TBD
4	TBD	TBD	39	TBD	TBD
5	TBD	TBD	40	TBD	TBD
6	TBD	TBD	41	TBD	TBD
7	TBD	TBD	42	TBD	TBD
8	TBD	TBD	43	TBD	TBD
9	TBD	TBD	44	TBD	TBD
10	TBD	TBD	45	TBD	TBD
11	TBD	TBD	46	TBD	TBD
12	TBD	TBD	47	TBD	TBD
13	TBD	TBD	48	TBD	TBD
14	TBD	TBD	49	TBD	TBD
15	TBD	TBD	50	TBD	TBD
16	TBD	TBD	51	TBD	TBD
17	TBD	TBD	52	TBD	TBD
18	TBD	TBD	53	TBD	TBD
19	TBD	TBD	54	TBD	TBD
20	TBD	TBD	55	TBD	TBD
21	TBD	TBD	56	TBD	TBD
22	TBD	TBD	57	TBD	TBD
23	TBD	TBD	58	TBD	TBD
24	TBD	TBD	59	TBD	TBD
25	TBD	TBD	60	TBD	TBD
26	TBD	TBD	61	TBD	TBD
27	TBD	TBD	62	TBD	TBD
28	TBD	TBD	63	TBD	TBD
29	TBD	TBD	64	TBD	TBD
30	TBD	TBD	65	TBD	TBD
31	TBD	TBD	66	TBD	TBD
32	TBD	TBD	67	TBD	TBD
33	TBD	TBD	68	TBD	TBD
34	TBD	TBD	69	TBD	TBD
35	TBD	TBD	70	TBD	TBD

Boundary Scan Order

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
71	TBD	TBD		TBD	TBD
72	TBD	TBD		TBD	TBD
73	TBD	TBD		TBD	TBD
74	TBD	TBD		TBD	TBD
75	TBD	TBD		TBD	TBD
76	TBD	TBD		TBD	TBD
77	TBD	TBD		TBD	TBD
78	TBD	TBD		TBD	TBD
79	TBD	TBD		TBD	TBD
80	TBD	TBD		TBD	TBD
81	TBD	TBD		TBD	TBD
82	TBD	TBD		TBD	TBD
83	TBD	TBD		TBD	TBD
84	TBD	TBD		TBD	TBD
85	TBD	TBD		TBD	TBD
86	TBD	TBD		TBD	TBD
87	TBD	TBD		TBD	TBD
88	TBD	TBD		TBD	TBD
89	TBD	TBD		TBD	TBD
90	TBD	TBD		TBD	TBD
91	TBD	TBD		TBD	TBD
92	TBD	TBD		TBD	TBD
93	TBD	TBD		TBD	TBD
94	TBD	TBD		TBD	TBD
95	TBD	TBD		TBD	TBD
96	TBD	TBD		TBD	TBD
97	TBD	TBD		TBD	TBD
98	TBD	TBD		TBD	TBD
99	TBD	TBD		TBD	TBD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND ..... –0.3V to +3.6V

DC Voltage Applied to Outputs in High Z State[8] ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[8] ..... –0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[9]	V_{DD}/V_{DDQ}
Com'l	0°C to +70°C	2.5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage			2.375	2.625	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA			0.2	V
V_{IH}	Input HIGH Voltage			1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[8]			–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
I_{ZZ}	Input Current of MODE			–30	30	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–2	2	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	5.0-ns cycle, 200 MHz		450	mA
			6.0-ns cycle, 166 MHz		400	mA
			7.5-ns cycle, 133 MHz		350	mA
			10-ns cycle, 100 MHz		325	mA
I_{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	5.0-ns cycle, 200 MHz		90	mA
			6.0-ns cycle, 166 MHz		80	mA
			7.5-ns cycle, 133 MHz		70	mA
			10-ns cycle, 100 MHz		65	mA
I_{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0			10	mA
I_{SB3}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = $1/t_{CYC}$	5.0-ns cycle, 200 MHz		45	mA
			6.0-ns cycle, 166 MHz		40	mA
			7.5-ns cycle, 133 MHz		35	mA
			10-ns cycle, 100 MHz		30	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} ,f = 0			25	mA

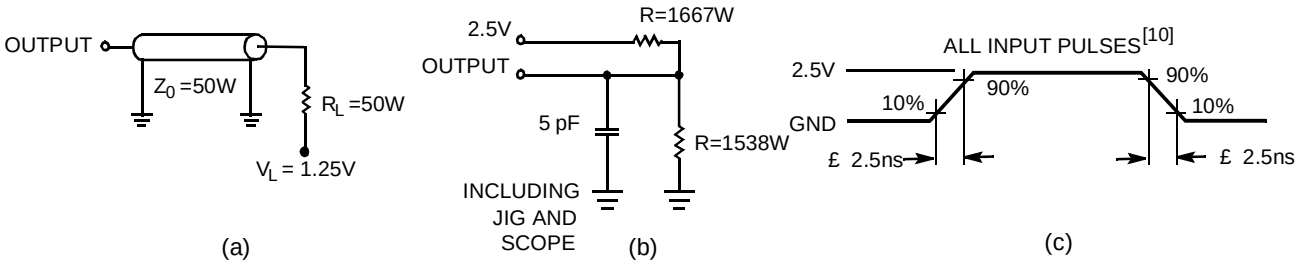
Notes:

8. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
9. T_A is the temperature.

Capacitance[10]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 2.5V, V_{DDQ} = 2.5V	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

AC Test Loads and Waveforms[11]



Notes:
10. Tested initially and after any design or process changes that may affect these parameters.
11. Input waveform should have a slew rate of 1 V/ns.

Switching Characteristics Over the Operating Range[12, 13, 14]

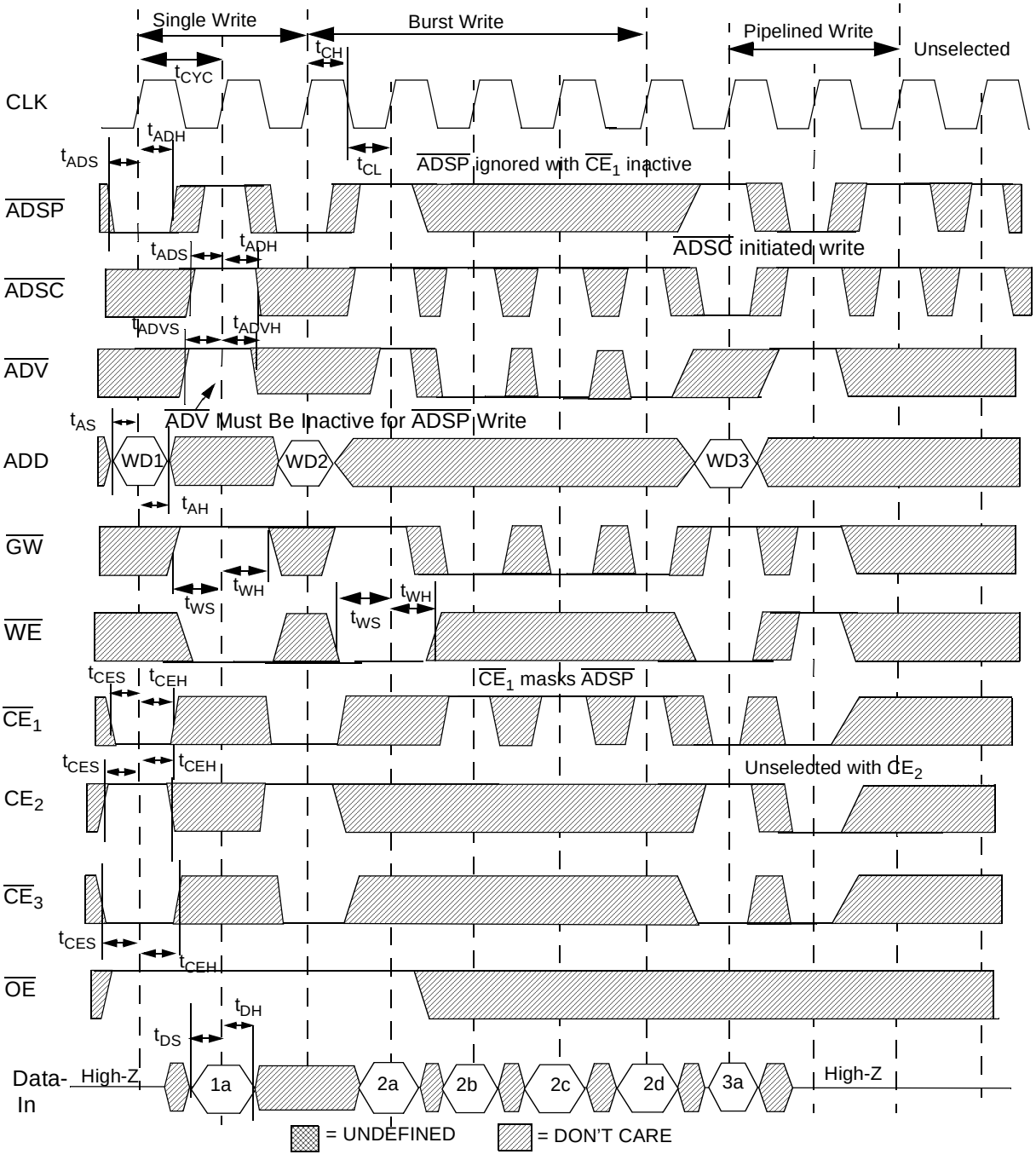
Parameter	Description	-200		-166		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	5.0		6.0		7.5		10		ns
t_{CH}	Clock HIGH	1.6		1.7		1.9		3.2		ns
t_{CL}	Clock LOW	1.6		1.7		1.9		3.2		ns
t_{AS}	Address Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		3.1		3.5		4.2		5.0	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0		1.5		1.5		1.5		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{WES}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_X$ Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		ns
t_{WEH}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_X$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	1.5		1.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CES}	Chip enable Set-Up	1.5		1.5		2.0		2.0		ns
t_{CEH}	Chip enable Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[13]	1.5	3.1	1.5	3.5	1.5	4.2	1.5	5.0	ns
t_{CLZ}	Clock to Low-Z[13]	0		0		0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[13, 14]		3.2		3.5		4.2		4.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[13,14]	0		0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[13]		3.1		3.5		4.2		5.0	ns

Notes:

12. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0 to 2.5V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
13. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
14. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ}.

Switching Waveforms

Write Cycle Timing[15, 16]

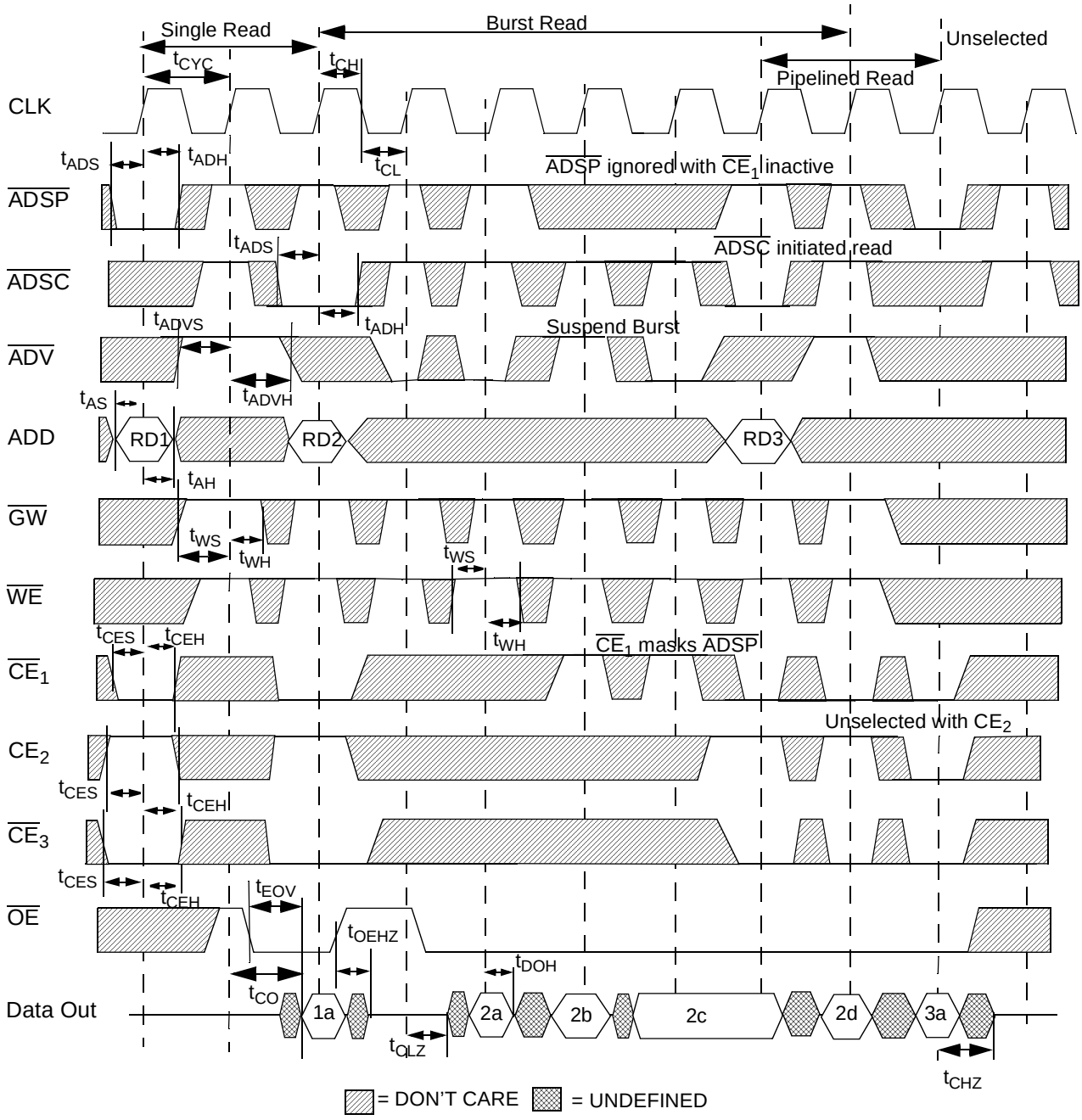


Notes:

15. $\overline{WE}$ is the combination of $\overline{BWE}$, $\overline{BW}$x and $\overline{GW}$ to define a write cycle (see Write Cycle Descriptions table).
16. WDx stands for Write Data to Address X.

Switching Waveforms (continued)

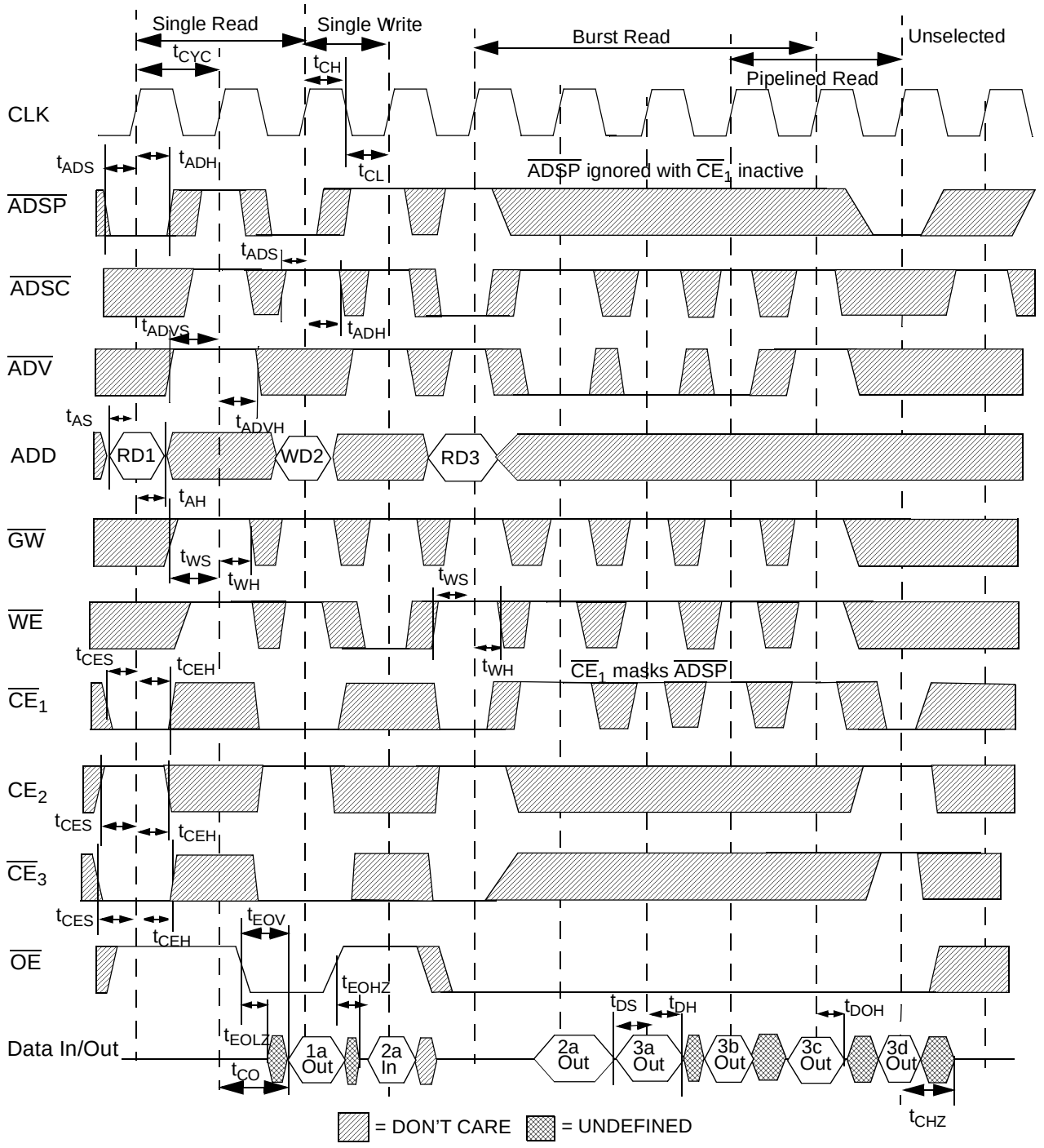
Read Cycle Timing[15, 17]



Note:
17. RDx stands for Read Data from Address X.

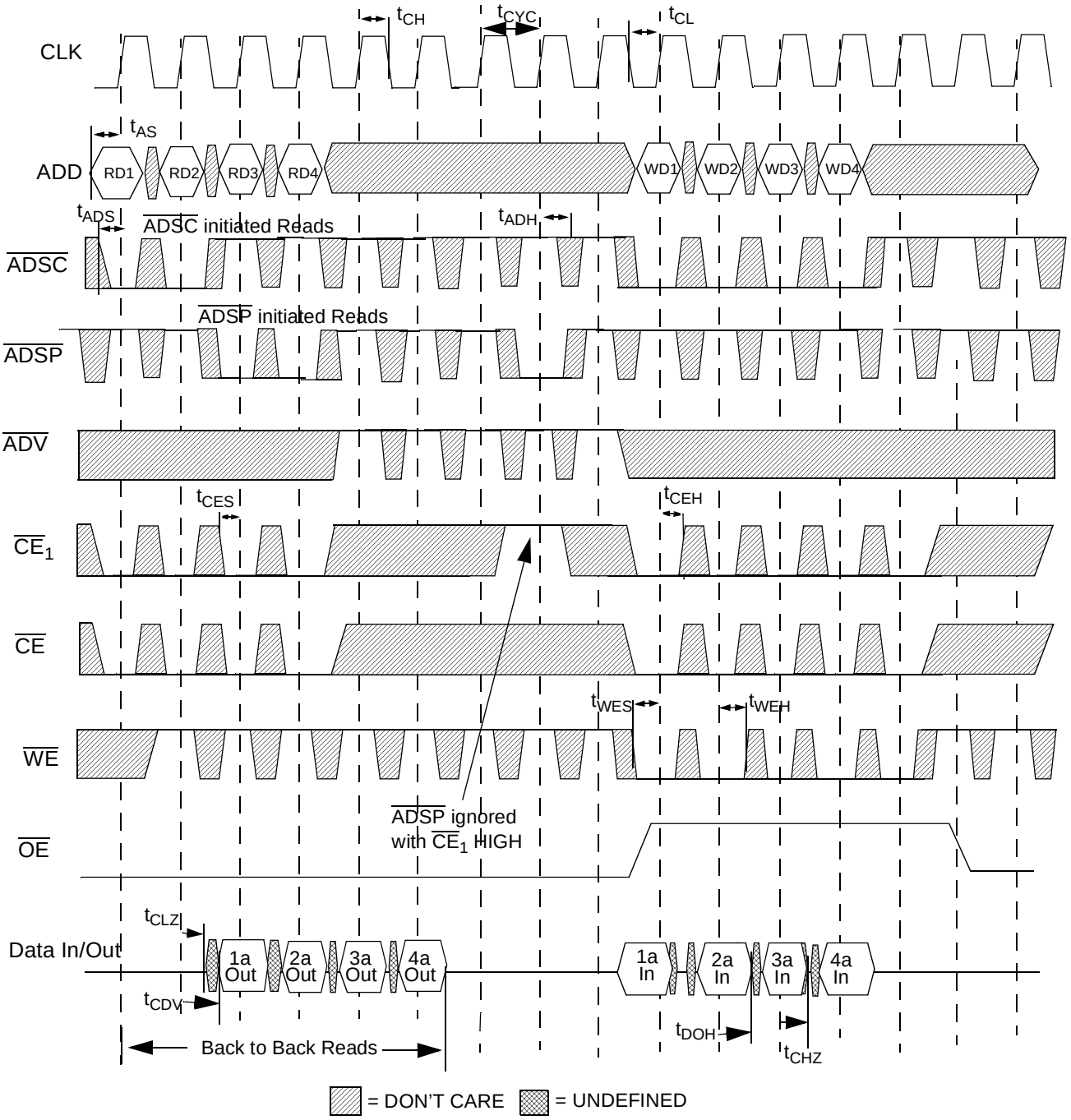
Switching Waveforms (continued)

Read/Write Cycle Timing[15, 16, 17]



Switching Waveforms (continued)

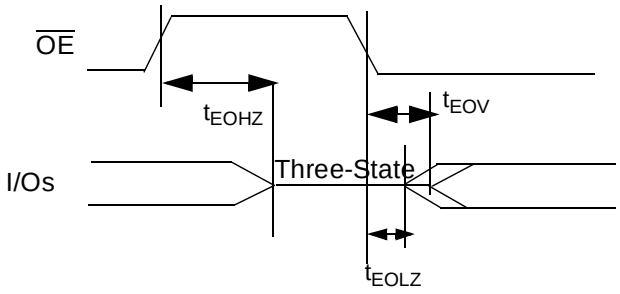
Pipeline Timing[18, 19]



Notes:
18. Device originally deselected.
19. $\overline{CE}$ is the combination of CE_2 and $\overline{CE_3}$. All chip selects need to be active in order to select the device.

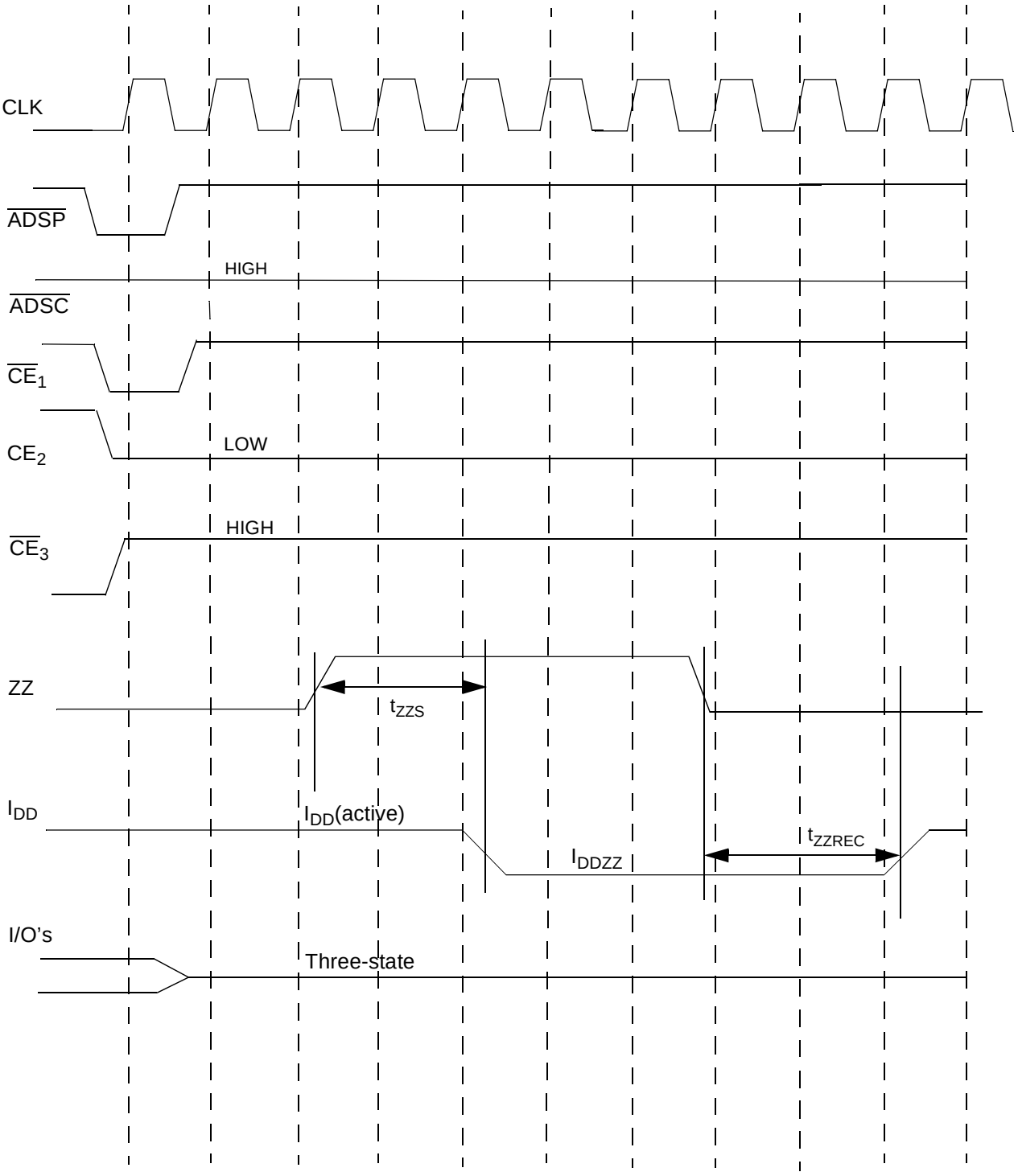
Switching Waveforms (continued)

OE Switching Waveforms



Switching Waveforms (continued)

ZZ Mode Timing [20, 21]



Notes:
20. Device must be deselected when entering ZZ mode. See Cycle Descriptions Table for all possible signal conditions to deselect the device.
21. I/Os are in three-state when exiting ZZ sleep mode.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CY7C1360V25-200AC	A101	100-Lead Thin Quad Flat Pack	Commercial
166	CY7C1360V25-166AC			
133	CY7C1360V25-133AC			
100	CY7C1360V25-100AC			
200	CY7C1362V25-200AC	A101	100-Lead Thin Quad Flat Pack	Commercial
166	CY7C1362V25-166AC			
133	CY7C1362V25-133AC			
100	CY7C1362V25-100AC			
200	CY7C1360V25-200BAC	TBD	119 Ball Fine Pitch BGA	Commercial
166	CY7C1360V25-166BAC			
133	CY7C1360V25-133BAC			
100	CY7C1360V25-100BAC			
200	CY7C1362V25-200BAC	TBD	119 Ball Fine Pitch BGA	Commercial
166	CY7C1362V25-166BAC			
133	CY7C1362V25-133BAC			
100	CY7C1362V25-100BAC			

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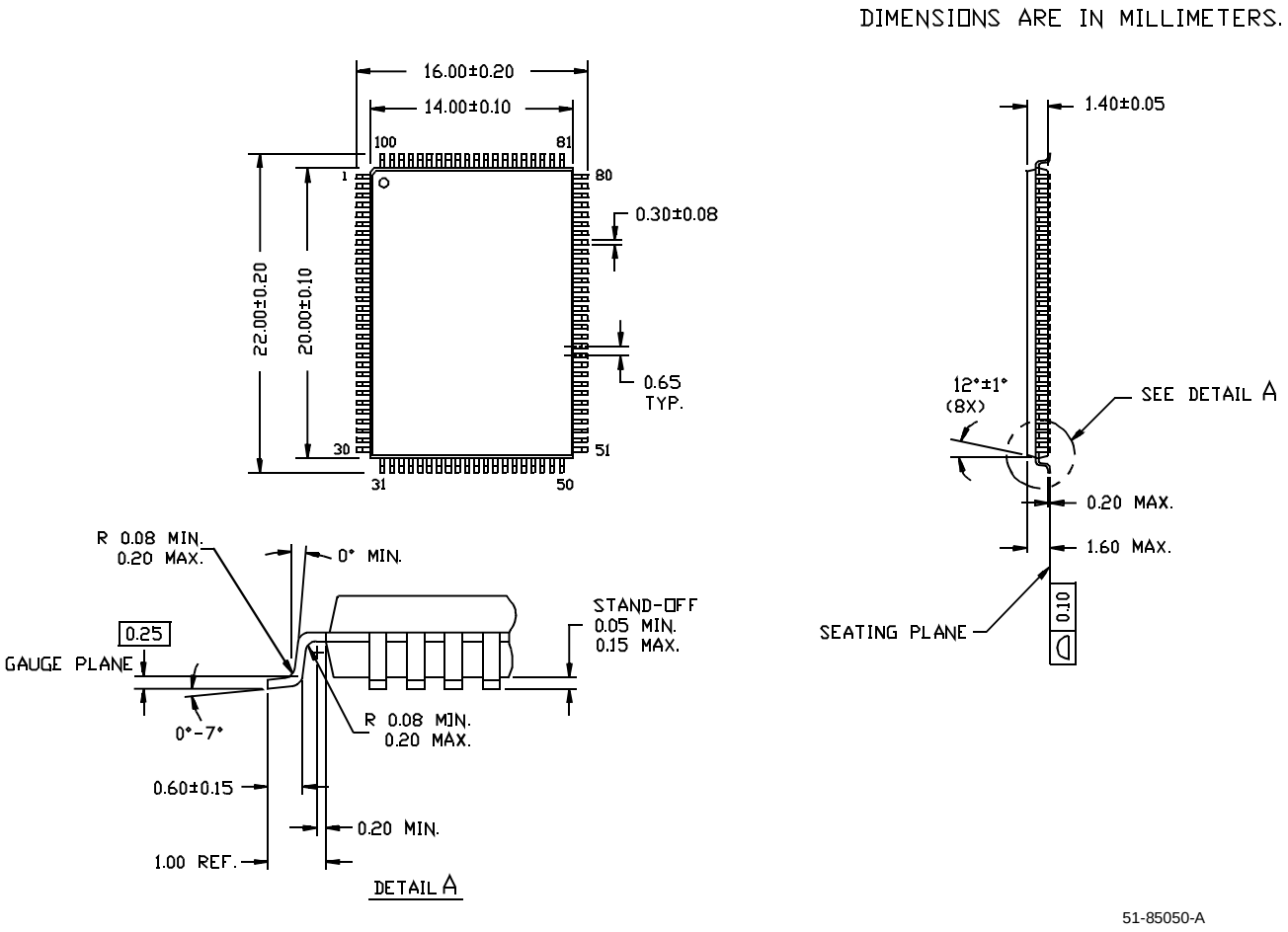
Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-A