Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT 54/74FCT841A/B-
IDT 54/74FCT846A/B*
(Replaces 39C841-46)

FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  - Non-inverting transparent t_{PD} = 5.5ns typ.
  - Inverting transparent t_{PD} = 6.0ns typ.
- Buffered common latch enable, clear and preset input
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

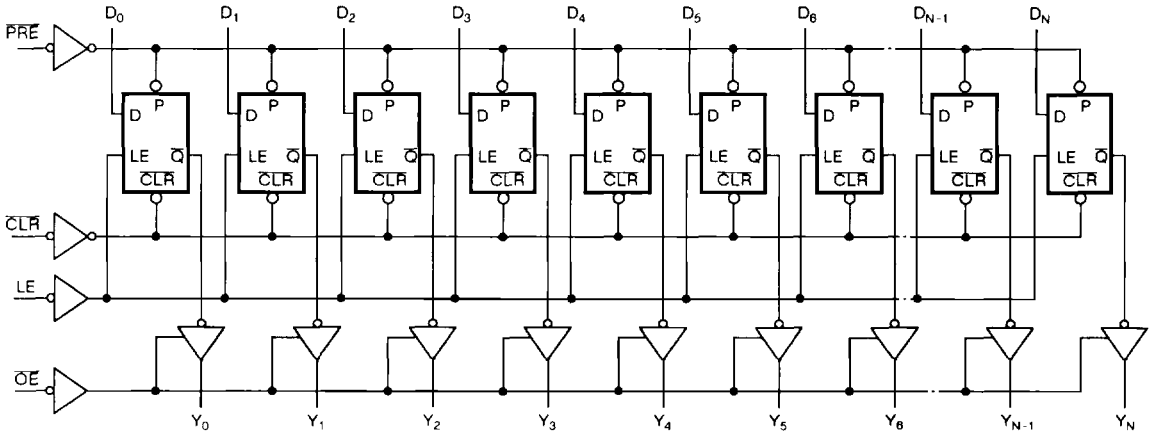
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 and IDT54/74FCT842 are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 and IDT54/74FCT846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT841A/B	54/74FCT843A/B	54/74FCT845A/B
Inverting	54/74FCT842A/B	54/74FCT844A/B	54/74FCT846A/B

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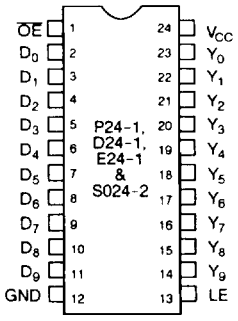
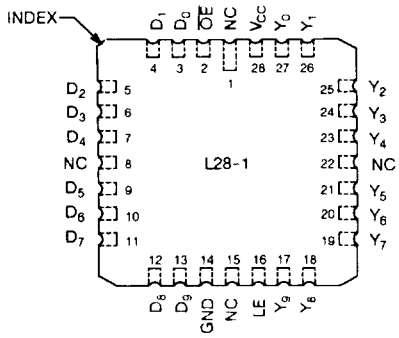
*Advance information only for IDT54/74FCT842 and IDT54/74FCT846.

PIN CONFIGURATIONS

IDT54/74FCT841/IDT54/74FCT842 10-BIT LATCHES

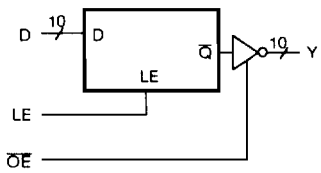


DIP/CERPACK/SOIC
TOP VIEW

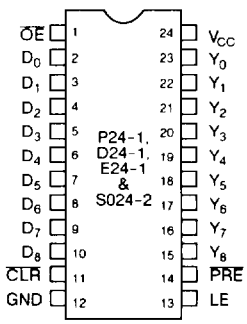


LCC
TOP VIEW

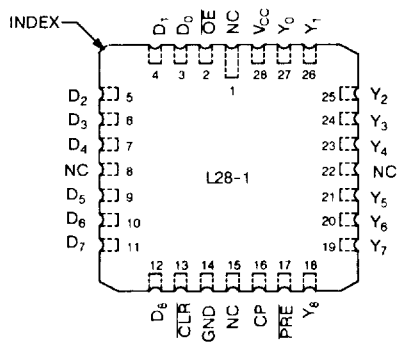
LOGIC SYMBOLS



IDT54/74FCT843/IDT54/74FCT844 9-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW



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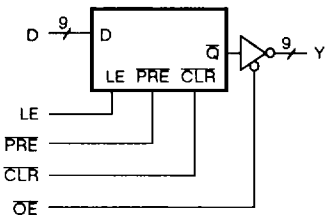
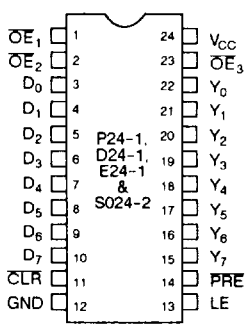
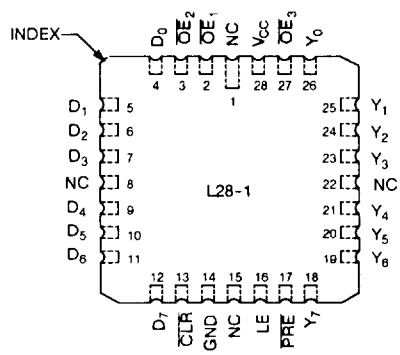
TOP VIEW



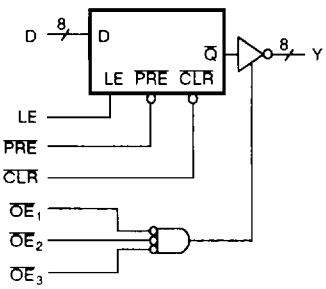
IDT54/74FCT845/IDT54/74FCT846 8-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT841/43/45 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
IDT54/74FCT842/44/46 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES [1]
IDT54/74FCT841/43/45

INPUTS					INTERNAL	OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLES [1]
IDT54/74FCT842/44/46

INPUTS					INTERNAL	OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions apply unless otherwise specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	μA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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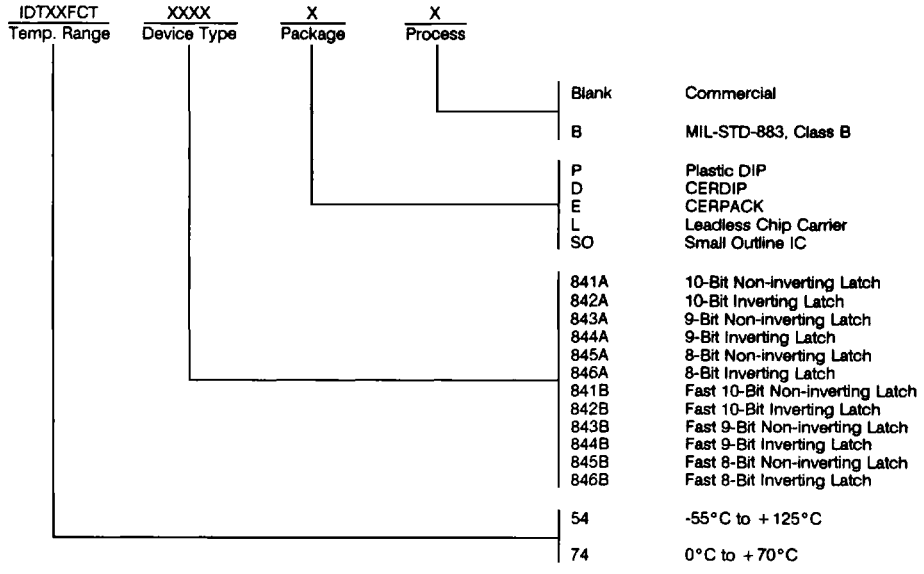
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	IDT54/74FCT841A-46A				IDT54/74FCT841B-46B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} (IDT54/74FCT841, 43, 45) t_{PHL}	Data (D_I) to Output (Y_I) (LE = HIGH)	C_L = 50pF R_L = 500Ω	–	9	–	10	–	6.5	–	7.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	13	–	15	–	13	–	15	ns
t_{SU}	Data to LE Set-up Time	C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns
t_H	Data to LE Hold Time		2.5	–	3	–	2.5	–	2.5	–	ns
t_{PLH} (IDT54/74FCT842, 44, 46) t_{PHL}	Data (D_I) to Output (Y_I) (LE = HIGH)	C_L = 50pF R_L = 500Ω	–	10	–	12	–	8.0	–	9.0	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	13	–	15	–	13	–	15	ns
t_{SU}	Data to LE Set-up Time	C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns
t_H	Data to LE Hold Time		2.5	–	3	–	2.5	–	2.5	–	ns
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_I	C_L = 50pF R_L = 500Ω	–	12	–	13	–	8.0	–	10.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	16	–	20	–	15.5	–	18	ns
t_{PLH}	Propagation Delay, Preset to Y_I	C_L = 50pF R_L = 500Ω	–	12	–	14	–	8.0	–	10	ns
t_{SU}	Preset Recovery ($\overline{PRE}$ ↓) Time		–	14	–	17	–	10	–	13	ns
t_{PHL}	Propagation Delay, Clear to Y_I		–	13	–	14	–	10	–	11	ns
t_{SU}	Clear Recovery ($\overline{CLR}$ ↓) Time		–	14	–	17	–	10	–	10	ns
t_{PWH}	LE Pulse Width HIGH	C_L = 50pF R_L = 500Ω	4	–	5	–	4	–	4	–	ns
t_{PWL}	Preset Pulse Width LOW		5	–	7	–	4	–	4	–	ns
t_{PWL}	Clear Pulse Width LOW		4	–	5	–	4	–	4	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ↑ to Y_I	C_L = 50pF R_L = 500Ω	–	11.5	–	13.0	–	8	–	8.5	ns
t_{PZH} t_{PZL}		C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	14	–	15	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ↓ to Y_I	C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6	–	6.5	ns
t_{PHZ} t_{PLZ}		C_L = 50pF R_L = 500Ω	–	8	–	10	–	7.0	–	7.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

ORDERING INFORMATION



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