

OBJECTIVE SPECIFICATION



GM76C256 32,768x8 BIT STATIC RAM HIGH PERFORMANCE

Description

The GM76C256 is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a typical operating current of 80mW/MHz and minimum cycle time of 85ns. When \overline{CS} is a logical high, the device is placed in low power standby mode in which standby current is 2mA typically. The GM76C256 has two control inputs. Chip select (\overline{CS}) allow for device selection and data retention control, and an output enable input (\overline{OE}) provides fast memory access. Thus the GM76C256 is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256 is offered in 28 pin DIP(600mil) and SOP(330mil).

Feature

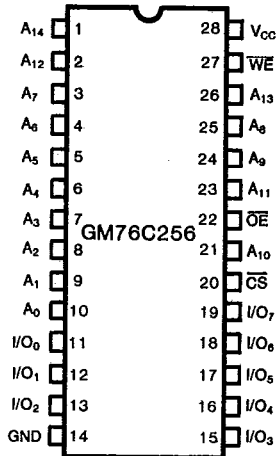
- High Speed: Fast Access and Cycle Time
85/100/120/150 ns(Max.)
- Low Power Standby and Low Power Operation;
Stand by : 1mW(Typ)
Operation: 80mW (Typ, f=1MHz)
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Standard 28 DIP and SOP
- Capability of Battery Back up Operation

Pin Name

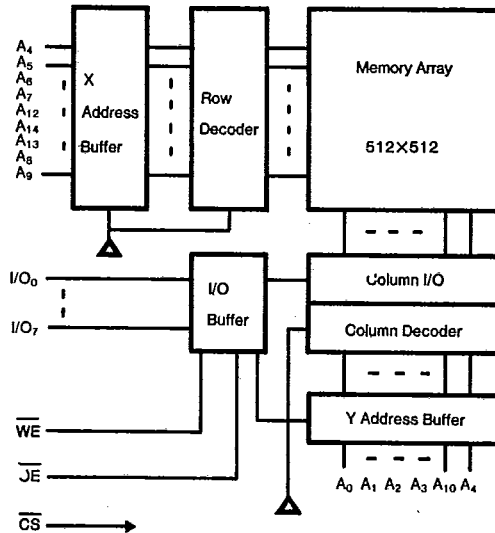
- $A_0 \sim A_{14}$: Address Input
- \overline{WE} : Write Enable Input
- \overline{OE} : Output Enable Input
- \overline{CS} : Chip Select Input
- $I/O_0 \sim I/O_7$: Data Input/Output
- V_{CC} : Power Supply, +5V
- GND : Ground

Pin Configuration

T-46-23-14



Block Diagram



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GM76C256

Absolute Maximum Ratings

Input Voltage	V_{IN}	-3.0 to 7.0V
Supply Voltage	V_{CC}	-0.5 to 7.0V
Supply Voltage Applied to Outputs High Z State	V_{CC} (High Z)	-0.5 to 7.0V
Storage Temperature	T_{STG}	-65 to +150°C
Storage Temperature with Power Supplied	T_{power}	-55 to +125°C
Output Current Into Output	I_O	10mA

Recommended Operating Condition: $T_A=0^\circ\sim 70^\circ\text{C}$

Supply Voltage	V_{CC}	4.5 to 5.5V
Input High Voltage	V_{IH}	2.2 to 6V
Input Low Voltage	V_{IL}	-3.0 to 0.8V
Data Retention Supply Voltage	V_{DH}	2.0 to 5.5V

DC Electrical Characteristics: ($V_{CC}=5V\pm 10\%$, $T_A=0^\circ\sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	TEST CONDITIONS	GM76C256		UNITS
			MIN	MAX	
V_{OH}	Output High Voltage	$V_{CC}=\text{Min}$, $I_{OH}=-1.0\text{mA}$	2.4		V
V_{OL}	Output Low Voltage	$V_{CC}=\text{Min}$, $I_{OL}=2.1\text{mA}$		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC}	V
V_{IL}	Input Low Voltage		-3.0	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_I \leq V_{CC}$	-10	10	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_I$, V_{CC} Output Disabled	-10	10	μA
I_{SB}	Stand-by Power	$\overline{\text{CS}}=V_{IH}$		5	mA
I_{SB1}	Supply Current	$\overline{\text{CS}}=V_{CC}-0.2\text{V}$		200	μA
I_{CC}	Operating Supply Current	$\overline{\text{CS}}=V_{IL}$, $I_{IO}=0\text{mA}$		25	mA
I_{CC1}	Average Operating Power Supply Current	Min Cycle, duty=100% $I_{IO}=0\text{mA}$		80	mA

AC Operating Characteristics: $V_{CC}=5V\pm 10\%$, $T_A=0^\circ\sim 70^\circ\text{C}$ (Note 2)

• Read Cycle

SYMBOL	PARAMETER	GM76C256-85		GM76C256-10		GM76C256-12		GM76C256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	85	—	100	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	—	150	ns
t_{OE}	Output Enable to Output Valid	—	45	—	50	—	60	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	10	—	10	—	10	—	ns
t_{CLZ}	Chip Selection to Output in Low Z	10	—	10	—	10	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low Z	6	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	30	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	0	40	0	50	ns

GM76C256

AC Operating Characteristics: $V_{CC}=5V \pm 10\%$, $T_A=0^\circ \sim 70^\circ C$

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• Write Cycle

SYMBOL	PARAMETER	GM76C256-85		GM76C256-10		GM76C256-12		GM76C256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	85	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	75	—	80	—	85	—	150	—	ns
t_{AW}	Address Valid to End of Write	75	—	80	—	85	—	100	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	60	—	60	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	10	—	0	—	0	—	0	—	ns
t_{WHZ}	Write to Output in High Z	0	30	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	40	—	40	—	50	—	60	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTES:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- AC operating conditions assume signal transition times of 5ns or less limiting reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- t_{HZOE} and t_{HZCE} are tested with $C_L=5$ pF as in Figure 1b condition is measured ± 500 mV from steady state voltage.
- By given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for all devices. These parameters are sampled and not 100% tested.
- The internal write time of the memory is defined by the overlap of \overline{CE} low and \overline{WE} low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- \overline{WE} is high for read cycle.
- Device is continuously selected. $\overline{OE}, \overline{CE} = V_L$
- Address valid prior to or coincident with \overline{CE} transition low.

Capacitance

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	$T_A=25^\circ C, f=1$ MHz		6	pF
C_{OUT}	Output Capacitance	$V_{CC}=5.0V$		8	

Notes: Tested on a sample basis

AC Test Loads and Waveforms

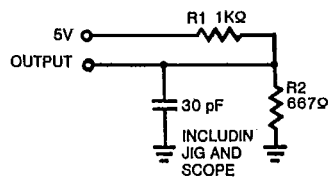


Figure 1a

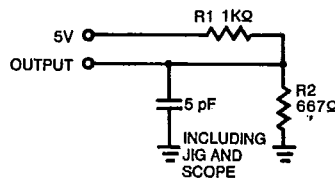


Figure 1b

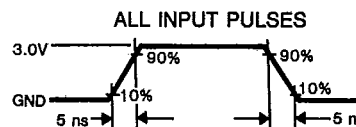
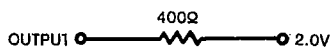


Figure 2

THEVENIN EQUIVALENT

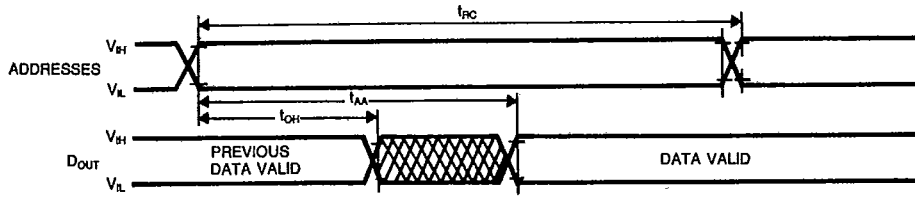


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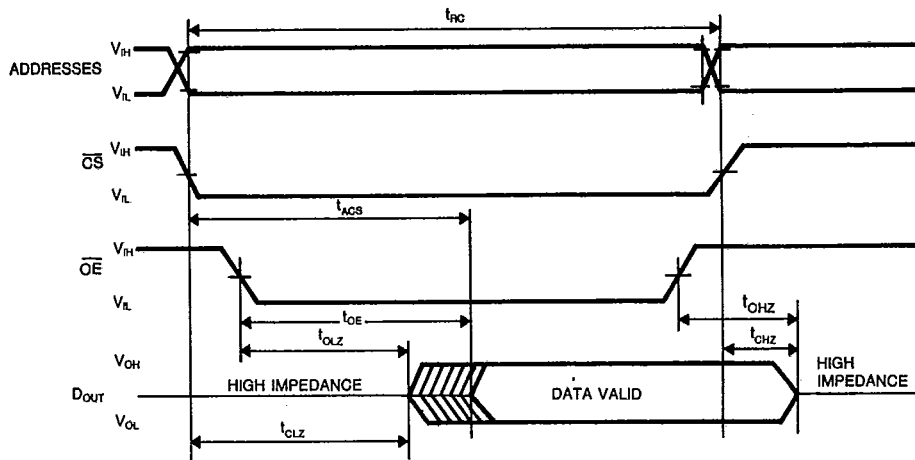
Timing Waveforms

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Read Cycle 1 (Notes 6,7)



Read Cycle 2 (Notes 6,8)

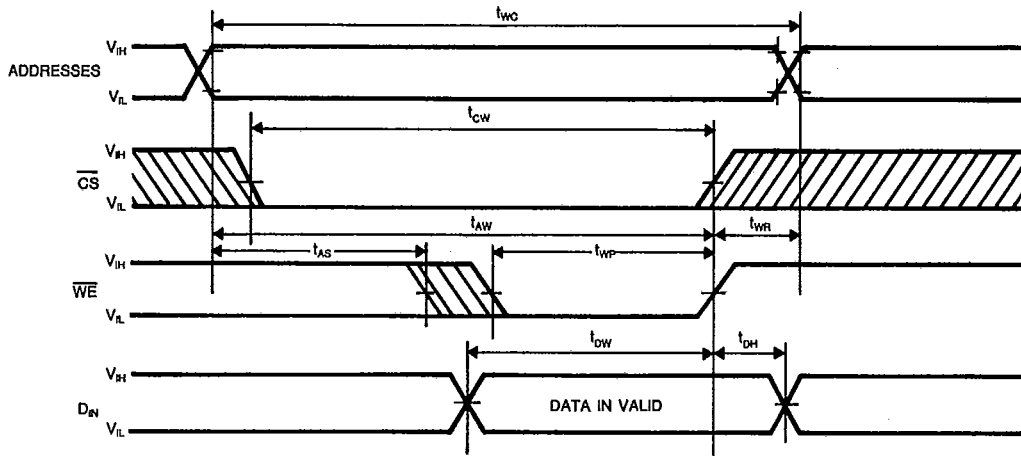


GM76C256

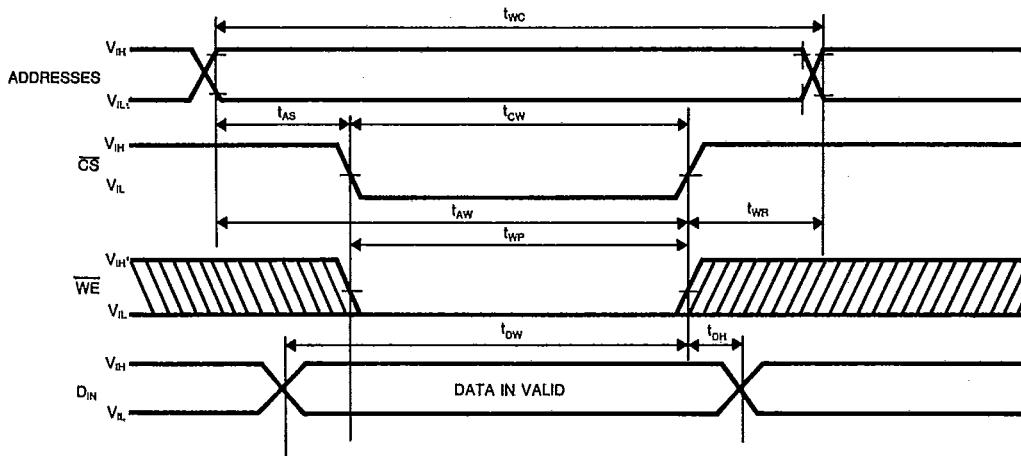
Timing Waveforms

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Write Cycle 1 (\overline{WE} Controlled) (Note 5)



Write Cycle 2 (\overline{CS} Controlled) (Note 5)



Note: If \overline{CS} goes high simultaneously with \overline{WE} High, the output remains in a high impedance state.

GM76C256

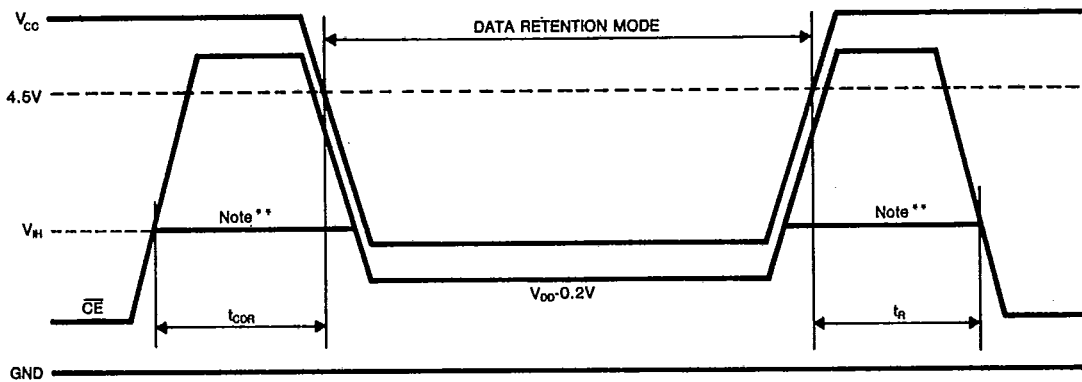
Data Retention Characteristics: ($T_A=0^{\circ}\sim 70^{\circ}\text{C}$)

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SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{DH}	Data Retention Supply Voltage	2.0	5.5	V	$\overline{CS} \geq V_{CC} - 0.2V$
I_{DSS2}	Data Retention Current	—	50	μA	$V_{CC}=3.0V,$ $\overline{CS} \geq 2.8V$
t_{CDR}	Chip Deselection to Data Retention Mode	0	—	ns	
t_R	Recovery Time	t_{RC}	—	ns	

Note*: Read Cycle Time

\overline{CE} Controlled Data Retention Mode

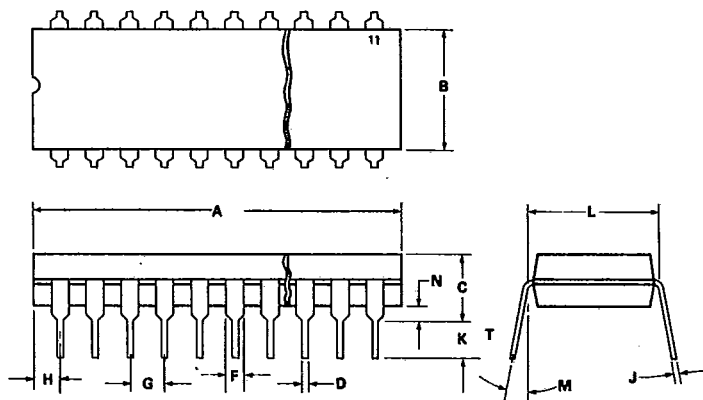


Note **: If the V_H of \overline{CS} is 2.2V in operation, I_{DSS1} current flows during the period that the V_{CC} voltage is going down from 4.5V to 2.2V

PACKAGE DIMENSION

PLASTIC DIP

T-90-20



(UNIT: INCHES)

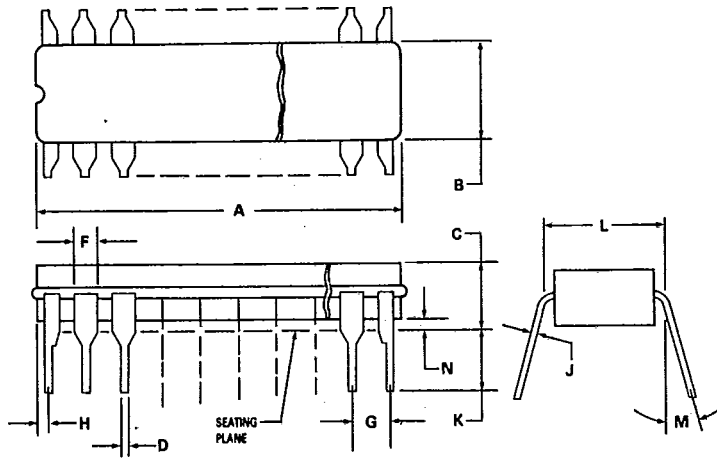
SYMBOL	16 PIN		18 PIN		20 PIN		22 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.738	0.752	0.875	0.900	1.013	1.040	1.095	1.150
B	0.245	0.255	0.245	0.255	0.263	0.273	0.260	0.287
C	0.143	0.152	0.145	0.162	0.143	0.152	0.145	0.160
D	TYP. 0.018		TYP. 0.018		TYP. 0.018		TYP. 0.018	
F	TYP. 0.063		TYP. 0.060		TYP. 0.065		TYP. 0.060	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.015	0.030	0.04	0.05	0.058	0.066	—	0.075
J	0.009	0.014	0.009	0.015	0.009	0.010	0.009	0.010
K	0.125	0.145	0.125	0.130	0.125	0.132	0.125	0.142
L	0.300 BSC		0.300 BSC		0.300 BSC		0.300 BSC	
M	0'	10'	0'	10'	0'	10'	0'	10'
N	0.015	—	0.015	—	0.015	—	0.015	—

SYMBOL	24 PIN		28 PIN					
	MIN	MAX	MIN	MAX				
A	1.243	1.260	1.415	1.460				
B	0.535	0.545	0.535	0.545				
C	0.158	0.170	0.158	0.170				
D	TYP. 0.018		TYP. 0.018					
F	TYP. 0.060		TYP. 0.060					
G	0.09	0.11	0.09	0.11				
H	0.06	0.075	0.06	0.076				
J	0.009	0.015	0.009	0.015				
K	0.125	0.132	0.125	0.132				
L	0.600	0.625	0.600	0.620				
M	0'	10'	0'	10'				
N	0.008	—	0.008	—				

PACKAGE DIMENSION

T-90-20

CER DIP



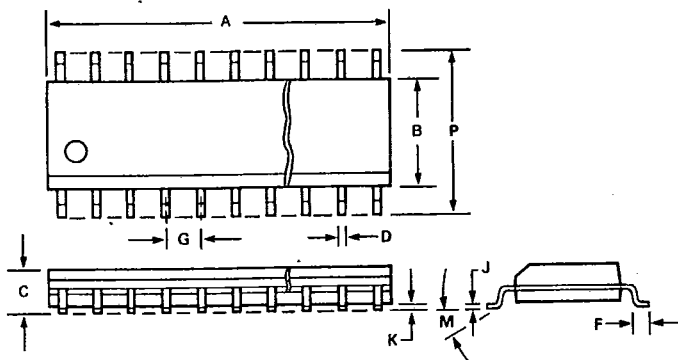
(UNIT : INCHES)

SYMBOL	16 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.753	0.785	0.940	0.985	1.240	1.290	1.440	1.485
B	0.272	0.294	0.265	0.306	0.514	0.526	0.514	0.598
C	0.165	0.200	0.165	0.200	0.165	0.200		0.225
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.023
F	0.055	0.065	0.055	0.065	0.055	0.065	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.012	0.060	0.012	0.060	0.040	0.098	0.040	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.590	0.620	0.590	0.620
M	0'	10'	0'	10'	0'	10'	0'	10'
N	0.02	0.06	0.02	0.07	0.02	0.07	0.02	0.07

PACKAGE DIMENSION

SOP

T-90-20



(UNIT : INCHES)

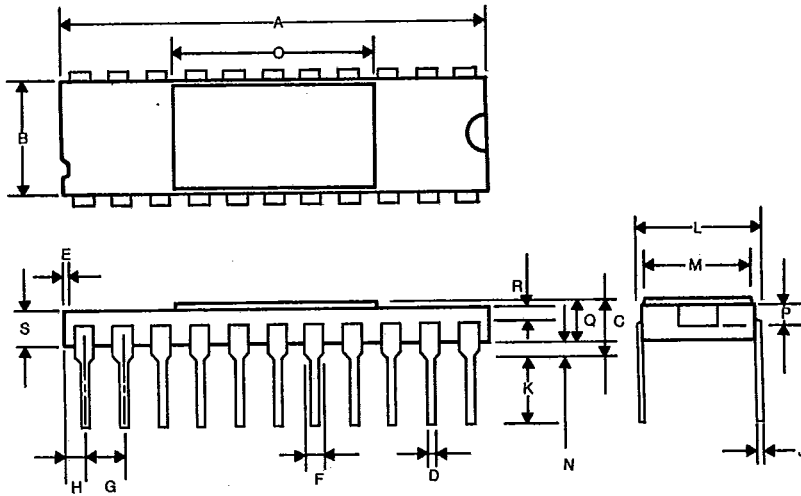
CODE NO. PIN SYMBOL	20 F		24 F		24 FW			
	20 PIN		24 PIN		24 PIN			
	MIN	MAX	MIN	MAX	MIN	MAX		
A	0.496	0.510	0.602	0.614	0.622	0.638		
B	0.292	0.299	0.292	0.299	TYP. 0.331			
C	0.097	0.104	0.097	0.104	—	0.098		
D	0.014	0.019	0.014	0.019	0.012	0.018		
F	0.018	0.035	0.018	0.035	TYP 0.039			
G	0.050 BSC		0.050 BSC		0.050 BSC			
J	0.010 BSC		0.010 BSC		0.010 BSC			
K	0.004	0.008	0.0055	0.0115	0.004	—		
P	0.400	0.410	0.400	0.410	0.453	0.477		
M	0'	8'	0'	8'	—	—		

CODE NO. PIN SYMBOL	28 F		28 FW			
	28 PIN		28 PIN			
	MIN	MAX	MIN	MAX		
A	0.703	0.712	0.720	0.750		
B	0.292	0.289	TYP. 0.331			
C	0.097	0.104	—	0.098		
D	0.014	0.019	0.012	0.018		
F	0.018	0.035	TYP. 0.039			
G	0.050 BSC		0.050 BSC			
J	0.010 BSC		0.010 BSC			
K	0.0055	0.0115	0.004	—		
P	0.400	0.410	0.453	0.477		
M	0'	8'	—	—		

PACKAGE DIMENSION

SIDE BRAZED

T-90-20



(UNIT: INCHES)

SYMBOL	22 PIN	
	MIN	MAX
A	1.088	1.112
B	0.281	0.298
C	—	0.160
D	0.016	0.020
E	0.004	—
F	TYP. 0.050	
G	0.09	0.105
H	0.035	0.065
J	0.009	0.011

SYMBOL	22 PIN	
	MIN	MAX
K	0.14	0.170
L	0.290	0.310
M	0.265	0.275
N	0.020	0.050
O	0.555	0.565
P	TYP. 0.050	
Q	0.092	0.122
R	0.005	—
S	0.08	—