Comlinear Corporation

Quad, Wideband Monolithic Op Amp

CLC430

T-79-07-20

APPLICATIONS:
- video distribution
- multiple-line driver
- analog bus driver
- video signal multiplexing
- DAC output buffer
- CCD amplifer

FEATURES (typical):
- 55MHz small-signal bandwidth ($4V_{pp}$)
- 2000 V/µs slew rate
- ± 5V to ± 15V supplies
- 100ns disable to high-impedance output
- 85mA continuous output current
- 0.02%/0.04° differential gain/phase
- high common mode input voltage

DESCRIPTION:

The CLC 430 is a high-speed, monolithic operational amplifier employing Comlinear's proprietary current feedback architecture. Equipped with a very fast disable/enable feature, the CLC430 is designed specifically for video switching and distribution systems. The CLC430's high-speed operation includes a 55MHz small signal bandwidth (4Vpp) and a 2000V/µs slew rate while requiring only 11mA quiescent current. Since the CLC430 is designed to operate over a wide range of supply voltages, there is little degradation in performance between ±5V and ±15V operation.

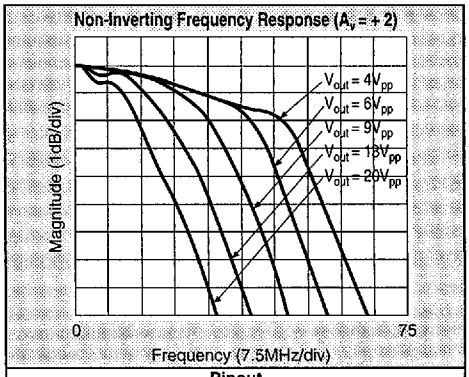
The CLC430 is designed to drive video speed signals through multiple 75Ω or 50Ω channels while maintaining excellent differential gain and phase performance. The disable/enable feature allows the CLC430 to be used in video switching and multiplexing applications with its quick turn-off (100ns) and turn-on (200ns). Switched into disable mode, the CLC430 provides a high impedance output while drawing only 1.5mA supply current. Multiplexing video signals onto an analog bus can easily be achieved by combining parallel CLC430s to form a common output. And since "break before make" is guaranteed, the disable pins of the paralleled combination can be driven with the same signal source.

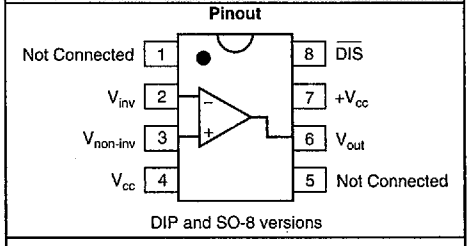
Applications with large DC components, such as CCD amplifiers will enjoy the CLC430's high common mode input range and wide signal swing.

The CLC430 is available in several versions to meet a variety of requirements.

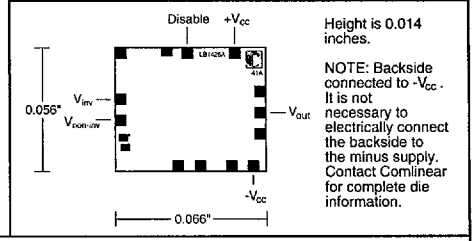
CLC430AJP	−40°C to +85°C	8-pin plastic DIP
CLC430AJE	−40°C to +85°C	8-pin plastic SOIC
CLC430AIB	−40°C to +85°C	8-pin hermetic CERDIP
CLC430A8B	−55°C to +125°C	8-pin hermetic CERDIP MIL-STD-883, Level B
CLC430ALC	−55°C to +125°C	dice
CLC430AMC	−55°C to +125°C	dice qualified to Method 5008, MIL- STD-883, Level B

Contact factory for other packages. DESC SMD number 5962-92030.





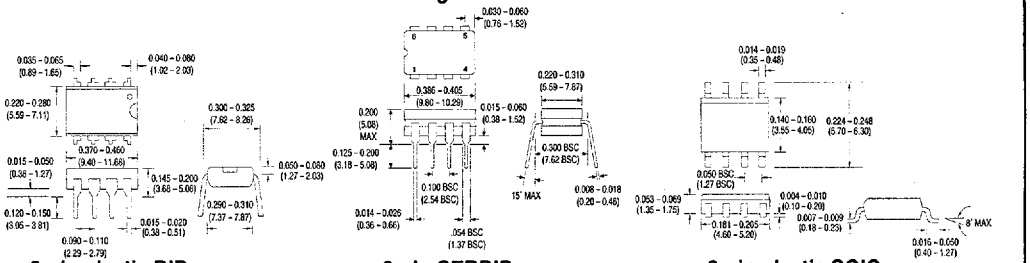
DIP and SO-8 versions



Height is 0.014 inches.

NOTE: Backside connected to -V_{cc}. It is not necessary to electrically connect the backside to the minus supply. Contact Comlinear for complete die information.

Package Dimensions



8-pin plastic DIP | 8-pin CERDIP | 8-pin plastic SOIC

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Electrical Characteristics (A_V=+2; $\pm V_{cc}$=±15V; R_L = 100Ω; R_f = 750Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC430AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC430A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN PERFORMANCE							
† −3dB bandwidth	V_{out} <4V_{pp}(note 1)	55	30	30	25	MHz	SSBW
	V_{out} <10V_{pp}	27	20	20	16	MHz	LSBW
gain flatness[2]	V_{out} <4V_{pp}(note 1)						
† peaking	DC to 10MHz	0.2	0.5	0.5	0.6	dB	GFPL
† peaking	DC to 10MHz	0.2	0.5	0.5	0.6	dB	GFPH
† rolloff	DC to 20MHz	0.5	1.5	1.5	1.8	dB	GFR
linear phase deviation	DC to 20MHZ	0.3	1.8	1.8	2.3	°	LPD
diff. gain pos/neg sync	4.43MHz,150Ω load	0.02	0.07/0.04	0.07/0.04	0.10/0.05	%	DG
diff. phase pos/neg sync	4.43MHz,150Ω load	0.04	0.20/0.07	0.20/0.07	0.25/0.15	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	10V step	10	16	14	16	ns	TRL
settling time to 0.05%	2V step	35	50	50	60	ns	TS
overshoot	2V step, 1ns rise/fall	0	8	5	8	%	OS
slew rate	V_{out} = ±10V	2000	1400	1500	1400	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 10MHz	40	34	34	34	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 10MHz	53	43	46	46	dBc	HD3
equivalent noise input							
voltage	>1MHz	3	3.5	3.5	4.0	nV/√Hz	VN
inverting current	>1MHz	15	21	18	21	pA/√Hz	ICI
non-inverting current	>1MHz	4	7	6	7	pA/√Hz	ICN
noise floor	>1MHz	−151	−148	−148	−148	dBm_{1Hz}	SNF
integrated input noise	1MHz to 100MHz	63	90	90	90	µV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		±2	±11	±7.5	±11	mV	VIO
average temperature coefficient		±25	+50	—	+50	µV/°C	DVIO
*input bias current	non-inverting	±3	±22	±14	+10	µA	IBN
average temperature coefficient		±10	±160	—	±80	nA/°C	DIBN
*input bias current	inverting	±3	±18	±14	±12	µA	IBI
average temperature coefficient		±10	±100	—	±50	nA°C	DIBI
•power supply rejection ratio		62	53	56	53	dB	PSRR
♠common mode rejection ratio		62	52	54	52	dB	CMRR
*supply current	no load	11	15	12	12	mA	ICC
supply current	disabled	1.5	2.5	2.0	2.5	mA	ICCD
SWITCHING PERFORMANCE (break before make is guaranteed)							
turn on time		200	300	300	350	ns	TON
turn off time		100	200	200	200	ns	TOFF
off isolation	10MHz	59	56	56	56	dB	ISO
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		8000	1500	3000	5000	kΩ	RIN
non-inverting input capacitance		0.5	1.0	1.0	1.0	pF	CIN
output voltage range	R_L=100Ω	±8	±6	±6	±4	V	VOL
output voltage range	no load	±13	±12	±12	±12	V	VO
common mode input range		±11	±10	±10	±10	V	CMIR
output current		±85	±60	±60	±45	mA	IO

Absolute Maximum Ratings

V_{cc}	±18V
I_{out} output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed...	125mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	±15V
maximum junction temperature	+175°C
operating temperature range	
AJ/AI:	−40°C to +85°C
A8/AL/AM:	−55°C to +125°C
storage temperature range	−65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

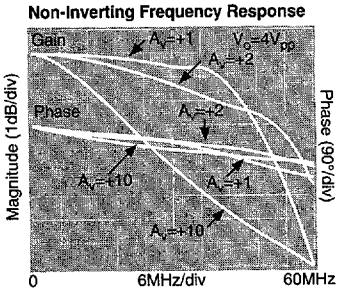
recommended gain range: ±1 to ±10

Notes:

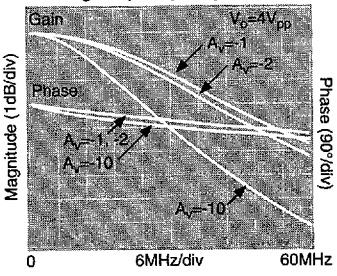
*	AI, AJ	100% tested at +25°C, sample at +85°C.
†	AJ	Sample tested at +25°C.
†	AI	100% tested at +25°C.
*	A8	100% tested +25°C, −55°C, +125°C.
†	A8	100% tested +25°C, sample at −55°C, +125°C.
*	AL, AM	100% wafer probed at +25°C to +25°C min/max specifications.
♠	SMD	Sample tested at +25°C, −55°C, +125°C.
note 1:		Specification is guaranteed for V_{out} = 4V_{pp} but is tested with V_{out} = 0.63 V_{pp}.
note 2:		Gain flatness test performed from 0.1MHz.

Typical Performance Characteristics (T_A = 25°C, A_V = +2, $\pm V_{CC}$ = ±15V, R_L=100Ω, R_f = 750Ω)

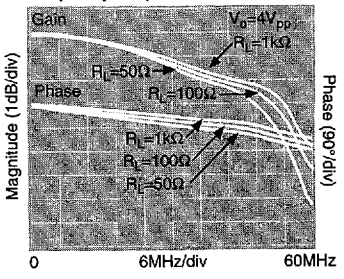
Non-Inverting Frequency Response



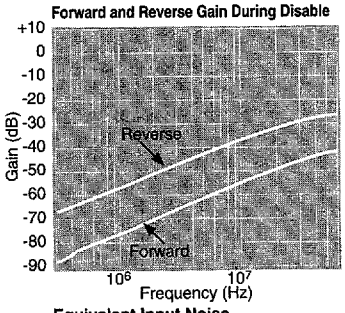
Inverting Frequency Response



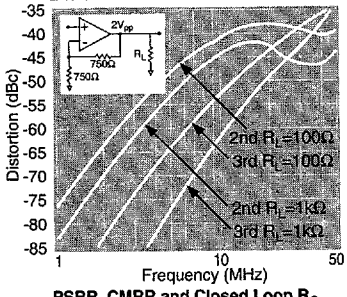
Frequency Response vs.Load



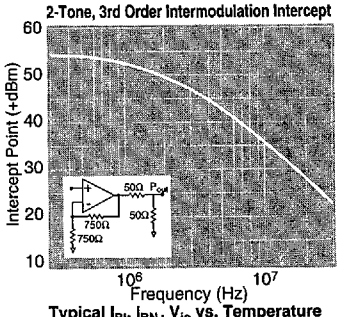
Forward and Reverse Gain During Disable



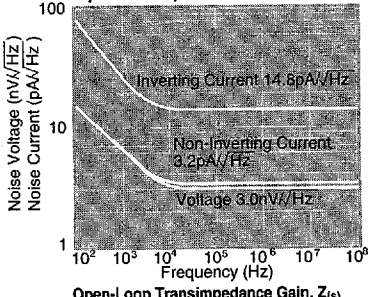
2nd and 3rd Harmonic Distortion



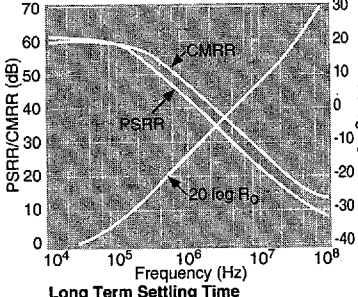
2-Tone, 3rd Order Intermodulation Intercept



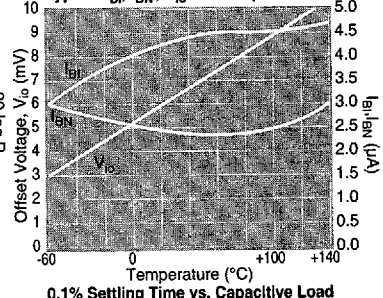
Equivalent Input Noise



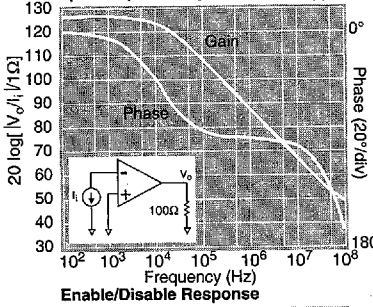
PSRR, CMRR and Closed Loop R_O



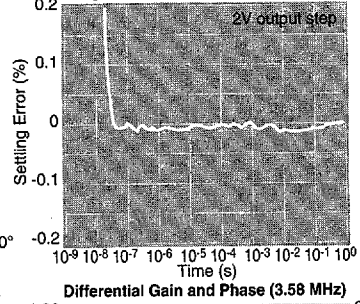
Typical I_{BI}, I_{BN}, V_{IO} vs. Temperature



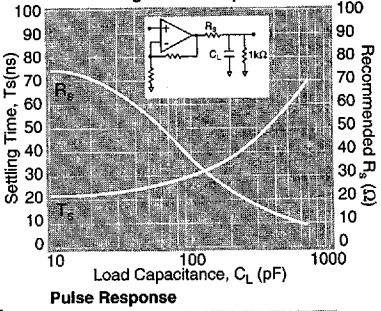
Open-Loop Transimpedance Gain, $Z_{(s)}$



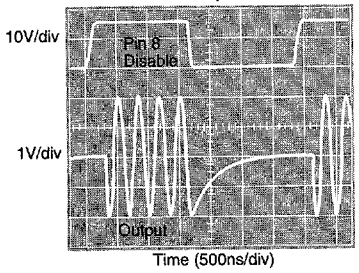
Long Term Settling Time



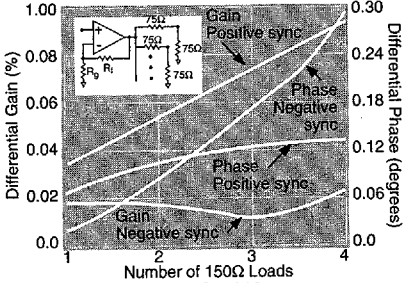
0.1% Settling Time vs. Capacitive Load



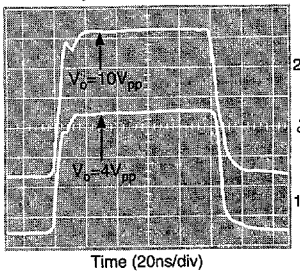
Enable/Disable Response



Differential Gain and Phase (3.58 MHz)



Pulse Response



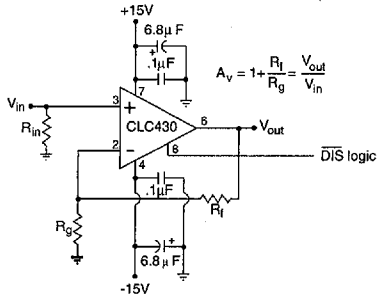


Figure 1: recommended non-inverting gain circuit

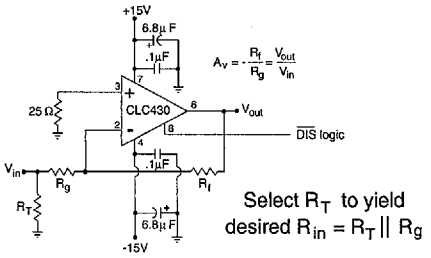


Figure 2: recommended inverting gain circuit

Figure 3

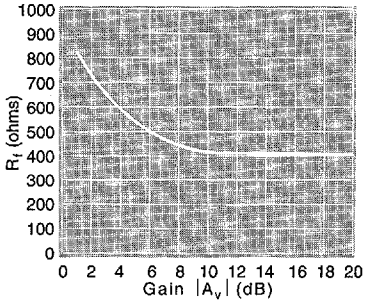


Figure 3: recommend R_f vs. Gain

Enable/Disable Operation

The CLC430 has a disable feature which allows several CLC430 outputs to be multiplexed on an analog output bus. When disabled, the CLC430 output and inverting input become a high impedance, and the amplifier quiescent power is reduced. The device is guaranteed to be disabled when the $\overline{DIS}$ line, pin 8, is grounded. An internal 10kΩ pull-up resistor ensures the amplifier is enabled when pin 8 is left floating or connected to the positive supply. Current, not voltage, determines the enabled state of the CLC430. Logic swings of 0V to + V_{CC} are required by the CLC430 disable pin. Open-collector TTL, or CMOS supplied from the same positive supply will effectively drive the disable feature of the CLC430.

Break-before-make operation is desirable to prevent large transient currents between amplifier outputs connected to the same output bus. The turn-on vs. turn-off time of the CLC430 guarantees two amplifiers will not be enabled simultaneously when driven from the same decoder circuit. Refer to Figure 3A on the CLC410 datasheet for a typical multiplexing circuit.

Feedback Resistor

The loop gain and frequency response for a current feedback amplifier is determined predominantly by the, feedback resistor, R_f. The datasheet electrical characteristics and typical performance plots, unless stated otherwise, specify a 750Ω R_f, a gain of +2, and ±15V supplies. Frequency response at different gains and supply voltages can be optimized by using a different value for R_f. Generally, lowering R_f, will peak the frequency response and extend the bandwith, while increasing its value will roll off the response. For unity-gain voltage follower circuits a non-zero R_f must be used with current feedback amplifiers such as the CLC430.

Application note OA-13 gives a detailed explanation of choosing R_f. The equations in the application note are to be considered as a starting point for the selection of R_f,and do not include the effects of parasitic capacitance at the inverting input, output, nor across the feedback resistor. The value for the inverting input impedance (R_i in OA-13) for the CLC430 is 60Ω when supplied from ±15V, a little higher at lower supply voltages. the following plot entitled "Recommended R_f, vs. Gain" is to be used to choose a value of R_f which will optimize the frequency response of the CLC430 over its entire recommended gain range. For ±5V operation a 675Ω feedback resistor at a gain of ±2 gives best response.

Differential Gain and Phase

The differential gain and phase of the CLC430 driving one video load (R_L=150Ω) is specified and guaranteed on the Electrical Characteristics table. A Typical Performance plot shows differential gain and phase with the part driving from one to four video loads. The technique used for measuring differential gain and phase is described in detail in application note OA-08.

Printed Circuit Layout

As with any high-speed amplifier, careful attention to circuit board layout is necessary for best performance. Of particular importance is the control of parasitic capacitance at the output and inverting input pins. Protoboards, sockets, and wirewrap construction must not be used due to the excessive parasitic capacitance and inductance resulting from such circuit construction techniques. A good low-impedance ground plane, and high-frequency power supply bypassing immediately adjacent to the device pins are critical to realizing full performance. The key to successful circuit operation is to be aware of frequencies at which the amplifier has power gain, not simply the frequency of the input signal. A discussion circuit design and construction guidelines applicable to the CLC430 can be found in application note OA-1 5.

Evaluation Board

Evaluation boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC430 are available. This board can be used for fast, trouble-free evaluation and characterization of the CLC430, and as a template for engineers designing their own printed circuit boards. Applications schematics for this board can be found in the product accessories section of the Comlinear databook.