HARRIS SEMICONDUCTOR

HS-65C162RRH

Radiation Hardened 2048 x 8-Bit Asynchronous CMOS Static RAM

December 1992

Features

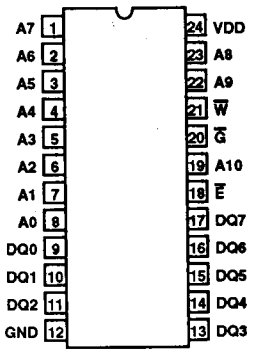
- Radiation Hardened EPI-CMOS
- Total Dose 2 x 10^5 RAD(Si)
- Transient Upset > 1 x 10^9 RAD(Si)/s
- Latch-Up Free > 1 x 10^{12} RAD(Si)/s
- Single Event Upset Hardened Option
- Low Standby Current 200μA Max
- Fast Access Time 160ns Max
- 2048 x 8-Bit
- Single +5V Power Supply
- Asynchronous Operation
- CMOS Compatible Inputs
- Completely Static Operation
- Three-State Output
- Military Temperature Range -55°C to +125°C Operation
- Functionally Equivalent to Harris HM-65162

Description

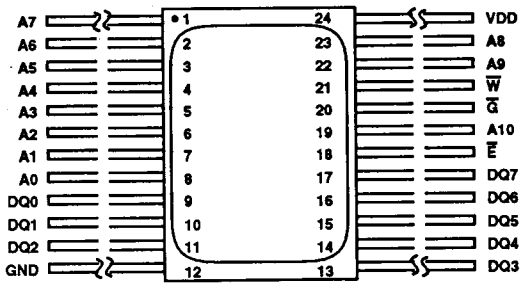
The HS-65C162RRH is designed to be functionally compatible with the Harris HM-65162. This device is a asynchronous 2048 x 8-bit static CMOS RAM fabricated using the Harris radiation hardened, self-aligned junction isolated silicon gate technology. The HS-65C162RRH is designed to have a maximum access time of 160ns after exposure to 2 x 10^5 Rads(Si) over the full military temperature range. Latch-up free operation is achieved by the use of epitaxial starting material. In addition, the device is single event upset hardened. Operation is designed for +5V.

Pinouts

24 PIN SIDEBRAZED DIP
CASE OUTLINE D3, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
CASE OUTLINE F6A, CONFIGURATION 2
TOP VIEW



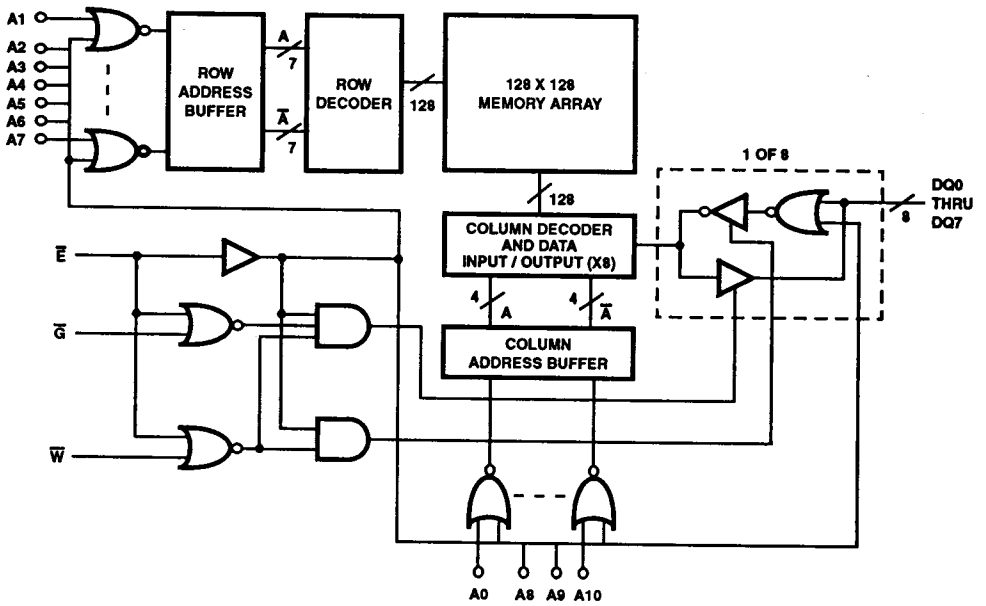
PIN	DESCRIPTION
A	Address Input
DQ	Data In/Data Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Connect
$\overline{W}$	Write Enable

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3030

Functional Diagram



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE
1	X	X	Disabled
0	1	1	Enabled
0	0	1	Read
0	X	0	Write

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	56°C/W	12°C/W
Braze Seal Flatpack Package	66°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.89W
Braze Seal Flatpack Package 0.76W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
SEU Immunity Operating Temperature Range ..... -20°C to +80°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
	VOH2	VDD = 4.5V, IO = -100mA	1, 2, 3	$-55°C \le T_A \le +125°C$	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, G = 5.5V, or E = 5.5V, VI/O = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, E = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, G = 5.5V, (Note 2), f = 1MHz, E = 0.8V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	mA
Enable Supply Current	ENIDD	VDD = 5.5V, IO = 0mA, E = 0.8V, VDD = VIH, VIL = 0V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

NOTE:

1. All voltages referenced to device GND.
2. Typical derating = 5mA/MHz increase in ICCOP.
3. Tested as follows: f = 1MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Access Time	TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	160	ns
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	120	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	160	ns
Write Enable Read Setup Time	TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Address Setup Time	TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Chip Selection to End of Write	TELWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	180	-	ns
Write Enable Pulse Setup Time	TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Chip Enable Data Setup Time	TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Address Valid to End of Write	TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	180	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns
Data Setup Time	TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns
Data Hold Time	TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	15	pF
			1, 3, 4	$T_A = +25°C$	-	12	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	12	pF
			1, 3, 4	$T_A = +25°C$	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	60	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable High to Output High Z	TEHQZ	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	40	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
Cycle Time	TAVAX	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	200	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device grounds.

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

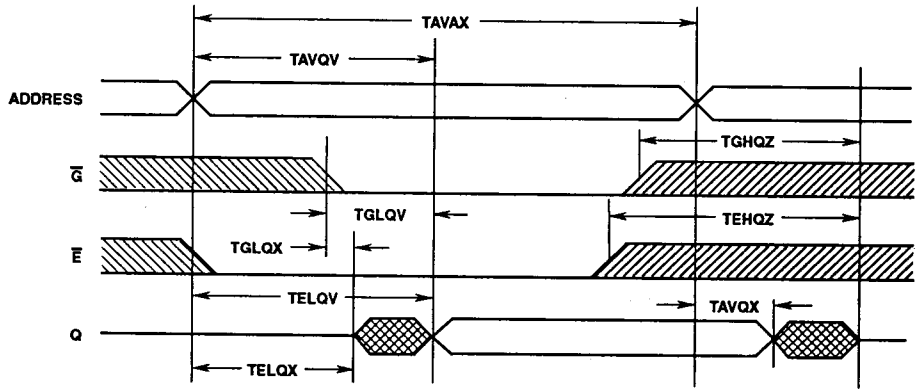
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 80mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Standby Supply Current	IDDSB1	±30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7, 9	N/A
Group C (Optional)		Samples/5005	N/A	1, 7, 9
Group D (Optional)		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

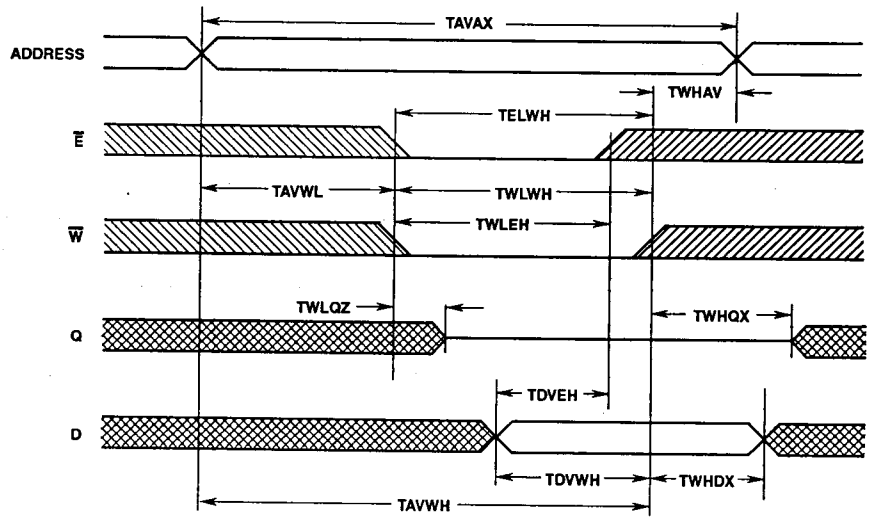
READ CYCLE



NOTE: $\overline{W}$ is high for a Read Cycle

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be ≤ VIL and W ≥ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

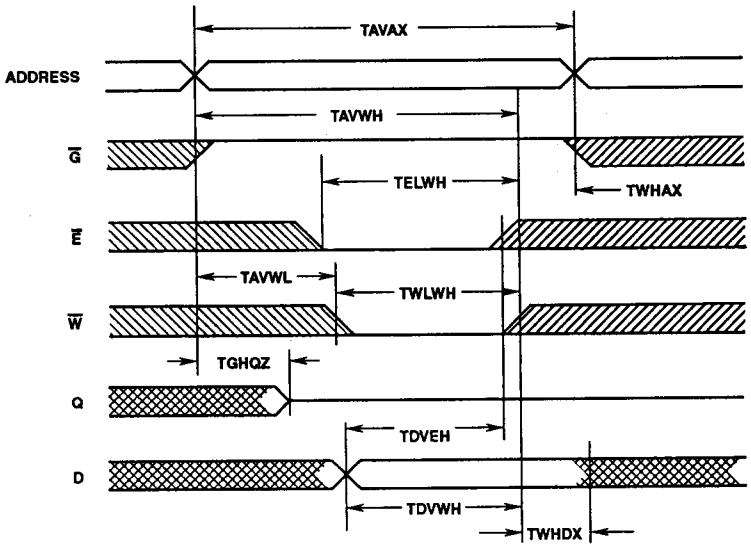
WRITE CYCLE I



NOTE: $\overline{W}$ is high for a Read Cycle

To write, addresses must be stable, E low and W falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of W. (TDVWH and TWHDX). While addresses are changing, W must be high. When W falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied. (Bus contention). If E transitions low simultaneously with the W line transitioning low or after the W transition, the output will remain in a high impedance state. G is held continuously low.

WRITE CYCLE II



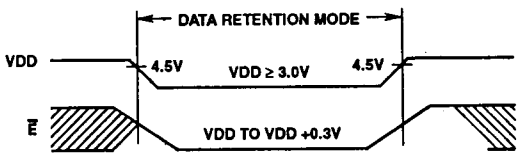
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

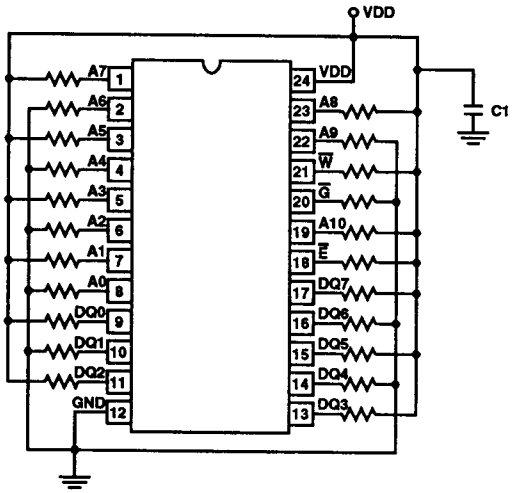
1. Chip Enable ($\overline{E}$) must be held high during data retention; within VDD to VDD +0.3V.
2. $\overline{E}$ must be kept between VDD +0.3V and 70% of VDD during the power up and power down transitions.

DATA RETENTION TIMING



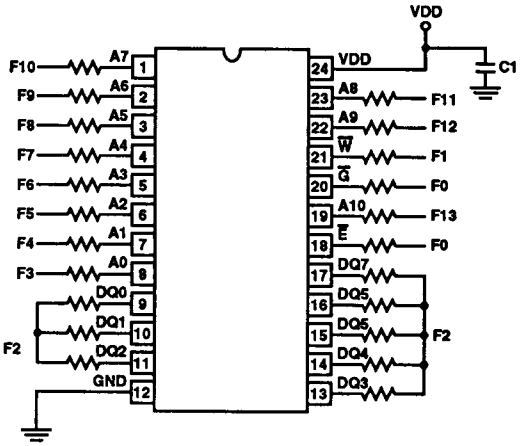
Burn-In Circuits

HS-65C162RRH (CERAMIC DIP)



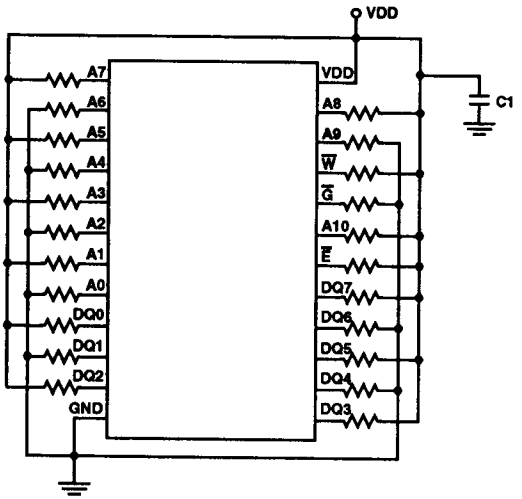
STATIC CONFIGURATION

HS-65C162RRH (CERAMIC DIP)



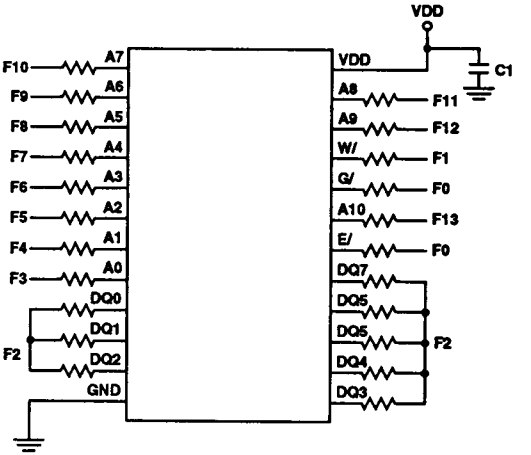
DYNAMIC CONFIGURATION

HS-65C162RRH (FLATPACK)



STATIC CONFIGURATION

HS-65C162RRH (FLATPACK)



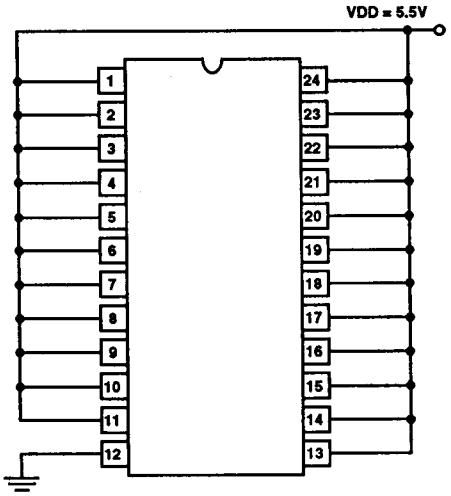
DYNAMIC CONFIGURATION

NOTE:
C1 = 0.01µF (min)

NOTES:
VCC = 6.0V ± 0.5V
VIH = 4.0V to VCC
VIL = 0.8V (max)
C1 = 0.01µF (min)
All Resistors = 27kΩ ± 10%
F0 = 100KHz ± 10%, 50% duty cycle
F1 = F0/2, F2 = F1/2, . . . F13 = F12/2

Irradiation Circuit

HS-65C162RRH (CERAMIC DIP)



NOTE:

1. Pin 12 to Ground
2. All other pins tied to VDD

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
198 x 270 x 19 ±1mils

METALLIZATION:
Type: Silicon-Aluminum
Thickness: 13kÅ ± 1.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Braze Seal DIP - 460°C (Max)
Braze Seal Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY:
1.4×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-65C162RRH