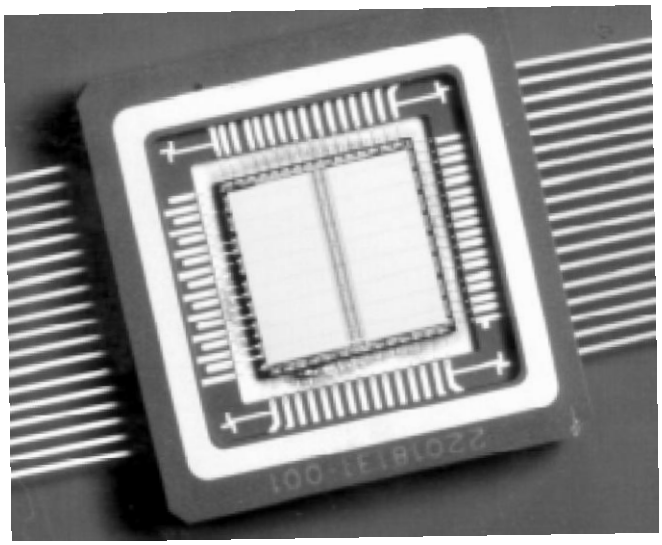
HX6356
32K x 8 STATIC RAM

The monolithic 32K x 8 Radiation Hardened Static RAM is a high performance 32,768 word x 8-bit static random access memory. It is fabricated with Honeywell's radiation hardened technology. It is QML qualified and is designed for use in systems operating in radiation environments with high dose rate upset needs. The SRAM operates over the full military temperature range and requires only a single 5V power supply. The SRAM is available with either TTL or CMOS compatible I/O. Power consumption is typically 800mW at 40MHz operation and less than 5mW when de-selected. SRAM operation is fully asynchronous, with a typical access time of 14ns. It is available in package and bare die forms.



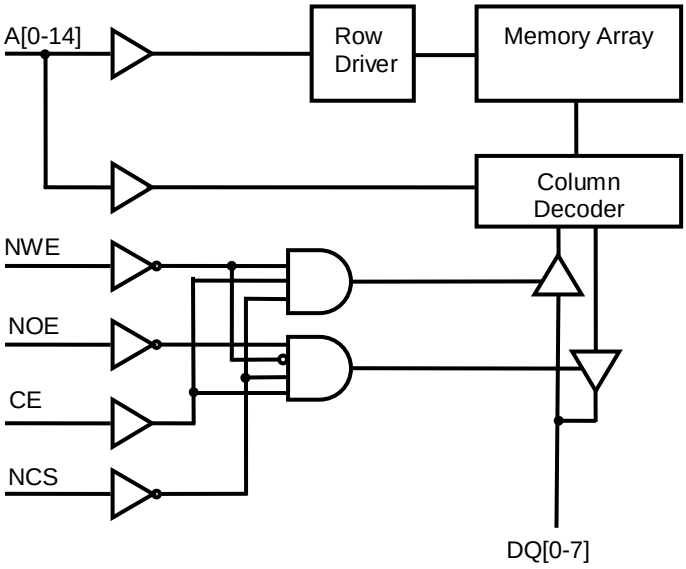
Honeywell's enhanced SOI RICMOS™ IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ IV process is a 5V, SOI CMOS technology with a 150 angstrom gate oxide and a minimum drawn feature size of 0.7um.

The memory cell is single event upset hardened, while multi-layer metal power busing and small collection volumes of SOI provides superior single event effect and dose rate hardening.

FEATURES

- Fabricated with RICMOS™ IV Silicon on Insulator (SOI)
- 0.75um Process (Leff = 0.6um)
- High Speed
  17ns Typical Write / Read Cycle
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Total Dose $1x10^{6}$ rad(Si)
- Soft Error Rate
  $1x10^{-10}$ upsets/bit-day
- Neutron Irradiation $1x10^{14}$ n/cm^2
- Dose Rate Upset
  $1x10^{11}$ rad(Si)/s
- Dose Rate Survivability
  $1x10^{12}$ rad(Si)/s
- Latchup Immune
- VDD Power Supply
  5V
- Operating Temperature Range
  -55°C to +125°C
- Package Options
  36-Lead CFP—Bottom Braze
  36-Lead CFP –Top Braze
- QML Qualified
  SMD 5962-95845

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



36 LEAD FLAT PACK PINOUT

HX6356
Top View

VSS	1	36	VSS
VDD	2	35	VDD
A14	3	34	NWE
A12	4	33	CE
A7	5	32	A13
A6	6	31	A8
A5	7	30	A9
A4	8	29	A11
A3	9	28	NOE
A2	10	27	A10
A1	11	26	NCS
A0	12	25	DQ7
DQ0	13	24	DQ6
DQ1	14	23	DQ5
DQ2	15	22	DQ4
NC*	16	21	DQ3
VDD	17	20	VDD
VSS	18	19	VSS

* NC pin must be connected to VSS.

PIN NAME DEFINITIONS

Pin Name	Timing Symbol	Definition
A[0-14]	A	Address input pins. Selects a particular 8-bit word within the memory array.
DQ[0-7]	D Q	Bi-directional data I/O pins. Data inputs (D) during a write operation. Data outputs (Q) during a read operation.
NCS	S	Negative chip select. Low allows normal read or write operation. High puts the SRAM into a deselected condition and holds the data output drivers in a high impedance (High-Z) state. If not used, it must be connected to VSS.
NWE	W	Negative write enable. Low activates a write operation and holds the data output drivers in a high impedance (High-Z) state. High allows normal read operation.
NOE	G	Negative output enable. High holds the data output drivers in a high impedance (High-Z) state. Low the data output driver state is defined by NCS, CE and NWE. If not used, it must be connected to VSS.
CE	E	Chip Enable. High allows normal read or write operation. Low puts the SRAM into a deselected condition and holds the data output drivers in a high impedance (High-Z) state. If not used, it must be connected to VDD.
VDD		Power input. Supplies power to the SRAM.
VSS		Ground

TRUTH TABLE

NCS	CE	NWE	NOE	Mode	DQ Mode
X	L	X	X	Deselected	High-Z
H	X	X	X	Deselected	High-Z
L	H	H	L	Read	Data Out
L	H	H	H	Read Standby	High-Z
L	H	L	X	Write	Data In

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Ratings		Unit
		Min	Max	
VDD	Positive Supply Voltage Referenced to VSS	-0.5	6.5	V
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.5	VDD + 0.5	V
IOUT	Average Output Current		25	mA
TSTORE	Storage Temperature	-65	150	°C
TSOLDER (2)	Soldering Temperature		270	°C
PD (3)	Package Power Dissipation		2.5	W
PJC	Package Thermal Resistance (Junction to Case)		2.0	°C/W
VHBM	Electrostatic Discharge Protection Voltage (Human Body Model)	2000		V
TJ	Junction Temperature		175	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Maximum soldering temperature can be maintained for no more than 5 seconds.
(3) IDDSB power + IDDOP power + Output driver power due to external loading must not exceed this specification.

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
VDD	Positive Supply Voltage Referenced to VSS	4.5	5.0	5.5	V
TC	Case Temperature	-55	25	125	°C
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.3		VDD + 0.3	V
TRAMP	VDD Power Supply Ramp Rate			50	ms

(1) Specifications listed in datasheet apply when operated under the Recommended Operating Conditions unless otherwise specified.

RADIATION HARDNESS RATINGS (1)

Symbol	Parameter	Environment Conditions	Limits (2)	Unit
TID	Total Ionizing Dose, R-Level		$1x10^5$	rad(Si)
	Total Ionizing Dose, F-Level		$3x10^5$	rad(Si)
	Total Ionizing Dose, H-Level		$1x10^6$	rad(Si)
DRU	Transient Dose Rate Upset	Pulse width ≤20ns	$1x10^{11}$	rad(Si)/s
DRS	Transient Dose Rate Survivability	Pulse width ≤20ns	$1x10^{12}$	rad(Si)/s
SER (2)	Projected Soft Error Rate	Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield	$1x10^{-10}$	upsets/bit-day
	Neutron Irradiation Damage	1 MeV equivalent energy	$1x10^{14}$	n/cm^2

(1) Device will not latchup when exposed to any of the specified radiation environments.
(2) Calculated using CREME96.

RADIATION CHARACTERISTICS

Total Ionizing Dose Radiation
The SRAM radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Single Event Soft Error Rate
Special process, memory cell, circuit and layout design considerations are included in the SRAM to minimize the impact of heavy ion and proton radiation and achieve small projected SER. These techniques sufficiently harden the SRAM such that cell redundancy and scrubbing are not required to achieve the projected SER.

Transient Dose Rate Ionizing Radiation
Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. This allows the SRAM to be capable of writing, reading, and retaining stored data during and after exposure to a transient dose rate ionizing radiation pulse, up to the DRU specification. The SRAM will also meet functional and timing specifications after exposure to a transient dose rate ionizing radiation pulse up to the DRS specification.

Neutron Irradiation Damage
SOI CMOS is inherently tolerant to damage from neutron irradiation. The SRAM meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup
The SRAM will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

PIN CAPACITANCE (1)

Symbol	Parameter	Max	Unit
CIN	Input Capacitance	7	pF
CDQ	Data I/O Capacitance	9	pF

(1) Maximum capacitance is verified as part of initial qualification only.

POWER PIN ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		Max	Unit
IDDSB	Static Supply Current	VIH = VDD, VIL = VSS, DQ = High-Z		1.5	mA
IDDOPW (1)(2)	Dynamic Supply Current Selected, Write	VIH = VDD, VIL = VSS, DQ = High-Z	1MHz	4	mA
			2MHz	8	mA
			10MHz	40	mA
			25MHz	100	mA
			40MHz	160	mA
IDDOPR (1)(2)	Dynamic Supply Current Selected, Read	VIH = VDD, VIL = VSS, DQ = High-Z	1MHz	4	mA
			2MHz	8	mA
			10MHz	40	mA
			25MHz	100	mA
			40MHz	160	mA
IDDOPD (1)(2)	Dynamic Supply Current Deselected	VIH = VDD, VIL = VSS, DQ = High-Z	40MHz	1.5	mA
IDR	Data Retention Supply Current	VDD = 2.5V		500	uA
		VDD = 3.0V		330	uA

(1) All inputs switching. DC average current.

(2) All dynamic operating mode current measurements (IDDOPx) exclude standby mode current (IDDSB). The total power is the sum of the power from the standby current (IDDSB), dynamic current (IDDOPx) and output driver current driving the output load.

SIGNAL PIN ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter		Conditions	Min	Max	Unit
IIN	Input Leakage Current		VSS ≤ VIN ≤ VDD	-5	5	uA
IOZ	Output Leakage Current		DQ = High-Z	-10	10	uA
VIL	Low-Level Input Voltage	CMOS			0.3 x VDD	V
		TTL			0.8	V
VIH	High-Level Input Voltage	CMOS		0.7 x VDD		V
		TTL		2.2		V
VOL	Low-Level Output Voltage	CMOS	IOL = 10mA		0.4	V
		TTL	IOL = 8mA		0.4	V
		CMOS / TTL	IOL = 200uA		0.05	V
VOH	High-Level Output Voltage	CMOS	IOH = -5mA	4.2		V
		TTL	IOH = -4mA	4.2		V
		CMOS / TTL	IOH = -200uA	VDD - 0.05		V

(1) Voltages referenced to VSS.

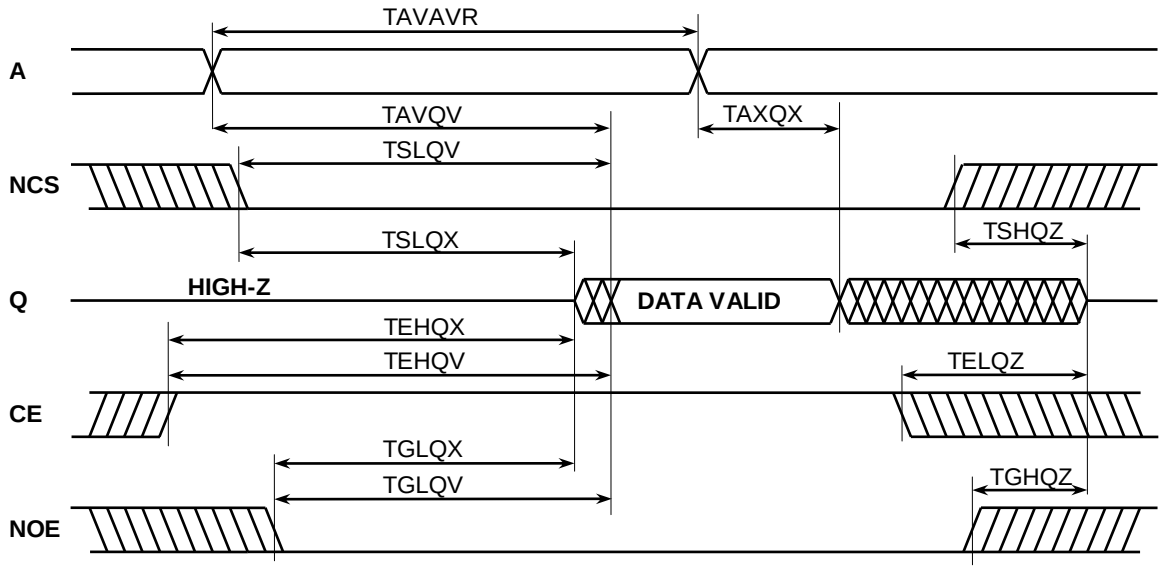
READ CYCLE TIMING CHARACTERISTICS (1)(2)

Symbol	Parameter	Limits		Unit
		Min	Max	
TAVAVR	Read Cycle Time	25		ns
TAVQV	Address Valid to Output Valid Access Time		25	ns
TAXQX	Address Change to Output Invalid Time	3		ns
TSLQV	Chip Select to Output Valid Access Time		25	ns
TSLQX	Chip Select to Output Low-Z Time	5		ns
TSHQZ	Chip Select to Output High-Z Time		10	ns
TEHQV	Chip Enable to Output Valid Access Time		25	ns
TEHQX	Chip Enable to Output Low-Z Time	5		ns
TELQZ	Chip Enable to Output High-Z Time		10	ns
TGLQV	Output Enable to Output Valid Access Time		9	ns
TGLQX	Output Enable to Output Low-Z Time	0		ns
TGHQZ	Output Enable to Output High-Z Time		9	ns

(1) The timing specifications are referenced to the Timing Input / Output References diagrams and the Timing Reference Load Circuit diagrams. IBIS models should be used to evaluate timing under application load and conditions.

(2) NWE = High

READ CYCLE TIMING WAVEFORMS



WRITE CYCLE TIMING CHARACTERISTICS (1)(2)(3)

Symbol	Parameter	Limits		Unit
		Min	Max	
TAVAVW	Write Cycle Time	25		ns
TWLWH	Start of Write to End of Write Pulse Width	20		ns
TSLWH	Chip Select to End of Write Time	20		ns
TEHWH	Chip Enable to End of Write Time	20		ns
TDVWH	Data Input Valid to End of Write Time	15		ns
TAVWH	Address Valid to End of Write Time	20		ns
TWHDX	Data Input Hold after End of Write Time	0		ns
TAVWL	Address Valid Setup to Start of Write Time	0		ns
TWHAX	Address Valid Hold after End of Write Time	0		ns
TWLQZ	Start of Write to Output High-Z Time		9	ns
TWHQX	End of Write to Output Low-Z Time	5		ns
TWHWL (4)	End of Write to Start of Write Pulse Width	5		ns

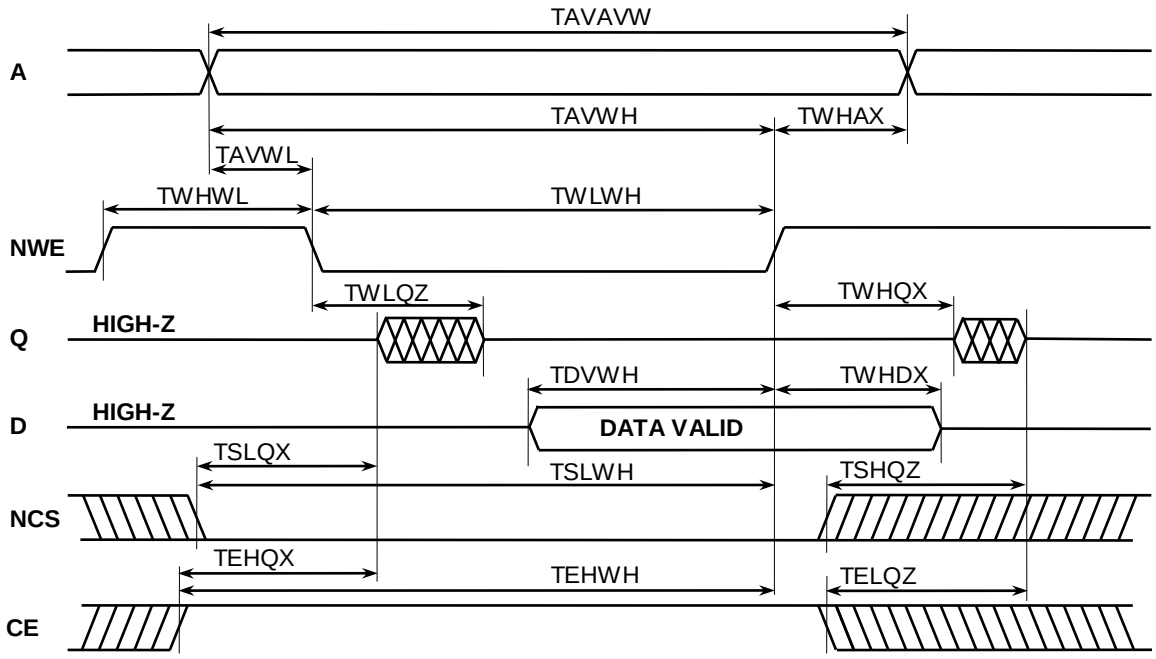
(1) The timing specifications are referenced to the Timing Input / Output References diagrams and the Timing Reference Load Circuit diagrams. IBIS models should be used to evaluate timing under application load and conditions.

(2) For an NWE controlled write, NCS must be Low and CE must be High when NWE is Low.

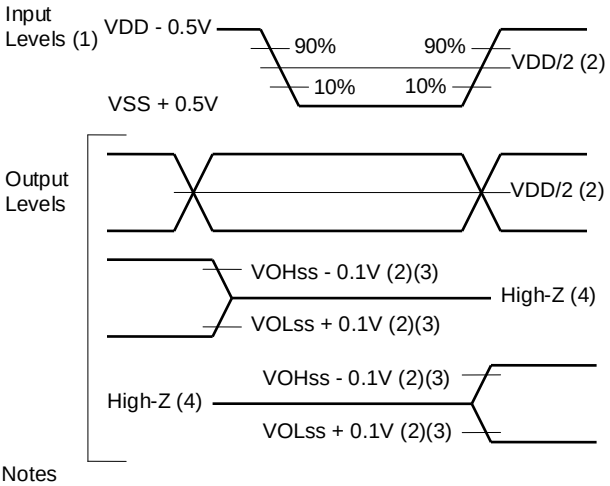
(3) Can use NOE = High to hold Q in a High-Z state when NWE = High, NCS = Low and CE = High.

(4) Guaranteed but not tested.

WRITE CYCLE TIMING WAVEFORMS

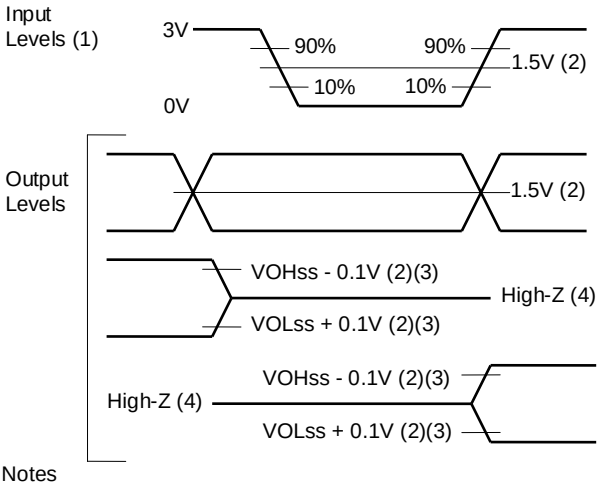


TIMING INPUT / OUTPUT REFERENCES (CMOS)



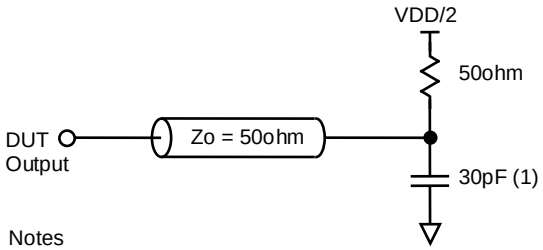
Notes
(1) Input rise and fall times = 1ns between 90% and 10% levels.
(2) Timing parameter reference voltage level.
(3) ss: Low-Z VOH and VOL steady-state output voltage.
(4) High-Z output pin pulled to VDD/2 by Reference Load Circuit.

TIMING INPUT / OUTPUT REFERENCES (TTL)



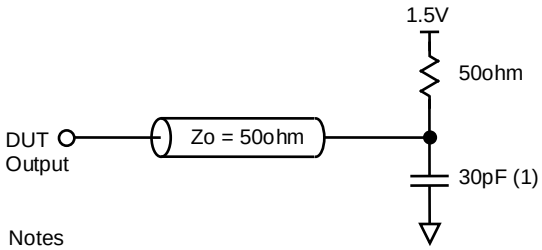
Notes
(1) Input rise and fall times = 1ns between 90% and 10% levels.
(2) Timing parameter reference voltage level.
(3) ss: Low-Z VOH and VOL steady-state output voltage.
(4) High-Z output pin pulled to 1.5V by Reference Load Circuit.

TIMING REFERENCE LOAD CIRCUIT (CMOS)



Notes
(1) Set to 5pF for T*QZ (Low-Z to High-Z) timing parameters.

TIMING REFERENCE LOAD CIRCUIT (TTL)



Notes
(1) Set to 5pF for T*QZ (Low-Z to High-Z) timing parameters.

FUNCTIONAL DESCRIPTION

SRAM Operation
SRAM operation is asynchronous. Operating modes are defined in the Truth Table. Read operations can be controlled by Address (A), Chip Enable (CE) or Chip Select (NCS). Write operations can be controlled by Write Enable (NWE), Chip Enable (CE) or Chip Select (NCS).

Read Operation
A read operation occurs when Chip Select (NCS) is low and Chip Enable (CE) and Write Enable (NWE) are high. The output drivers are controlled independently by the Output Enable (NOE) signal.

To control a read cycle with NCS/CE where TSLQV/TEHQV is the access time, all addresses must be valid TAVQV minus TSLQV/TEHQV prior to the enabling NCS/CE transition. Address transitions can occur later; however, the valid Data Output (Q) access time will then be defined by TAVQV instead of TSLQV/TEHQV. NCS/CE can disable the read at any time; however, Data Output drivers will enter a High-Z state TSHQZ/TELQZ later.

To control a read cycle with Address where TAVQV is the access time, NCS/CE must transition to active TSLQV/TEHQV minus TAVQV prior to the last Address transition. The NCS/CE active transition can occur later; however, the valid Data Output (Q) access time will then be defined by TSLQV/TEHQV instead of TAVQV. To perform consecutive read cycles, NCS/CE is held continuously low/high, and

the toggling of any Address will start a new read cycle. Any amount of toggling or skew between Address transitions is permissible; however, Data Output will not become valid until TAVQV following the last occurring Address transition. The minimum Address activated read cycle time is TAVAVR which is the time between the last Address transition of the previous cycle and the first Address transition of the next cycle. The valid Data Output from a previous cycle will remain valid until TAXQX following the first Address transition of the next cycle.

Write Operation

A write operation occurs when Write Enable (NWE) and Chip Select (NCS) are low and Chip Enable (CE) is high. The write mode can be controlled via three different control signals: NWE, NCS or CE can start the write mode and end the write mode, but the write operation itself is defined by the overlap of NWE low, NCS low and CE high. All three modes of control are similar, except the NCS and CE controlled modes deselect the SRAM when NCS is high or CE is low between writes.

To write Data (D) into the SRAM, NWE and NCS must be held low and CE must be held high for at least TWLWH, TSLSH and TEHEL respectively. Any amount of skew between these signal transitions can be tolerated, and any one of these control signals can start or end the write operation as long as there is sufficient overlap in these signals to ensure a valid write time (e.g., TSLWH, TWLSH, TEHWH and TWLEL).

Address inputs must be valid at least TAVWL/TAVSL/TAVEH before the start of write and TAVWH/TAVSH/TAVEL before the end of write and must remain valid during the write operation. Hold times for address inputs with respect to the end of write must be a minimum of TWHAX/TSHAX/TELAX.

A Data Input (D) valid to the end of write time of TDVWH/TDVSH/TDVEL must be provided during the write operation. Hold times for Data Input with respect to the end of write must be at least TWHDX/TSHDX/TELDX. To avoid Data Input driver contention with the SRAM output driver, the Data Input (D) must not be applied until TWLQZ/TGHQZ/TSHQZ/TELQZ after the output drive (Q) is put into a High-Z condition by NWE/NOE/NCS/CE.

Consecutive write cycles are performed by toggling at least one of the start of write control signals for TWHWL/TSHSL/TELEH. If only one of these signals is used, the other two must be in their write enable states. The minimum write cycle time is TAVAVW/TAVAVS/TAVAVE.

Signal Integrity

As a general design practice, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns. This is especially important in a selected and enabled state. When the device is selected and enabled, the last transitioning input for the desired operation must have good signal integrity to maintain valid operation. The transitioning inputs that bring the device into and out of a selected and enabled state must also have good signal integrity to maintain valid operation. When the device is deselected and/or disabled, inputs can have poor signal integrity and even float as long as the inputs that are defining the deselected and/or disabled state stay within valid VIL and VIH voltage levels. However, floating inputs for an extended period of time is not recommended.

RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

SCREENING AND CONFORMANCE INSPECTION

The product test flow includes screening units with the applicable flow (Engineering Model, Class V or equivalent, Class Q or equivalent) and the appropriate periodic or lot Conformance Testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) / Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

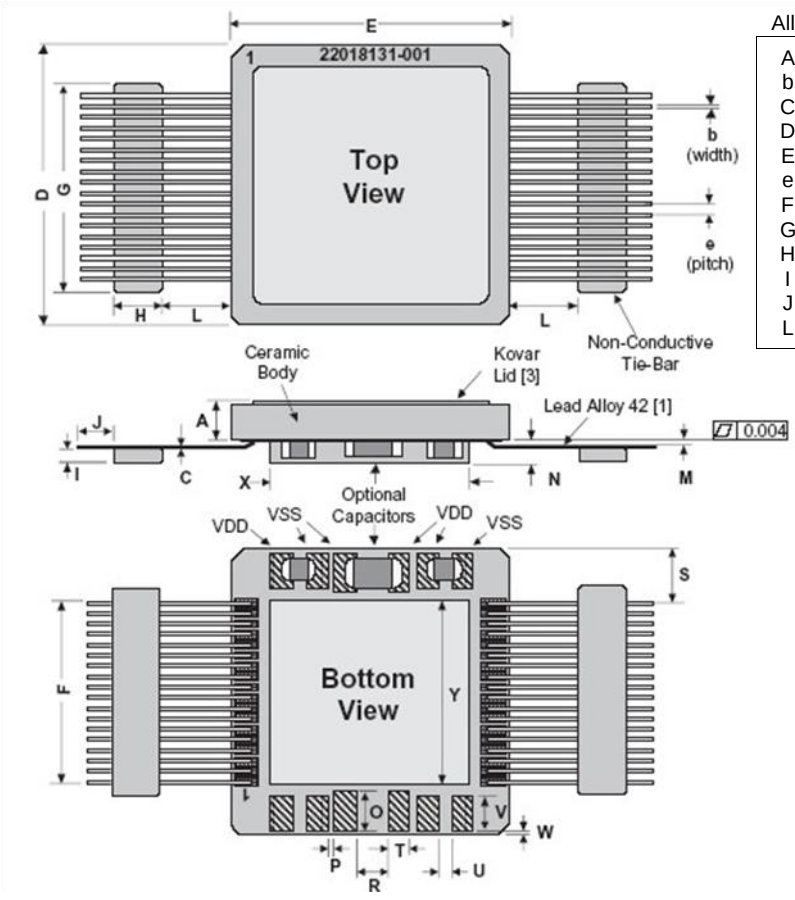
PACKAGE FEATURES

Feature	Description	Description
Designation	X	P
Type	36-lead CFP (bottom braze)	36-lead CFP (top braze)
Body Construct	multi-layer ceramic (Al_2O_3)	multi-layer ceramic (Al_2O_3)
VDD, VSS Planes	Yes	Yes
Lid Construct	Kovar	Kovar
Lid Electrical Connection	VSS	VSS
VDD to VSS Chip Capacitors (Caps) (1)	User Option	NA

(1) Default configuration is without package capacitors.
Contact Honeywell for part ordering information if capacitors are desired.

PACKAGE DIAGRAMS

36-Lead Flat Pack - Bottom Braze, Designation = X

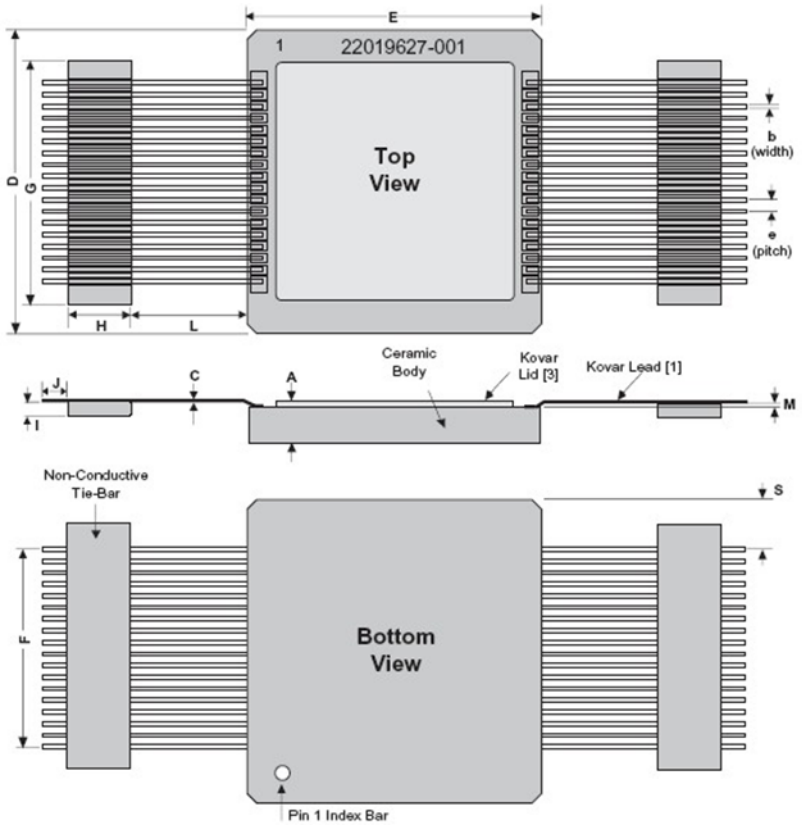


All dimensions in inches

A	0.095 ± 0.014	M	0.008 ± 0.003
b	0.008 ± 0.002	N	0.050 ± 0.010
C	0.005 to 0.0075	O	0.090 ref
D	0.650 ± 0.010	P	0.015 ref
E	0.630 ± 0.007	R	0.075 ref
e	0.025 ± 0.002 [2]	S	0.113 ± 0.010
F	0.425 ± 0.005 [2]	T	0.050 ref
G	0.525 ± 0.005	U	0.030 ref
H	0.135 ± 0.005	V	0.080 ref
I	0.030 ± 0.005	W	0.005 ref
J	0.080 typ.	X	0.450 ref
L	0.285 ± 0.015	Y	0.400 ref

[1] Parts delivered with leads unformed
[2] At tie bar
[3] Lid tied to VSS

36-Lead Flat Pack - Top Braze, Designation = P



All dimensions in inches

A	0.085 ± 0.010
b	0.008 ± 0.002
C	0.005 to 0.0075
D	0.650 ± 0.010
E	0.630 ± 0.007
e	0.025 ± 0.002 [2]
F	0.425 ± 0.005 [2]
G	0.525 ± 0.005
H	0.135 ± 0.005
I	0.030 ± 0.005
J	0.080 typ.
L	0.285 ± 0.015
M	0.009 ± 0.003
S	0.113 ± 0.010

[1] Parts delivered with leads unformed
[2] At tie bar
[3] Lid tied to VSS

ORDERING INFORMATION (1)

Standard Microcircuit Drawing (SMD)

The QML qualified HX6356 SRAM can be ordered under the SMD drawing 5962-95845.

Order Code

H	X	6356	X	V	H	C

SOURCE
H = Honeywell

PROCESS
X = SOI

PART NUMBER
6356 = 32k x 8 SRAM

PACKAGE DESIGNATION
X = 36 Lead CFP (bottom braze) (2) (5)
P = 36 Lead CFP (top braze)
K = Known Good Die (4)
- = Bare Die (no package) (4)

SCREEN LEVEL
V = QML Class V
Q = QML Class Q
S = Non-QML Class Level S
B = Non-QML Class Level B
E = Engineering Model (3)

TOTAL DOSE HARDNESS
R = $1x10^5$ rad(Si)
F = $3x10^5$ rad(Si)
H = $1x10^6$ rad(Si)
N = No Level Guaranteed (3)

INPUT BUFFER TYPE
C = CMOS
T = TTL

(1) Orders may be faxed to 763-954-2051.
Please contact our Customer Service Representative at 763-954-2474 or 1-800-323-8295 for further information.
(2) For CMOS I/O type only.
(3) Engineering Model Description: Screen Level and Total Dose Hardness codes must be “E” and “N” respectively.
Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.
(4) Information herein applies to packaged parts. Contact Honeywell for known good die and bare die information.
(5) Default configuration is without package capacitors. Contact Honeywell for ordering information if capacitors are desired.

FIND OUT MORE

For more information about Honeywell’s family of radiation hardened integrated circuit products and services, visit www.honeywellmicroelectronics.com.

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ADS-14272 Rev. B
August 2014