n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Choppers**
- **Amplifiers**

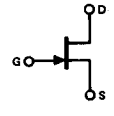
BENEFITS

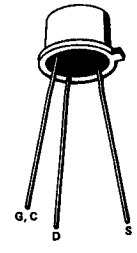
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (2N3970)
- Good Off-Isolation
  $I_{D(off)} < 250$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Note 1) . . . . . 1.8 W
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 7



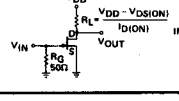


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	2N3970 Min	2N3970 Max	2N3971 Min	2N3971 Max	2N3972 Min	2N3972 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate Reverse Breakdown Voltage	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2	STATIC	I_{DGO} Drain Reverse Current		250		250		250	pA	$V_{DG} = 20$ V, $I_S = 0$	
3	STATIC	I_{DGO} Drain Reverse Current		500		500		500	nA	$V_{DG} = 20$ V, $I_S = 0$	150°C
4	STATIC	$I_{D(off)}$ Drain Cutoff Current		250		250		250	pA	$V_{DS} = 20$ V, $V_{GS} = -12$ V	
5	STATIC	$I_{D(off)}$ Drain Cutoff Current		500		500		500	nA	$V_{DS} = 20$ V, $V_{GS} = -12$ V	150°C
6	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
7	STATIC	I_{DSS} Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
8	STATIC	$V_{DS(on)}$ Drain-Source ON Voltage						2	V	$V_{GS} = 0$, $I_D = 5$ mA	
9	STATIC	$V_{DS(on)}$ Drain-Source ON Voltage				1.5			V	$V_{GS} = 0$, $I_D = 10$ mA	
10	STATIC	$V_{DS(on)}$ Drain-Source ON Voltage		1					V	$V_{GS} = 0$, $I_D = 20$ mA	
11	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13	DYN	C_{iss} Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
14	DYN	C_{rss} Common-Source Reverse Transfer Capacitance		6		6		6	pF	$V_{DS} = 0$, $V_{GS} = -12$ V	f = 1 MHz
15	SW	$t_{d(on)}$ Turn-On Delay Time		10		15		40	ns	$V_{DD} = 10$ V, $V_{GS(on)} = 0$	
16	SW	t_r Rise Time		10		15		40	ns	2N3970: $I_{D(on)}$ 20 mA, R_L 450 Ω, $V_{GS(off)}$ −10 V	
17	SW	t_{off} Turn-Off Time		30		60		100	ns	2N3971: 10 mA, 850 Ω, −5 V; 2N3972: 5 mA, 1.6KΩ, −3 V	

*JEDEC registered data.

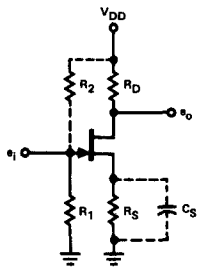
NOTE:
1. Derate linearly at the rate of 10 mW/°C.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

NC
SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

APPLICATIONS



Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

V_{DD} (V)	R_S (Ω)	R_1 (MΩ)	R_2 (MΩ)	C_S (μF)	I_{DD} (mA)	R_D (Ω)	e_o Max (V)	A_V
2N3970								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
V_{DD} = 15 V_{SS} = -15	3K	1	Source Follower		7	0	8.5	0.96
	7.5K	1			6	0	8.5	0.96
V_{DD} = 15 V_{SS} = -15	7.5K	1	Source Follower		6	0	15	0.97
2N3971								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97
2N3972								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-55
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		2.5	0	13	0.98
	7.5K	1			1.5	0	13	0.98