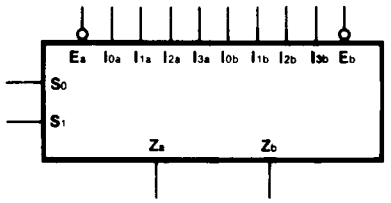
HD74AC153/HD74ACT153 ● Dual 4-Input Multiplexer

Description

The HD74AC153/HD74ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the HD74AC153/HD74ACT153 can act as a function generator and generate any two functions of three variables.

- Outputs Source/Sink 24 mA
- HD74ACT153 has TTL-Compatible Inputs

Logic Symbol



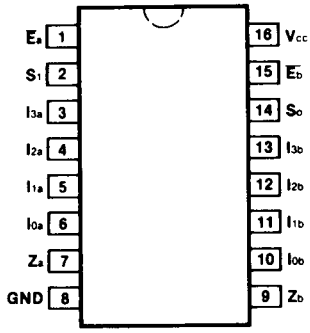
Functional Description

The HD74AC153/HD74ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are High, the corresponding outputs (Z_a, Z_b) are forced Low. The HD74AC153/HD74ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

Pin Assignment



(Top View)

Pin Names

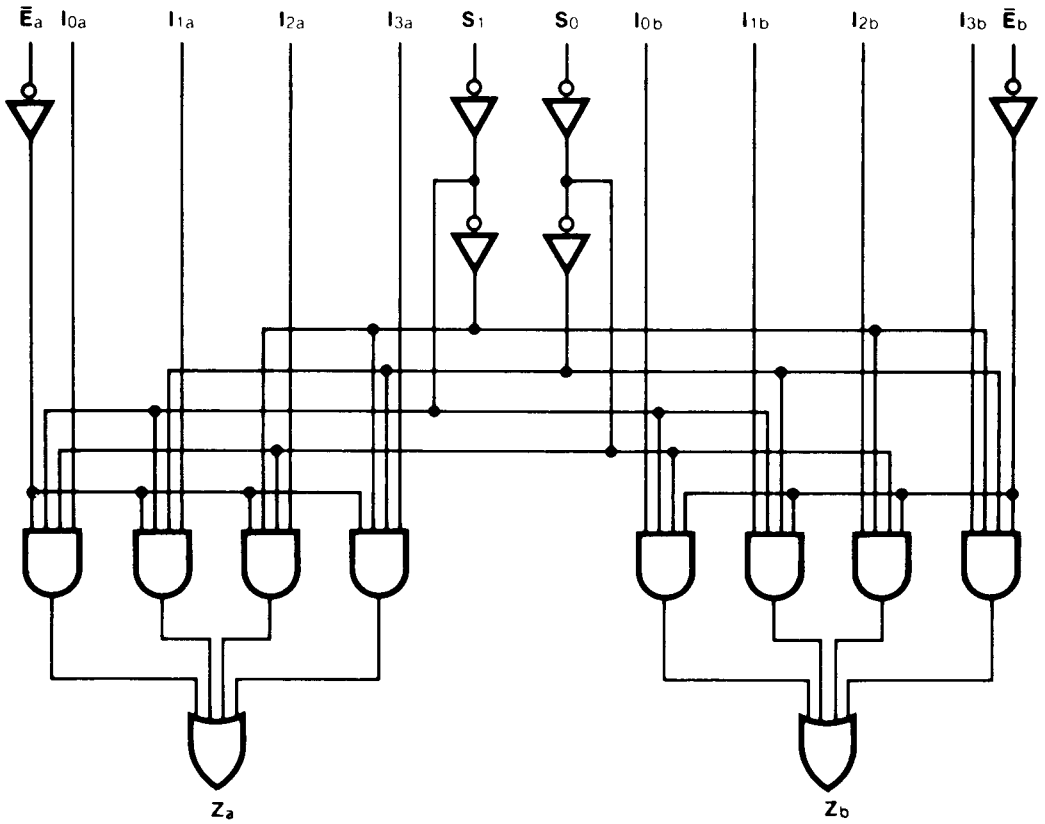
I_{0a} • I_{3a}	Side A Data Inputs
I_{0b} • I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{E}_a$	Side A Enable Input
$\overline{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input (HD74ACT153)	1.5	mA	V_{IN} = V_{CC} − 2.1V, V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC153

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Sn to Zn	3.3	1.0	9.5	15.0	1.0	17.5	ns
		5.0	1.0	6.5	11.0	1.0	12.5	
t_{PHL}	Propagation Delay Sn to Zn	3.3	1.0	8.5	14.5	1.0	16.5	ns
		5.0	1.0	6.5	11.0	1.0	12.0	
t_{PLH}	Propagation Delay $\overline{En}$ to Zn	3.3	1.0	8.0	13.5	1.0	16.0	ns
		5.0	1.0	5.5	9.5	1.0	11.0	
t_{PHL}	Propagation Delay $\overline{En}$ to Zn	3.3	1.0	7.0	11.0	1.0	12.5	ns
		5.0	1.0	5.0	8.0	1.0	9.0	
t_{PLH}	Propagation Delay In to Zn	3.3	1.0	7.5	12.5	1.0	14.5	ns
		5.0	1.0	5.5	9.0	1.0	10.5	
t_{PHL}	Propagation Delay In to Zn	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.0	8.5	1.0	10.0	

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT153

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Sn to Zn	5.0	1.0	7.0	11.5	1.0	13.5	ns
t_{PHL}	Propagation Delay Sn to Zn	5.0	1.0	7.0	11.5	1.0	13.5	ns
t_{PLH}	Propagation Delay $\overline{En}$ to Zn	5.0	1.0	6.5	10.5	1.0	12.5	ns
t_{PHL}	Propagation Delay $\overline{En}$ to Zn	5.0	1.0	6.0	9.5	1.0	11.0	ns
t_{PLH}	Propagation Delay In to Zn	5.0	1.0	5.5	9.5	1.0	11.0	ns
t_{PHL}	Propagation Delay In to Zn	5.0	1.0	5.5	9.5	1.0	11.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	65.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

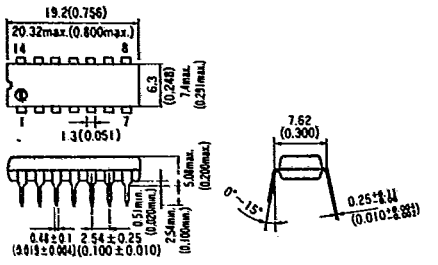
• Package code of Advanced CMOS Logic

HD74AC XXXX P

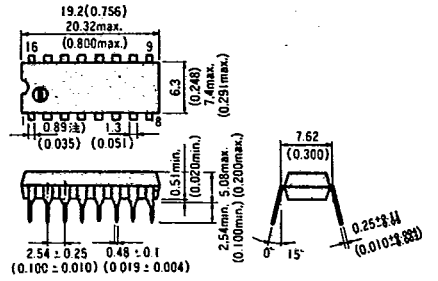
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

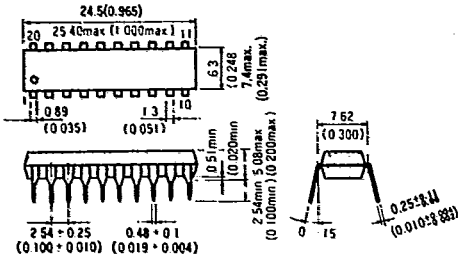
14 Pin type



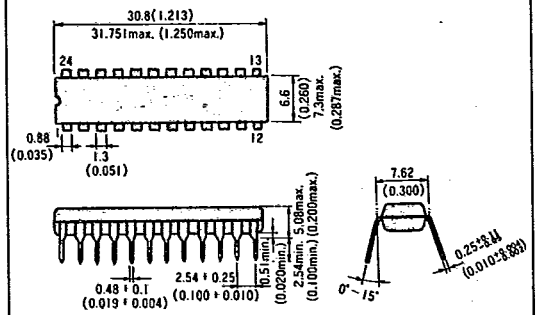
16 Pin type



20 Pin type



24 Pin type



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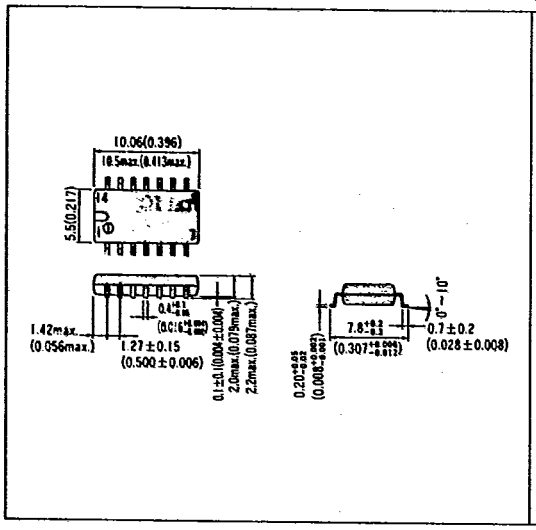
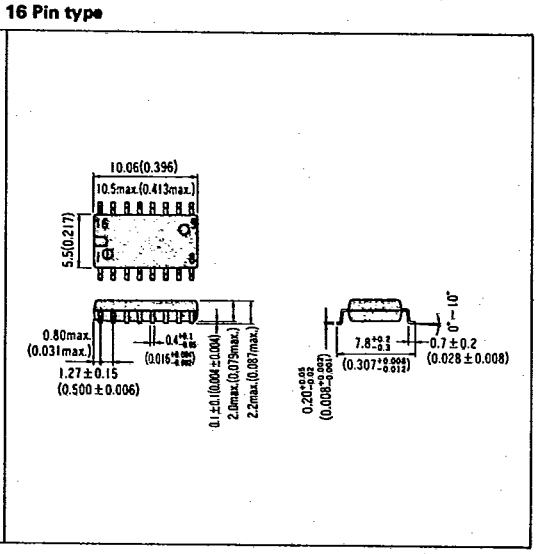
Package Information

Small Outline Package [Unit: mm (inch)]

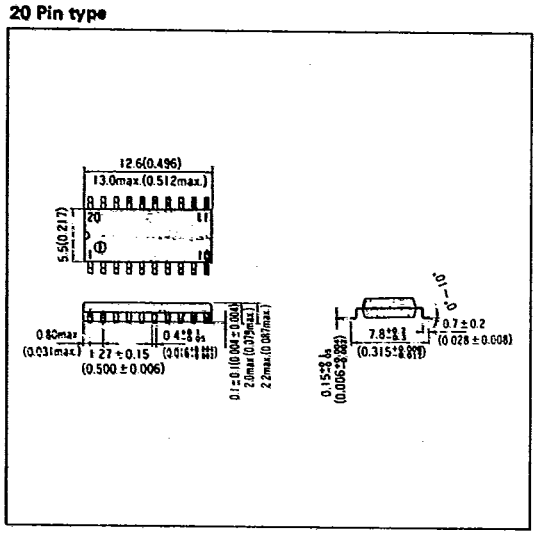
14 Pin type



16 Pin type



20 Pin type



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