V53C318160A
3.3 VOLT 1M X 16 FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE	50	60	70
Max. $\overline{RAS}$ Access Time, (t_{RAC})	50 ns	60 ns	70 ns
Max. Column Address Access Time, (t_{CAA})	25 ns	30 ns	35 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	35 ns	40 ns	45 ns
Min. Read/Write Cycle Time, (t_{RC})	90 ns	104 ns	124 ns

Features

- 1M x 16-bit organization
- Fast Page Mode for a sustained data rate of 29 MHz
- $\overline{RAS}$ access time: 50, 60, 70 ns
- Dual $\overline{CAS}$ Inputs
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh, and Self Refresh.
- Refresh Interval: 1024 cycles/16 ms
  1024 cycles/256 ms (L-version)
- Available in 42-pin 400 mil SOJ and 50/44-pin 400 mil TSOP-II
- Single +3.3 V ±0.3 V Power Supply
- LVTTL Interface

Description

The V53C318160A is a 1048576 x 16 bit high-performance CMOS dynamic random access memory. The V53C318160A offers Fast Page mode operation. The V53C318160A has an symmetric address, 10-bit row and 10-bit column.

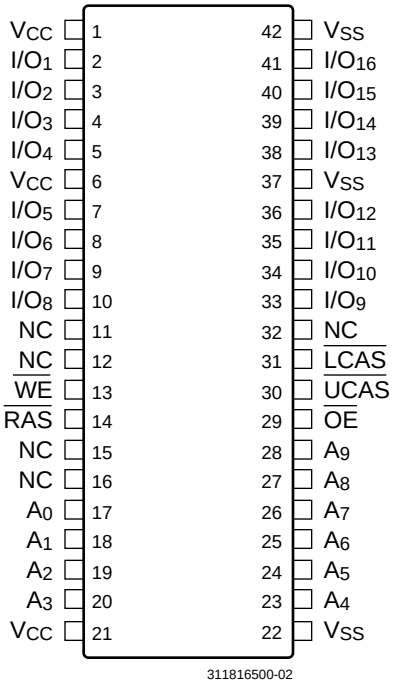
All inputs are LVTTL compatible. Fast Page Mode operation allows random access up to 1024 x 16 bits, within a page, with cycle times as short as 35 ns.

These features make the V53C318160A ideally suited for a wide variety of high performance computer systems and peripheral applications.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	K	T	50	60	70	Std.	L	
0°C to 70°C	•	•	•	•	•	•	•	Blank

42-Pin Plastic SOJ PIN CONFIGURATION Top View



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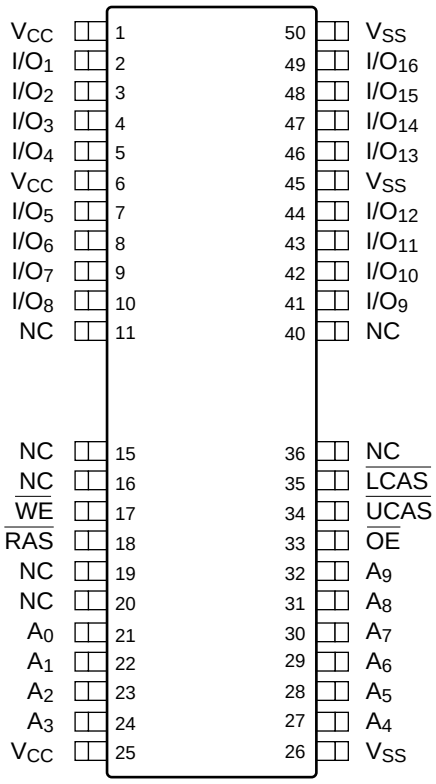
50/44-Pin Plastic TSOP-II PIN CONFIGURATION Top View



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Pin Names

A_0–A_9	Row, Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_{16}	Data Input, Output
V_{CC}	+3.3V Supply
V_{SS}	0V Supply
NC	No Connect

Description	Pkg.	Pin Count
SOJ	K	42
TSOP-II	T	50

Absolute Maximum Ratings*

Operating temperature range .....0 to 70 °C
Storage temperature range ..... -55 to 150 °C
Soldering temperature .....260 °C
Soldering time.....10 s
Input/output voltage .... -0.5 to min (V_{CC}+0.5, 4.6) V
Power supply voltage .....-0.5V to 4.6 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

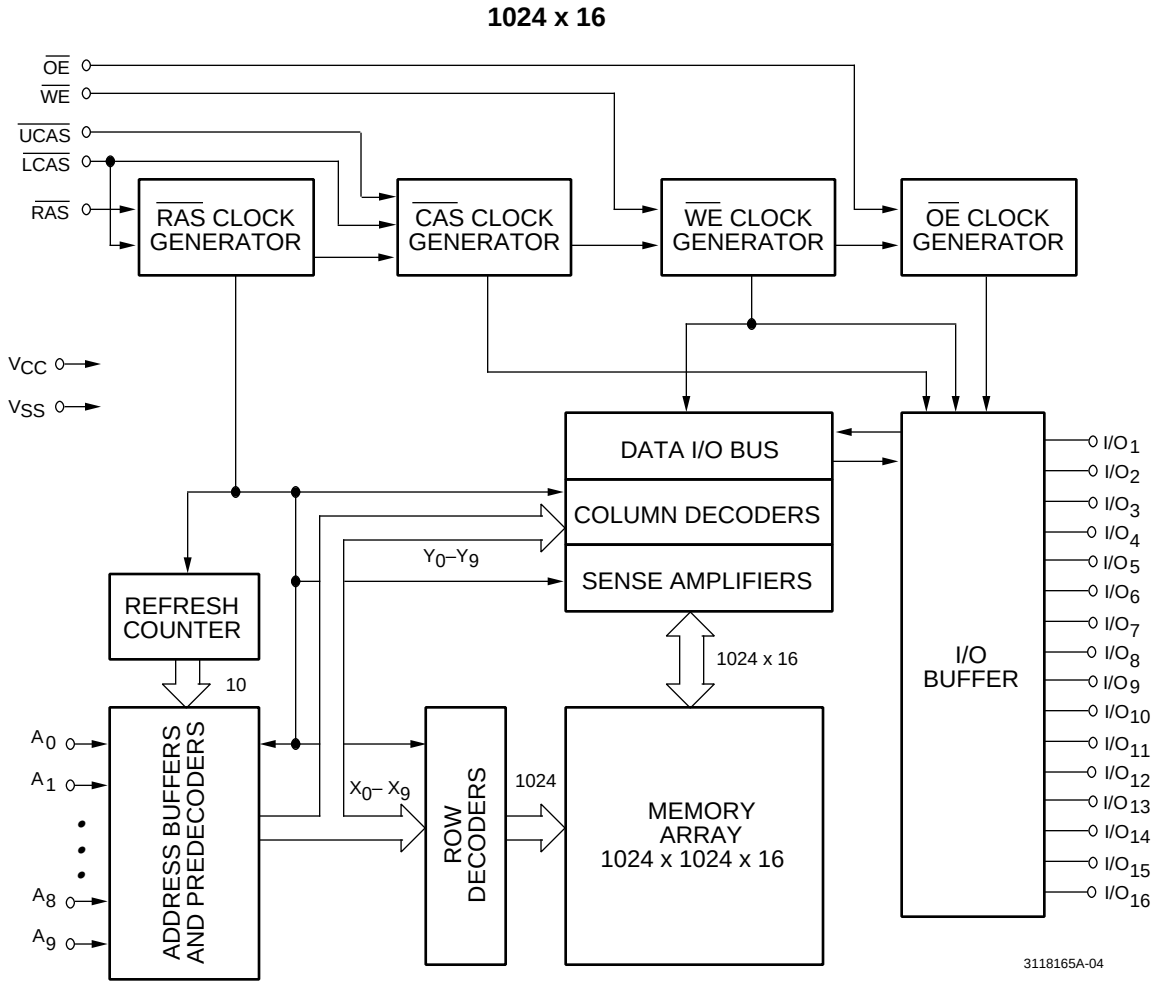
Capacitance*

T_A = 25°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, f = 1 MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Address Input	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

***Note:** Capacitance is sampled and not 100% tested.

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, t_T = 2ns, unless otherwise specified.

Symbol	Parameter	Access Time	V53C318160A			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10	µA	$V_{SS} \le V_{IN} \le V_{CC}$ + 0.3V	1
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$ + 0.3V $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	1
I_{CC1}	V_{CC} Supply Current, Operating	50			200	mA	$t_{RC} = t_{RC}$ (min.)	2, 3, 4
		60			180			
		70			160			
I_{CC2}	V_{CC} Supply Current, TTL Standby				2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	50			200	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		60			180			
		70			160			
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	50			55	mA	Minimum Cycle	2, 3, 4
		60			50			
		70			45			
I_{CC5}	V_{CC} Supply Current, CMOS Standby				1.0	mA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V	1
I_{CC6}	Average Self Refresh Current CBR cycle with $t_{RAS} > t_{RASS}$ min., $\overline{CAS}$ held low, $\overline{WE} = V_{CC} - 0.2$V, Address and $D_{IN} = V_{CC} - 0.2$V or 0.2V				1.0 250	mA µA	L version	
I_{CC7}	V_{CC} Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh	50			200	mA	$t_{RC} = t_{RC}$ (min)	2, 4
		60			180			
		70			160			
V_{IL}	Input Low Voltage		–0.5		0.8	V		1
V_{IH}	Input High Voltage		2		V_{CC}+0.5	V		1
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2 mA	1
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –2 mA	1

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0V, t_T = 2ns unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	50		60		70		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	90		110		130		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	30		40		50		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	50		60		70		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	13	10K	15	10K	20	10K	ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	37	20	45	20	50	ns	
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8		10		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		15		15		ns	
12	$t_{CL1RH1(R)}$	t_{RSH}	$\overline{RAS}$ Hold Time	13		15		20		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	9
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	9
16	t_{CL1}	t_{COH}	Output Hold after $\overline{CAS}$ LOW	5		5		5		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		13		15		20	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		13		15		20	ns	7, 12
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		50		60		70	ns	7, 12
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		25		30		35	ns	7, 13
21	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	7
22	t_{CH2QX}	t_{OFF}	Output Buffer Turnoff Delay	0	13	0	15	0	20	ns	
23	t_{CL1QZ}	t_{DZC}	Data to $\overline{CAS}$ Low Delay	0		0		0		ns	15
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	25	15	30	15	35	ns	
25	t_{GL2QZ}	t_{OEZ}	Output Buffer Turnoff Delay from $\overline{OE}$	0	13	0	15	0	17	ns	8
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	13		15		20		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	11
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	8		10		10		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	8		10		10		ns	
30	t_{GL1QZ}	t_{DEO}	Data to $\overline{OE}$ Delay	0		0		0		ns	15
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13		15		17		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	10

AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	50		60		70		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
33	t_{WL1DX}	t_{DH}	Data in Hold Time	10		10		15		ns	10
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	10		13		15		ns	10
35	t_{CH2RH2}	t_{PRWC}	EDO Page Mode Read-Write Cycle Time	58		68		77		ns	
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	71		80		95		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	31		35		45		ns	10
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	68		80		95		ns	10
40	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	43		50		60		ns	10
41	t_{CL2CL2}	t_{PC}	EDO Page Mode Read or Write Cycle Time	35		40		45		ns	
42	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
43	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	25		30		35		ns	
44	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		27		32		37	ns	6
46	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
47	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		5		ns	
48	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
50	t_{RH2CL2}	t_{RASP}	$\overline{RAS}$ Pulse Width	50	200K	60	200K	70	200K	ns	
51	t_{RH2CL2}	t_{RHCP}	$\overline{CAS}$ Precharge Time to $\overline{RAS}$ Delay	30		35		40		ns	
52	t_{RH2CL2}	t_{CPWD}	$\overline{CAS}$ Precharge Time to $\overline{WE}$	48		55		65		ns	
53	t_{RH2CL2}	t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test)	35		40		40		ns	
54	t_{RH2CL2}	t_{WRP}	Write to $\overline{RAS}$ Precharge time (CRB Cycle)	10		10		10		ns	
55	t_{RH2CL2}	t_{WRH}	Write Hold time reference to $\overline{RAS}$ (CRB Cycle)	10		10		10		ns	
56	t_{RH2CL2}	t_{CDD}	$\overline{CAS}$ High to Data delay	13		15		20		ns	16
57	t_{RH2CL2}	t_{ODD}	$\overline{OE}$ High to Data delay	13		15		20		ns	16
58	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
59		t_{REF}	Refresh Interval (1024 Cycles)		16		16		16	ms	
		t_{REF}	Refresh Interval (1024 Cycles) (L-version)		256		256		256	ms	

Self Refresh AC Characteristics

60		t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh	100K		100K		100K		ns	17
61		t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh	95		110		130		ns	17
62		t_{CHS}	$\overline{CAS}$ Hold Time Width During Self Rerfresh	50		50		50		ns	17

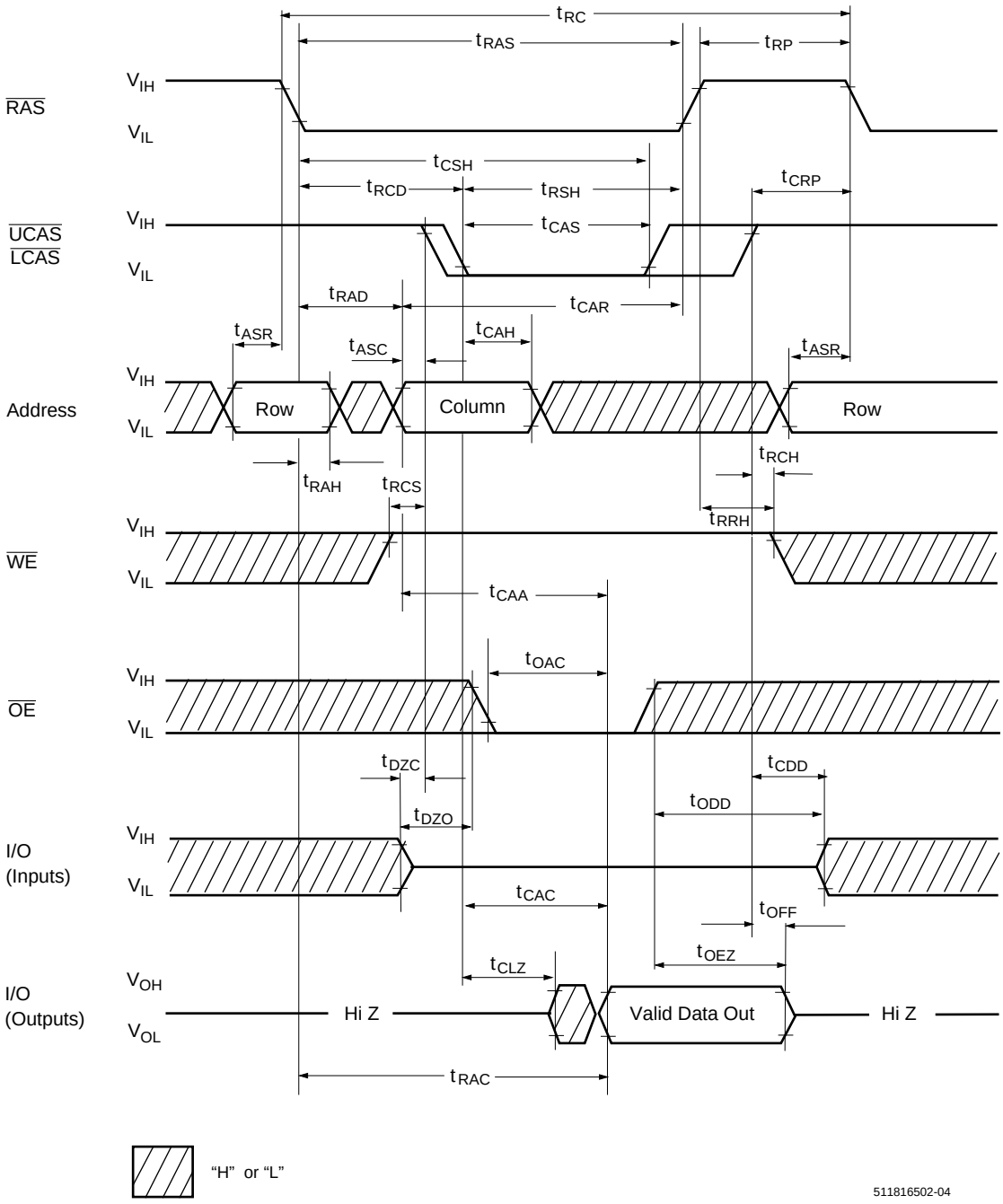
Notes:

1. All voltage are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC7} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during an EDO cycle (t_{HPC}).
5. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 RAS cycles are required.
6. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
7. Measured with a load equivalent to 2 TTL gates and 50 pF (V_{OL} = 0.8V and V_{OH} = 2.0V).
8. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs acheive the open-circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the WE leading edge in read-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} > t_{WCS} (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if t_{RWD} > t_{RWD} (min.), t_{CWD} > t_{CWD} (min.), t_{AWD} > t_{AWD} (min.), and t_{CPWD} > t_{CPWD} (min.), the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
12. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{CAA}.
14. AC measurements assume t_T = 2 ns.
15. Either t_{DZC} or t_{DEO} must be satisfied.
16. Either t_{CDD} or t_{ODD} must be satisfied.
17. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

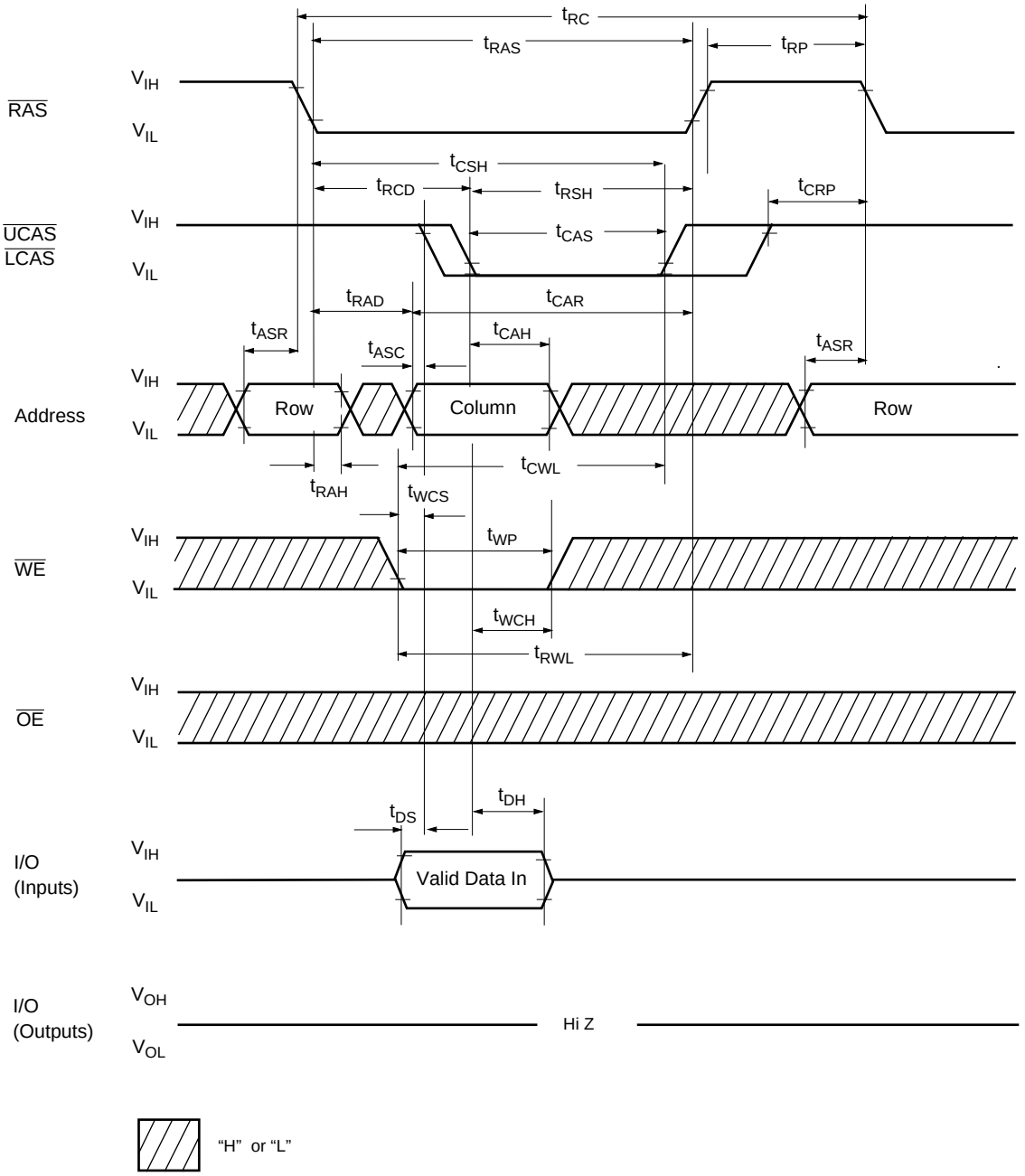
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR – Distributed/Burst; or CBR – Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
18. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

Waveforms of Read Cycle



Waveforms of Write Cycle (Early Write)



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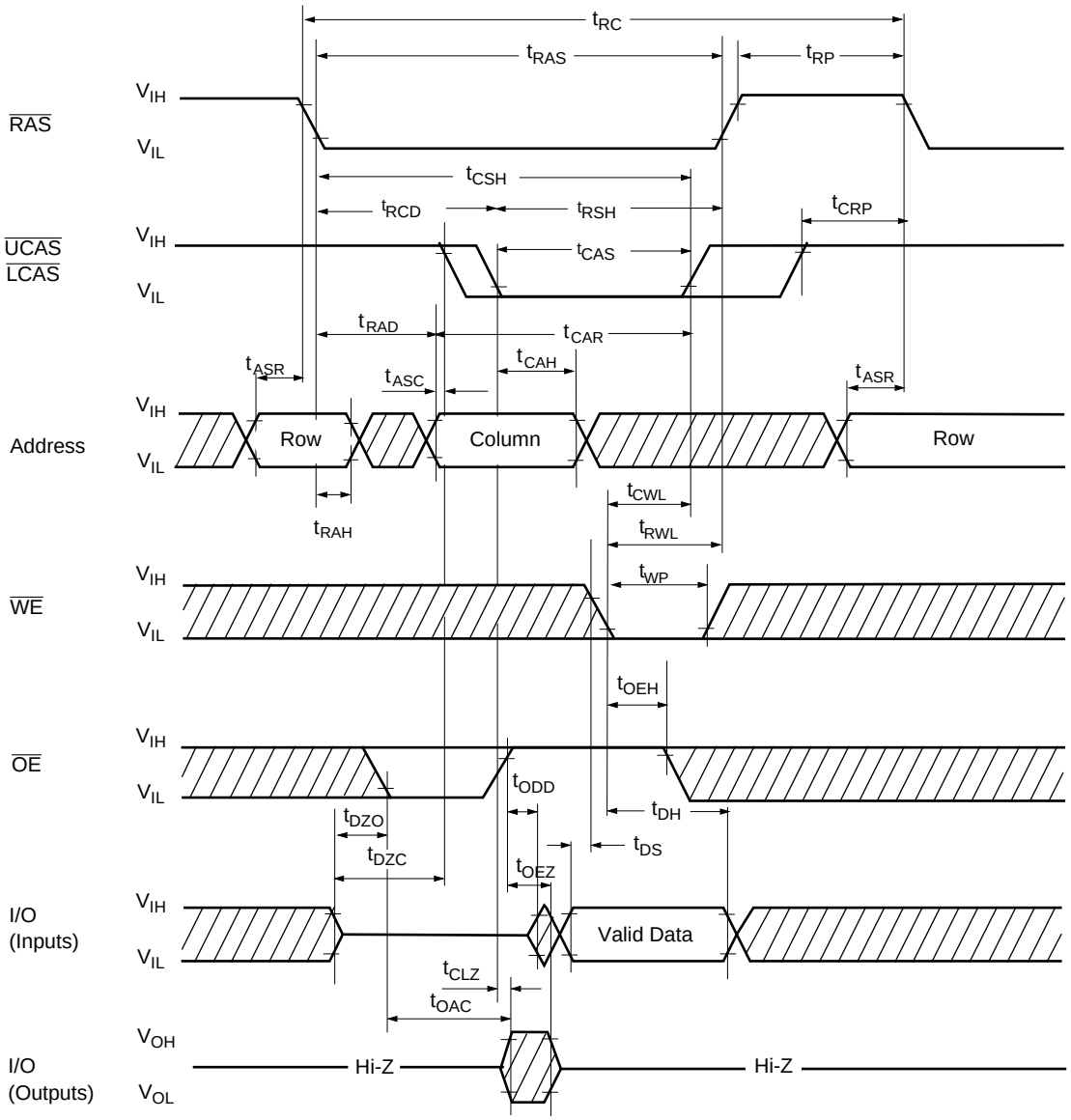
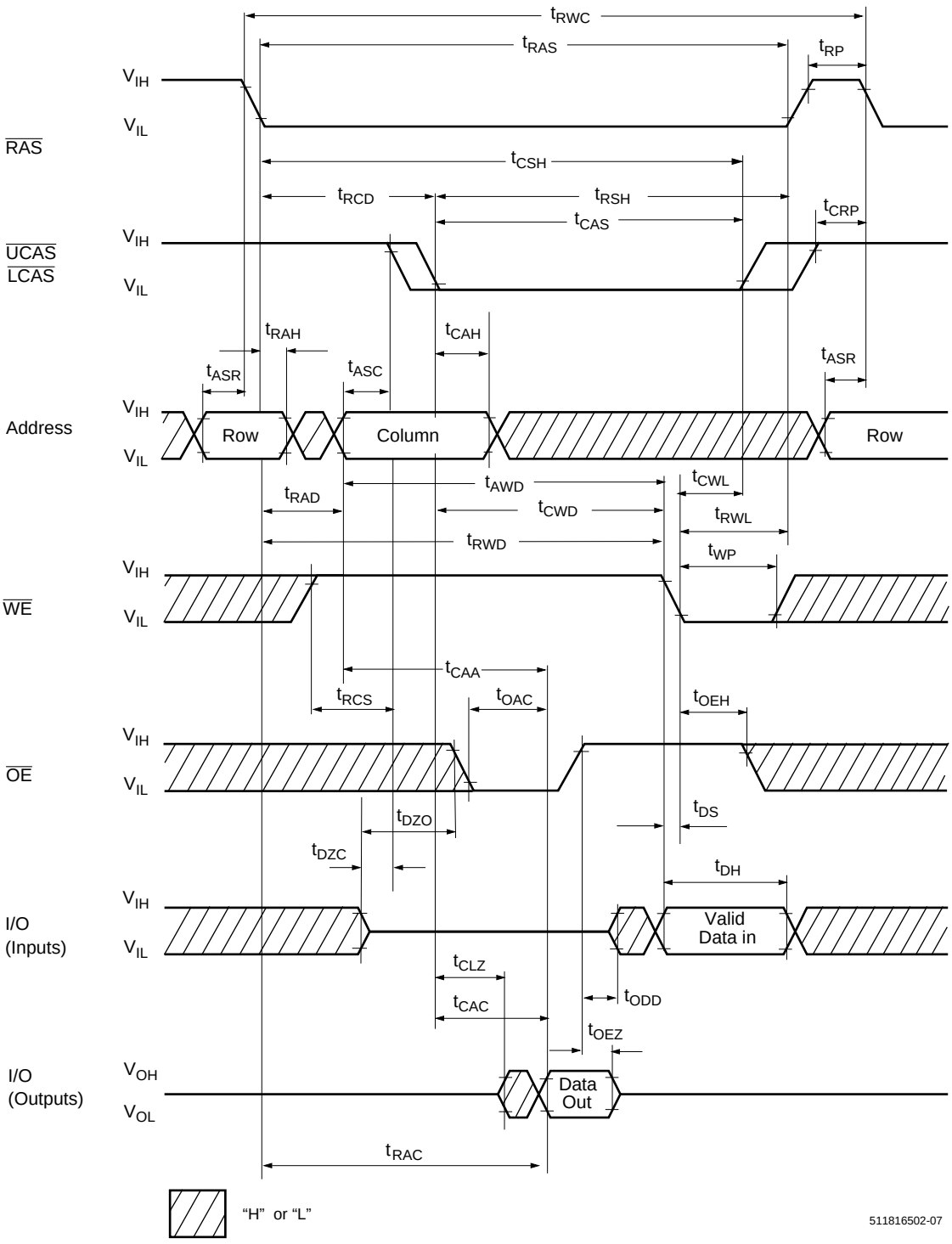
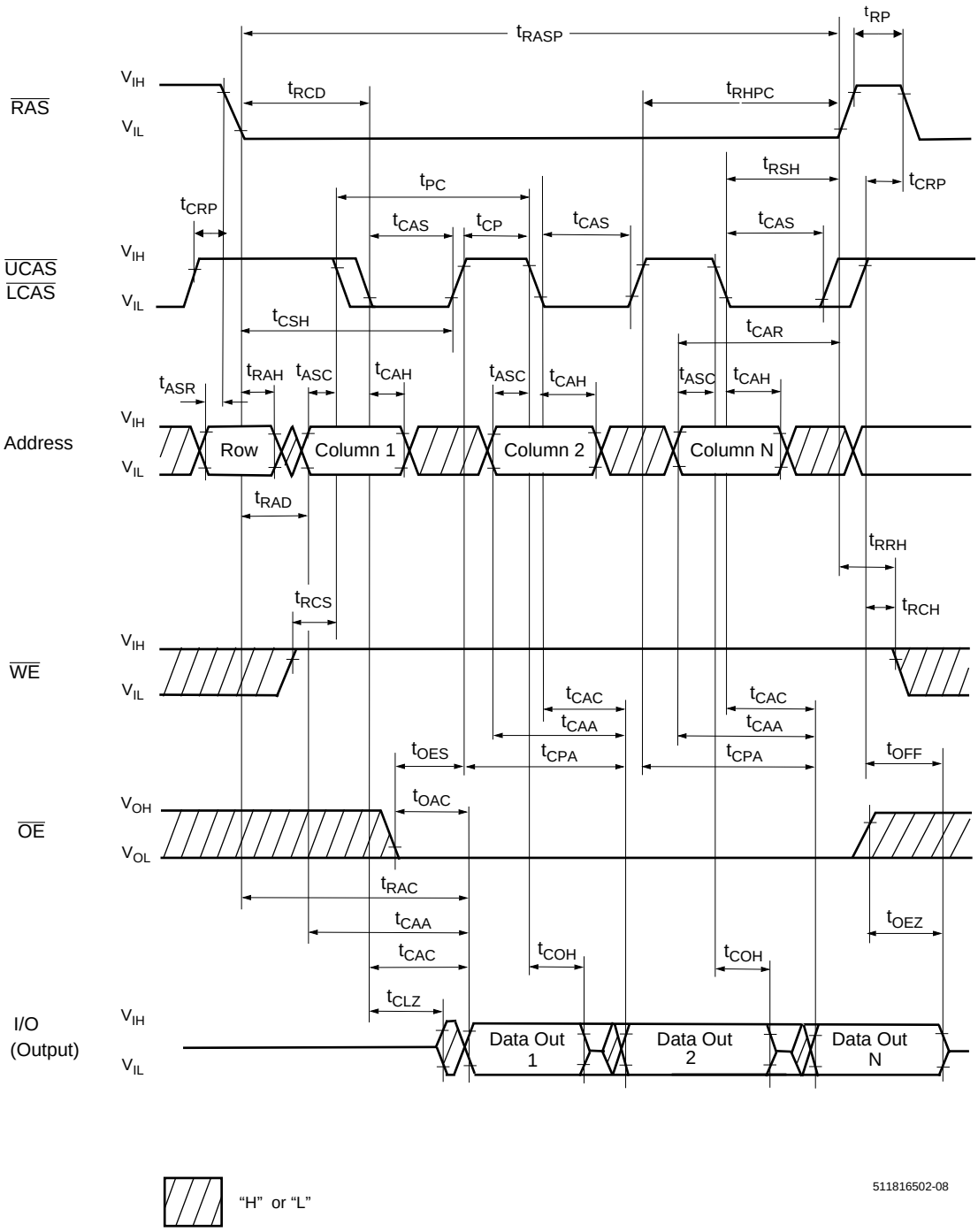
Waveforms of Write Cycle ($\overline{OE}$ Controlled Write)



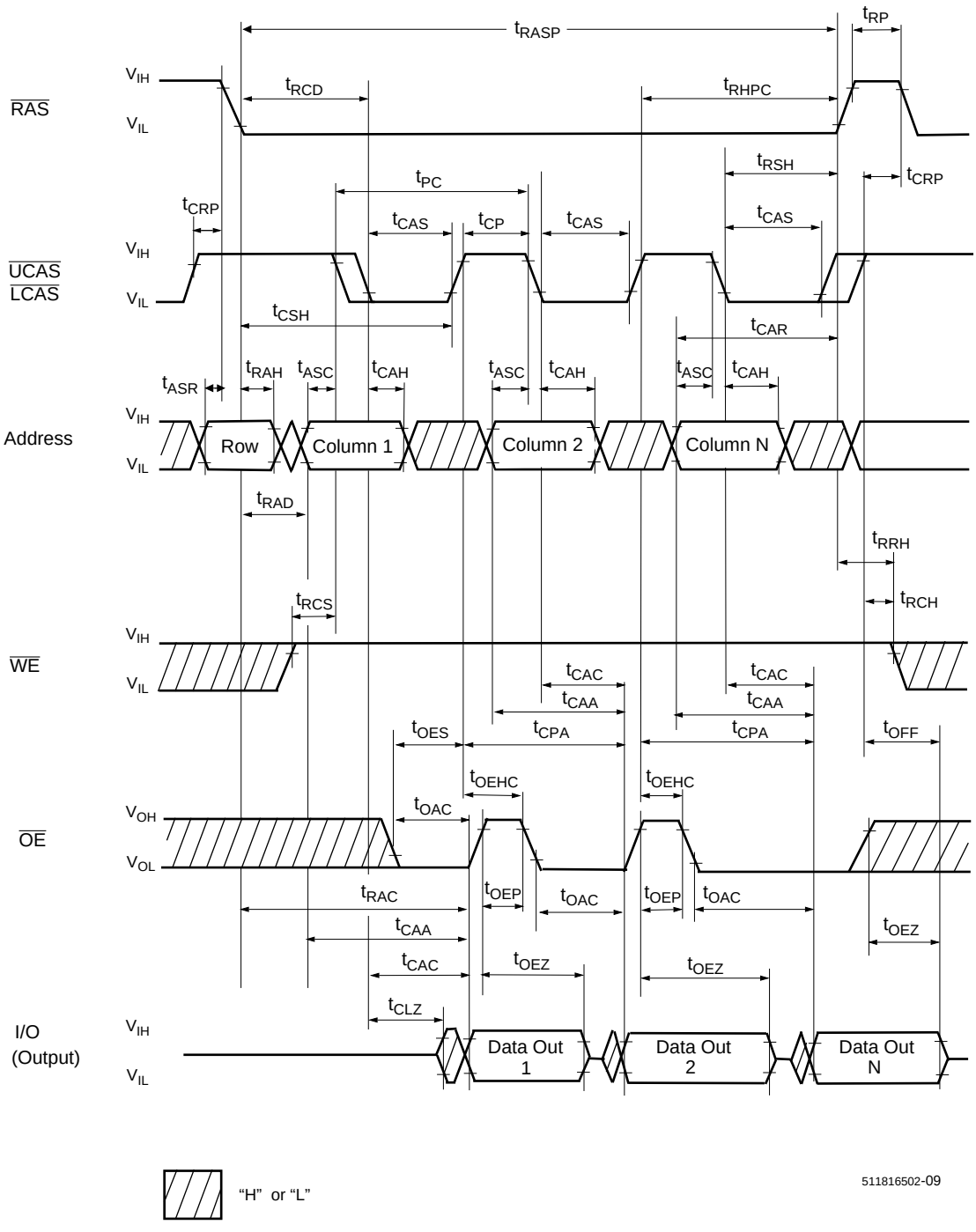
Waveforms of Read-Write (Read-Modify-Write) Cycle



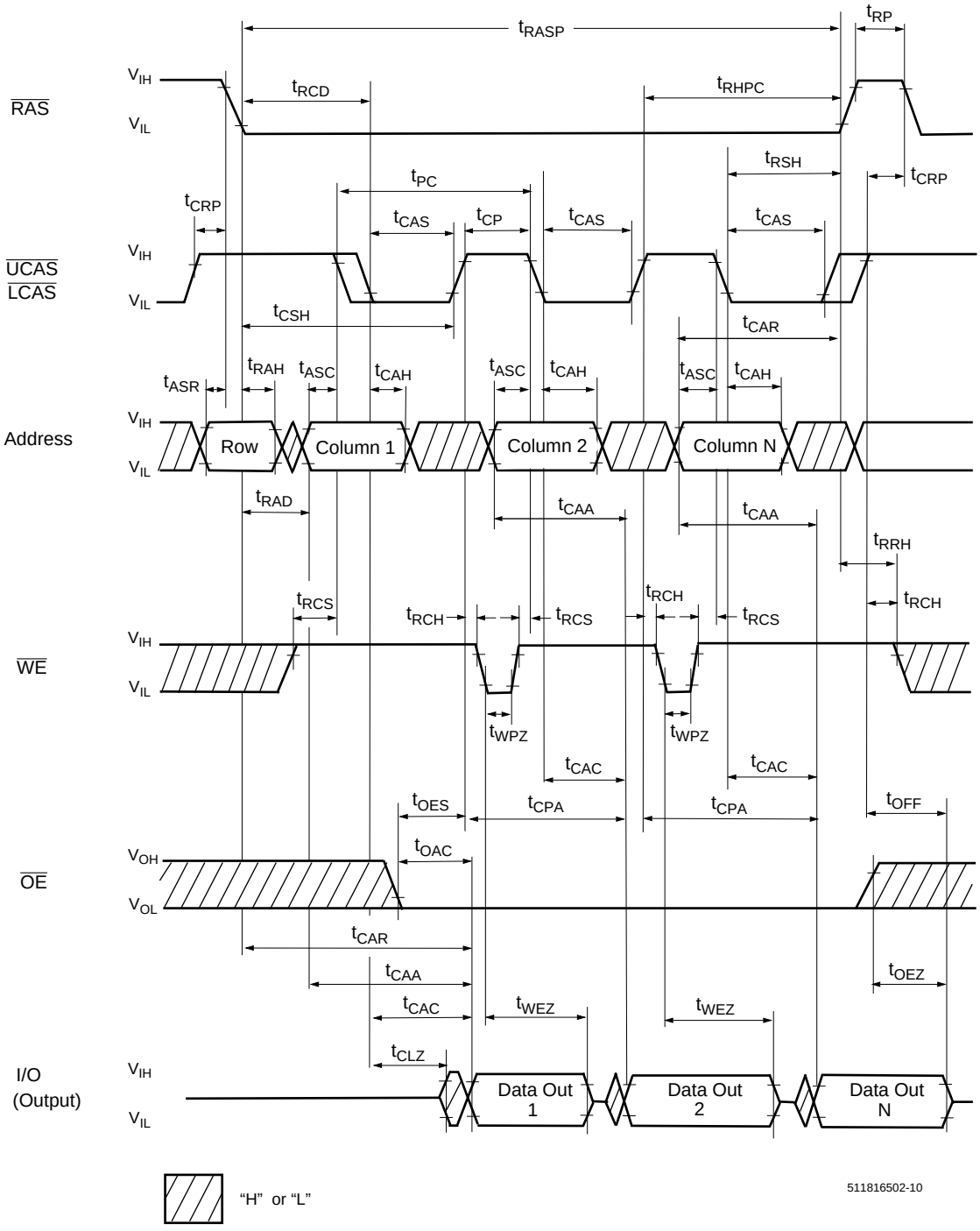
Waveforms of Fast Page Mode Read Cycle



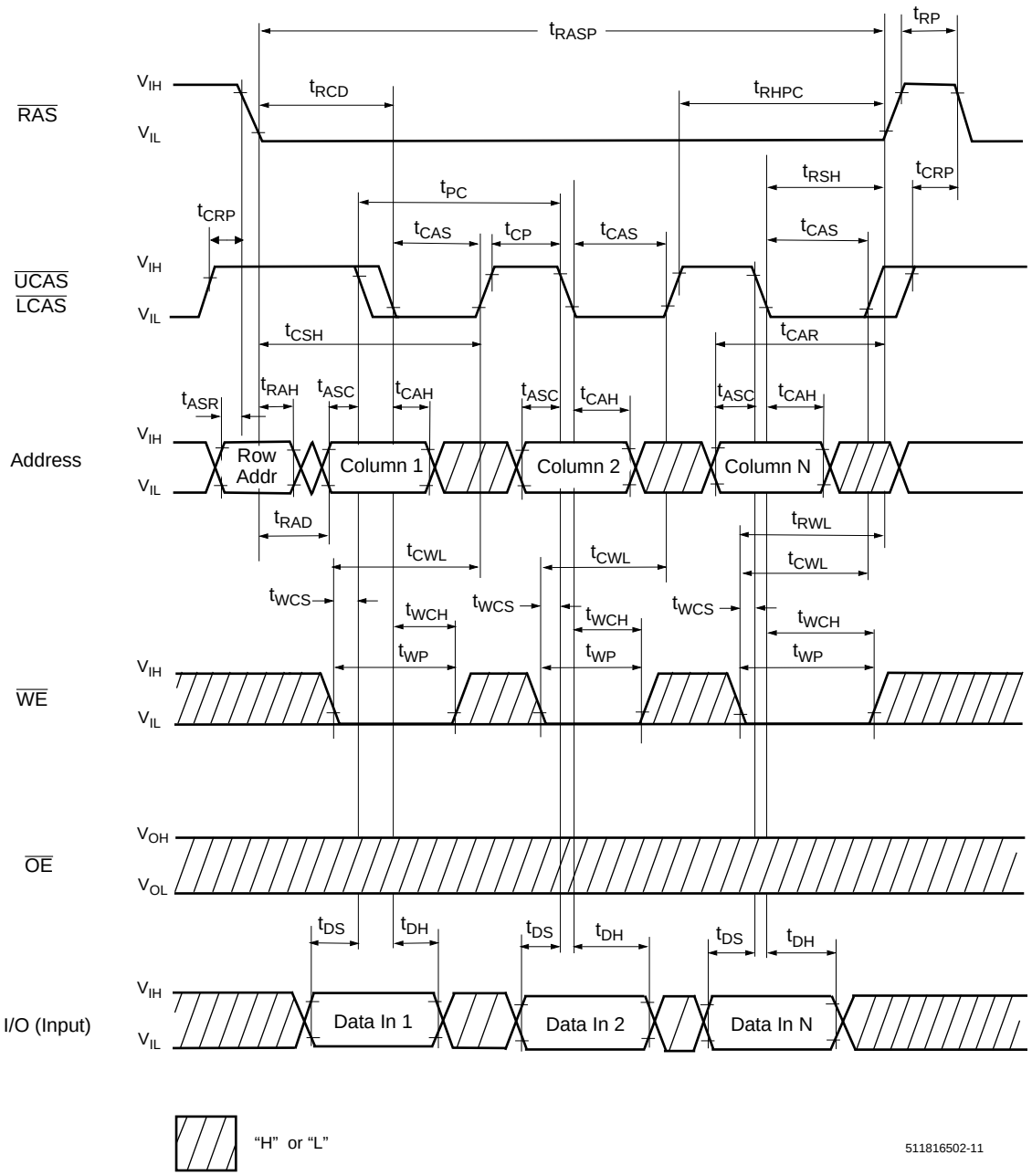
Waveforms of Fast Page Mode Read Cycle ($\overline{OE}$ Control)



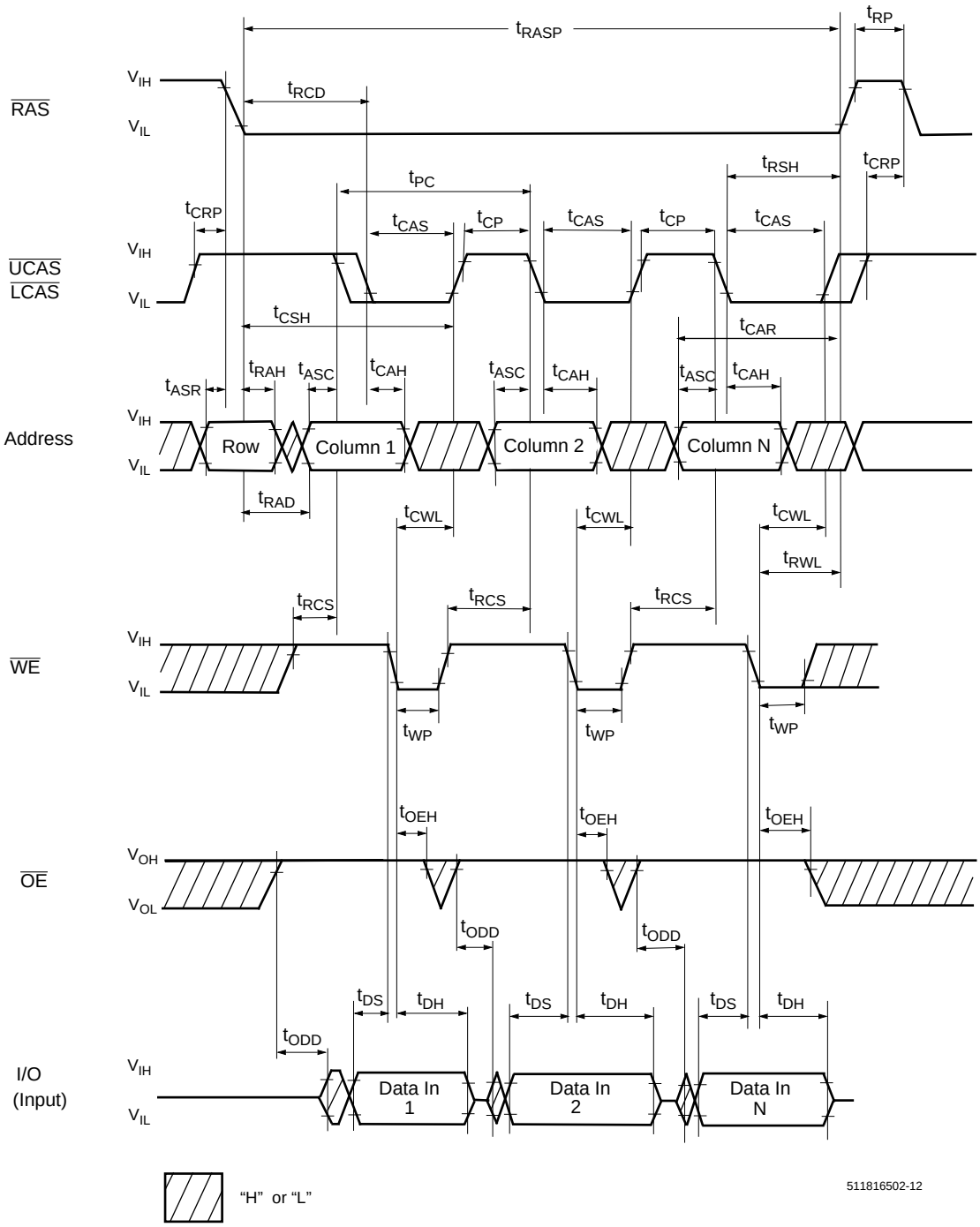
Waveforms of Fast Page Mode Read Cycle ($\overline{WE}$ Control)



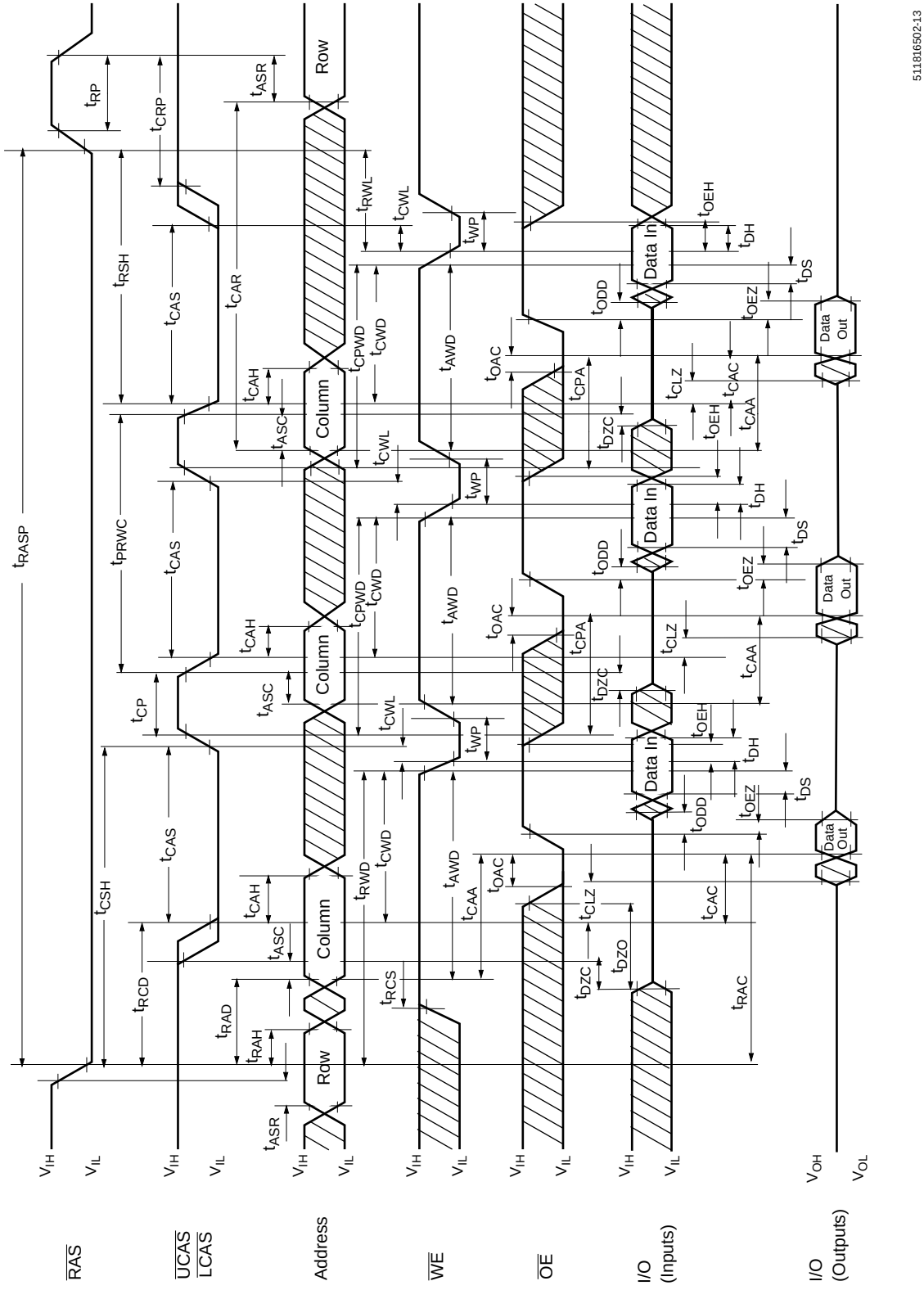
Waveforms of Fast Page Mode Early Write Cycle



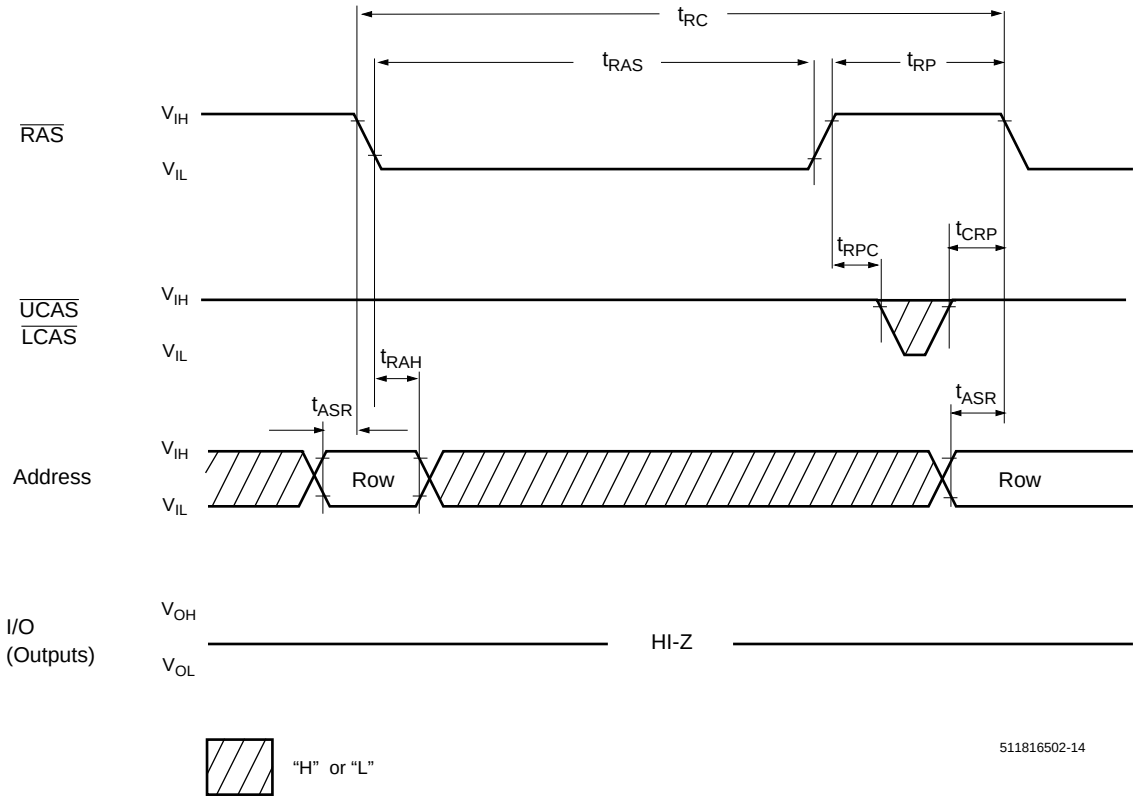
Waveforms of Fast Page Mode Late Write Cycle



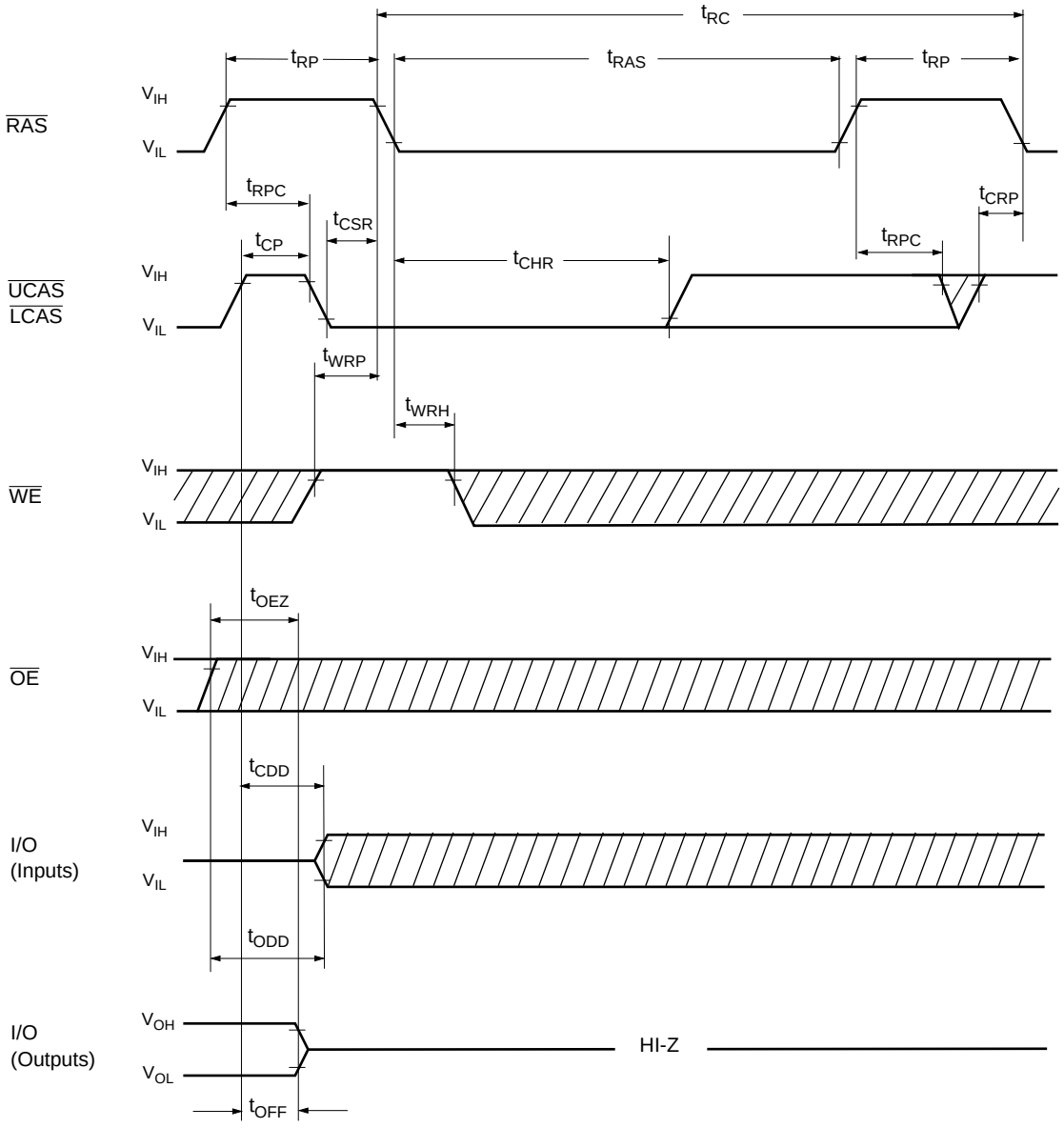
Waveforms of Fast Page Mode Read-Modify-Write Cycle



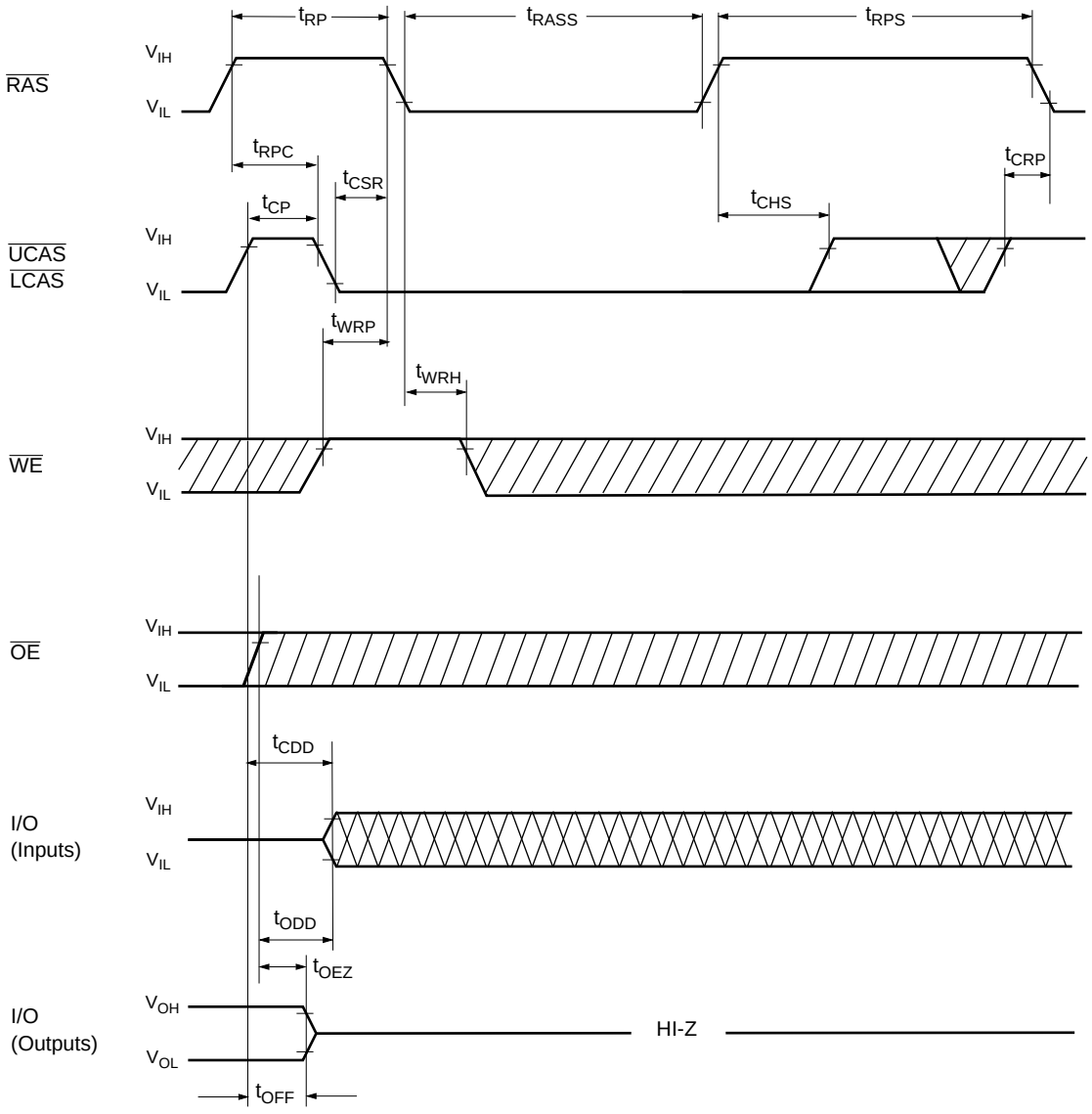
Waveforms of $\overline{RAS}$ Only Refresh Cycle



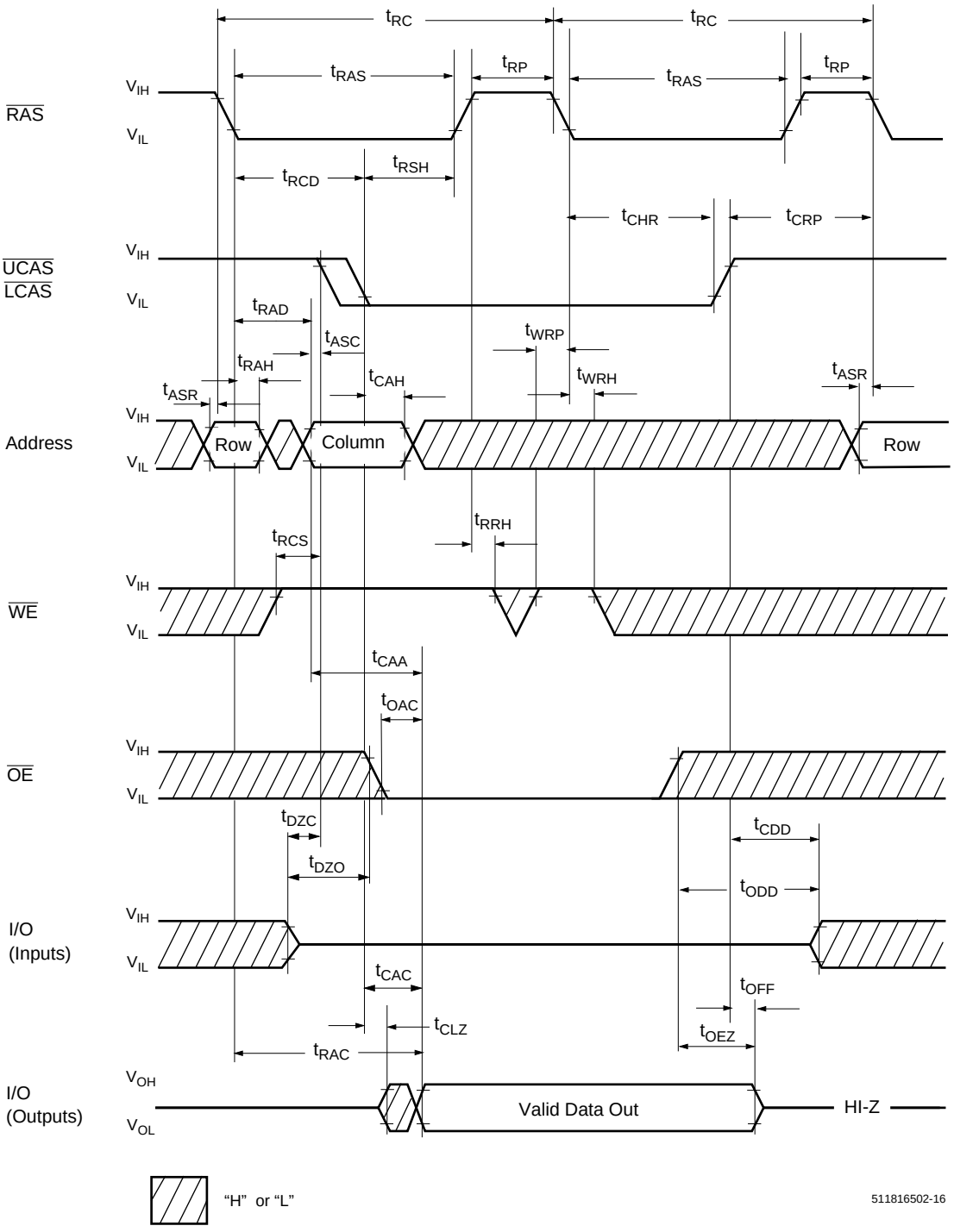
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



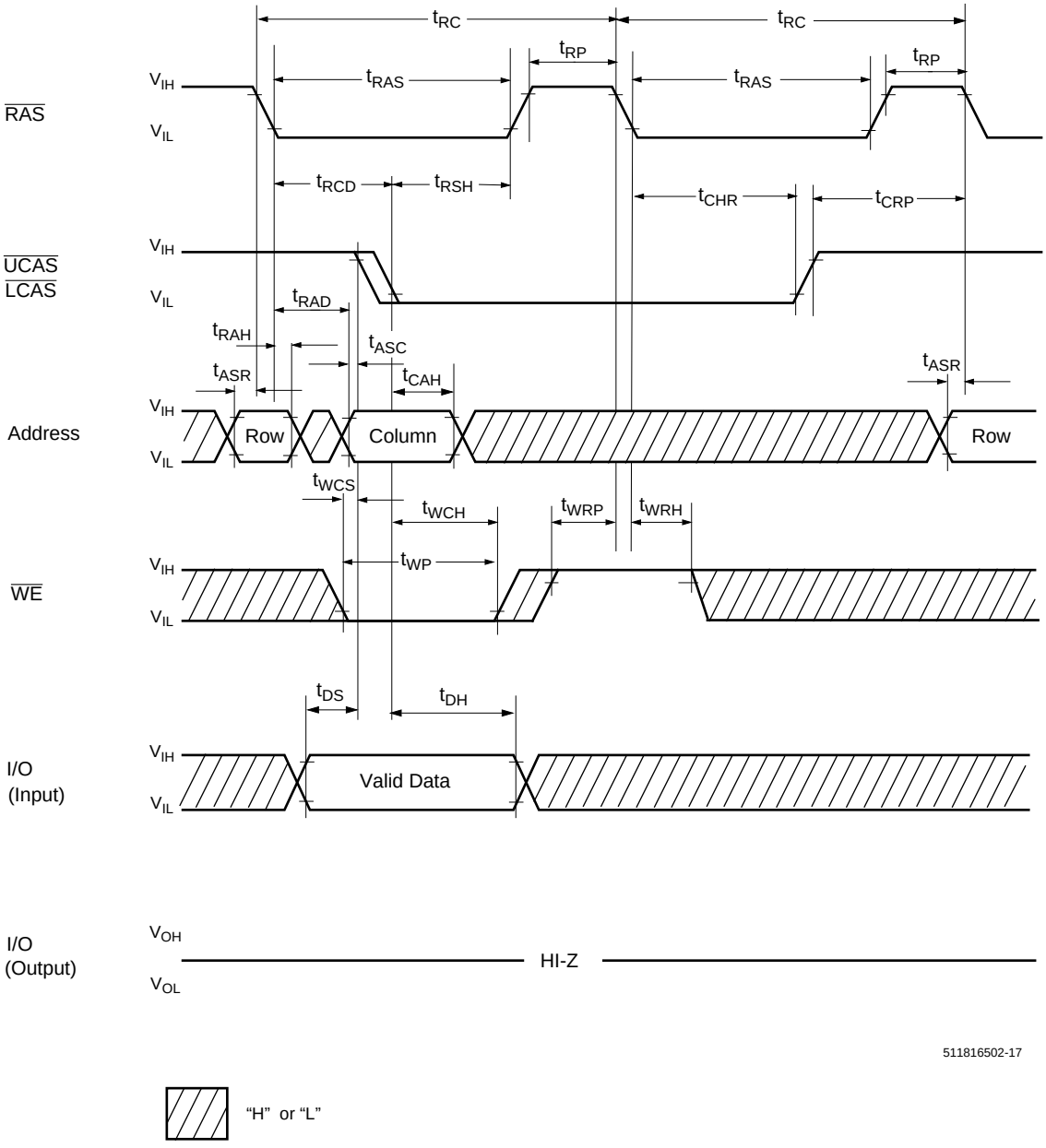
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Self Refresh Cycle (Optional)



Waveforms of Hidden Refresh Read Cycle



Waveforms of Hidden Refresh Early Write Cycle



Functional Description

The V53C318160A is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C318160A reads and writes data by multiplexing an 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Fast Page Mode

Fast Page operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer. During Fast Page operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into EDO Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page provides a sustained data rate of 29 MHz for applications that require high bandwidth such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

Self Refresh

Self Refresh mode provides internal refresh control signals to the DRAM during extended periods of inactivity. Device operation in this mode provides additional power savings and design ease by elimination of external refresh control signals. Self Refresh mode is initialed with a $\overline{CAS}$ before $\overline{RAS}$ (CBR) Refresh cycle, holding both $\overline{RAS}$ low (t_{RASS}) and $\overline{CAS}$ low (t_{CHD}) for a specified period. Both of these parameters are specified with minimum values to guarantee entry into Self Refresh operation. Once the device has been placed in to Self Refresh mode the $\overline{CAS}$ clock is no longer required to maintain Self Refresh operation.

The Self Refresh mode is terminated by returning the $\overline{RAS}$ clock to a high level for a specified (t_{RPS}) minimum time. After termination of the Self Refresh cycle normal accesses to the device may be initiated immediately, poviding that subsequest refresh cycles utilize the $\overline{CAS}$ before $\overline{RAS}$ (CBR) mode of operation.

Data Output Operation

The V53C318160A Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{CC} supply, an initial pause of 200 μs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

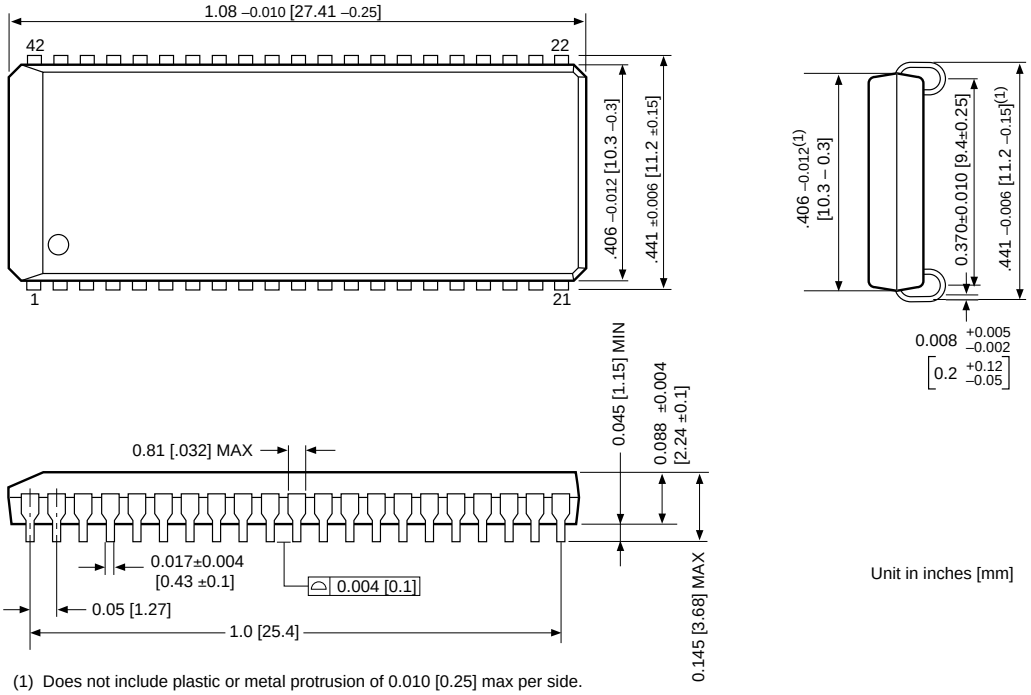
During Power-On, the V_{CC} current requirement of the V53C318160A is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{CC} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C318160A Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
CAS-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Read Cycle	Data from Addressed Memory Cell
EDO Write Cycle (Early Write)	High-Z
EDO Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	High-Z
$\overline{CAS}$-only Cycles	High-Z

Package Diagrams

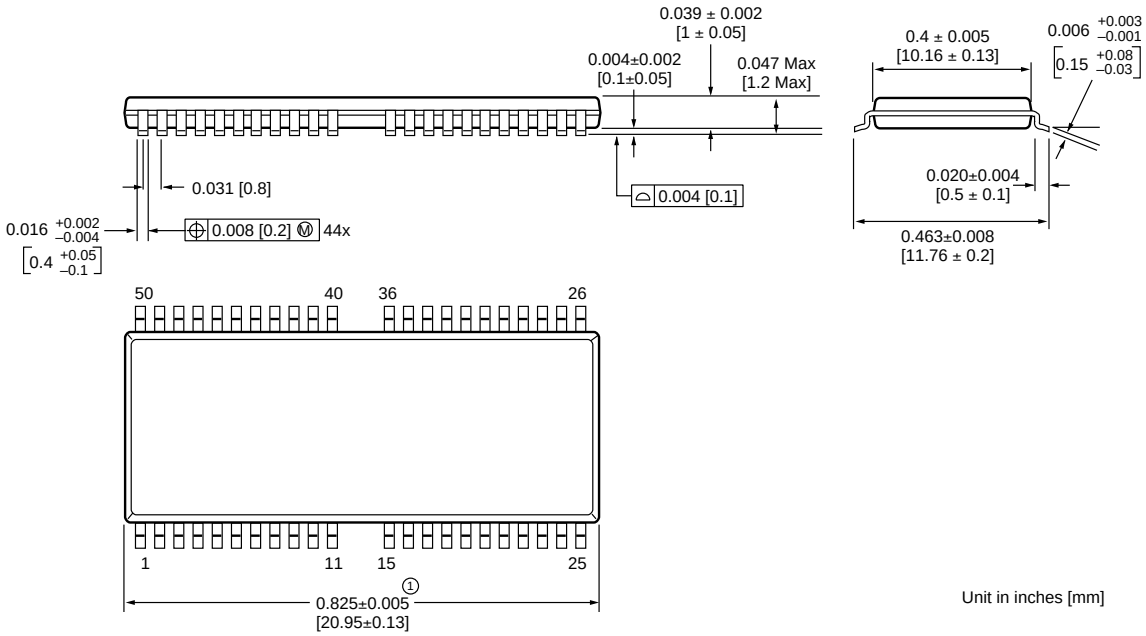
42-Pin 400 mil SOJ



Unit in inches [mm]

(1) Does not include plastic or metal protrusion of 0.010 [0.25] max per side.

50/44-Pin 400 mil TSOP-II



Unit in inches [mm]

① Does not include plastic or metal protrusion of 0.010 [0.25] max. per side

Notes

Notes

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