

# HM628512I Series

524,288-word × 8-bit High Speed CMOS Static RAM

# HITACHI

Preliminary  
Rev. 0.0  
May 12, 1994

The Hitachi HM628512 is a 4M-bit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 μm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 600-mil plastic DIP, is available for high density mounting. L-version is suitable for battery back up system.

## Features

- High speed: Fast access time:  
70/85/100 ns (max)
- Low power  
Standby: 10 μW (typ) (L-version)  
Operation: 75 mW (typ) (f = 1MHz)
- Single 5 V supply
- Completely static memory  
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)

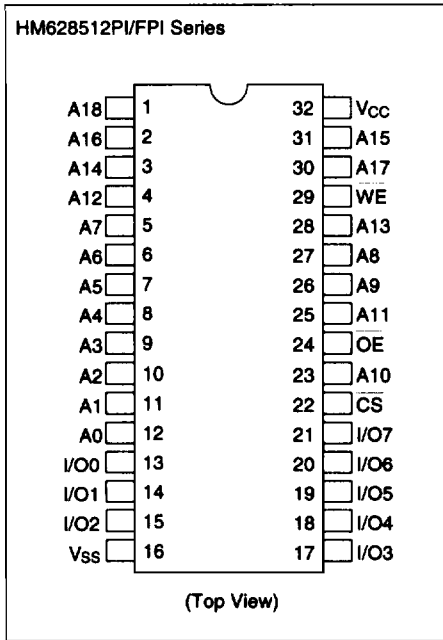
## Ordering Information

Type No.	Access time	Package
HM628512PI-7	70 ns	600-mil 32-pin
HM628512PI-8	85 ns	plastic DIP
HM628512PI-10	100 ns	(DP-32)
HM628512LPI-7	70 ns	
HM628512LPI-8	85 ns	
HM628512LPI-10	100 ns	
HM628512FPI-7	70 ns	525-mil 32-pin
HM628512FPI-8	85 ns	plastic SOP
HM628512FPI-10	100 ns	(FP-32D)
HM628512LFPI-7	70 ns	
HM628512LFPI-8	85 ns	
HM628512LFPI-10	100 ns	

Note: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

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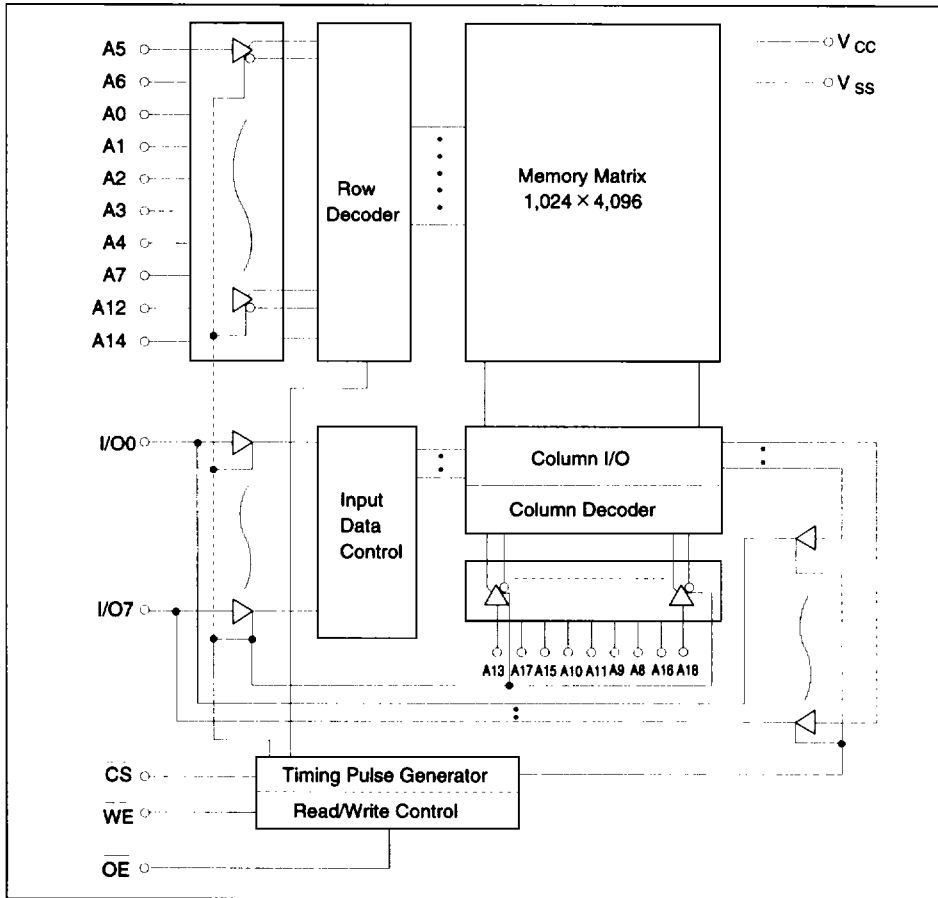
## Pin Arrangement



## Pin Description

Symbol	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

Block Diagram



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### Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
X	H	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: X: H or L

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	$-0.5^{*1}$ to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +125	°C
Storage temperature under bias	Tbias	-40 to +85	°C

Note: 1. -3.0 V for pulse half-width  $\leq$  30 ns

### Recommended DC Operating Conditions ( $T_a = -40$ to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high (logic 1) voltage	$V_{IH}$	2.4	—	6.0	V
Input low (logic 0) voltage	$V_{IL}$	$-0.3^{*1}$	—	0.6	V

Note: 1. -3.0 V for pulse half-width  $\leq$  30 ns

## HM628512I Series

### DC Characteristics (Ta = -40 to +85°C, V<sub>CC</sub> = 5 V ±10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Operating power supply current: DC	I <sub>CC READ</sub>	—	15	30	mA	$\overline{CS} = V_{IL}$ , $\overline{WE} = V_{IH}$ others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	
	I <sub>CC WRITE</sub>	—	20	50	mA	$\overline{CS} = V_{IL}$ , $\overline{WE} = V_{IL}$ others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	
Operating power supply current	-7	I <sub>CC1</sub>	—	60	100	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$ , others = V <sub>IH</sub> /V <sub>IL</sub> I <sub>I/O</sub> = 0 mA
			—	55	90	mA	
	-8/10	I <sub>CC2</sub>	—	15	35	mA	Cycle time = 1 μs, duty = 100% I <sub>I/O</sub> = 0 mA, $\overline{CS} \leq 0.2$ V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V
Standby power supply current: DC	I <sub>SB</sub>	—	1	3	mA	$\overline{CS} = V_{IH}$	
Standby power supply current (1): DC	I <sub>SB1</sub>	—	0.02	2	mA	V <sub>in</sub> ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V	
		—	2	100*2	μA		
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1.0 mA	

- Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.  
2. This characteristics is guaranteed only for L-version.

### Capacitance (Ta = 25°C, f = 1 MHz)\*1

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C <sub>in</sub>	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

- Note: 1. This parameter is sampled and not 100% tested.

## HM628512I Series

AC Characteristics (Ta = -40 to +85°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

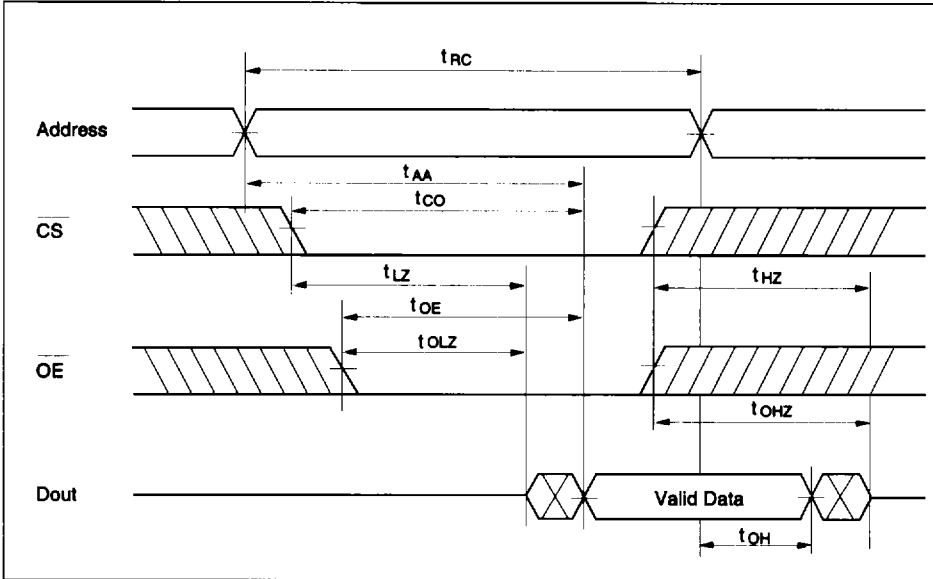
### Test Conditions

- Input pulse levels: 0.5 V to 2.5 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C<sub>L</sub> (100 pF)  
(HM628512I-7/8/10)  
(Including scope & jig)

### Read Cycle

Parameter	Symbol	HM628512I						Unit	Note
		-7		-8		-10			
		Min	Max	Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	70	—	85	—	100	—	ns	
Address access time	t <sub>AA</sub>	—	70	—	85	—	100	ns	
Chip select access time	t <sub>CO</sub>	—	70	—	85	—	100	ns	
Output enable to output valid	t <sub>OE</sub>	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t <sub>LZ</sub>	10	—	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t <sub>HZ</sub>	0	25	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t <sub>OZH</sub>	0	25	0	30	0	35	ns	1, 2, 3
Output hold from address change	t <sub>OH</sub>	10	—	10	—	10	—	ns	

Read Timing Waveform\*4



- Notes:
1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. At any given temperature and voltage condition,  $t_{HZ}$  (max) is less than  $t_{LZ}$  (min).
  3. This parameter is sampled and not 100% tested.
  4.  $\overline{WE}$  is high for read cycle.

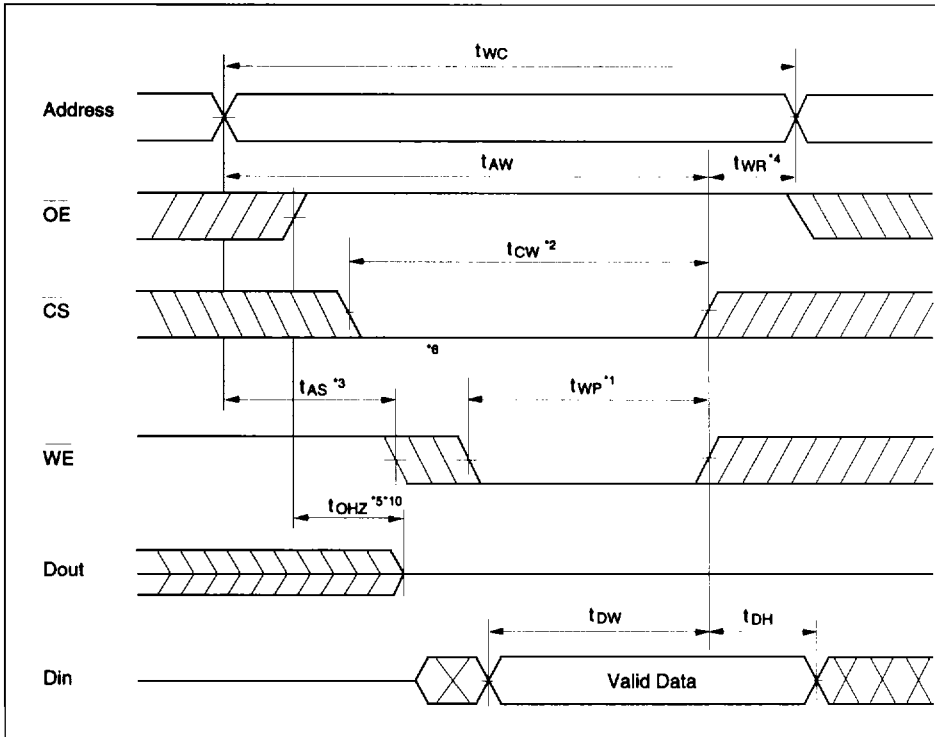
## HM628512I Series

### Write Cycle

Parameter	Symbol	HM628512I						Unit	Note
		-7		-8		-10			
		Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	70	—	85	—	100	—	ns	
Chip selection to end of write	$t_{CW}$	60	—	75	—	80	—	ns	2
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns	3
Address valid to end of write	$t_{AW}$	60	—	75	—	80	—	ns	
Write pulse width	$t_{WP}$	50	—	55	—	60	—	ns	1, 12
Write recovery time	$t_{WR}$	5	—	5	—	5	—	ns	4
$\overline{WE}$ to output in high-Z	$t_{WHZ}$	0	25	0	30	0	35	ns	10, 11
Data to write time overlap	$t_{DW}$	30	—	35	—	40	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	ns	10

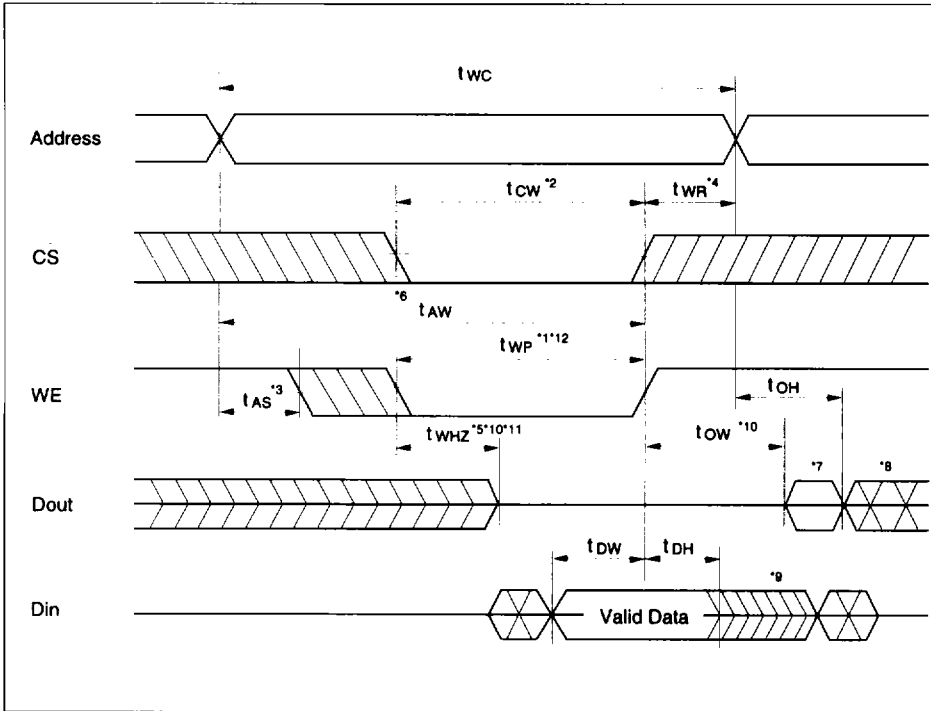


Write Timing Waveform (1) ( $\overline{OE}$  Clock)



## HM628512I Series

### Write Timing Waveform (2) ( $\overline{OE}$ Low Fixed)



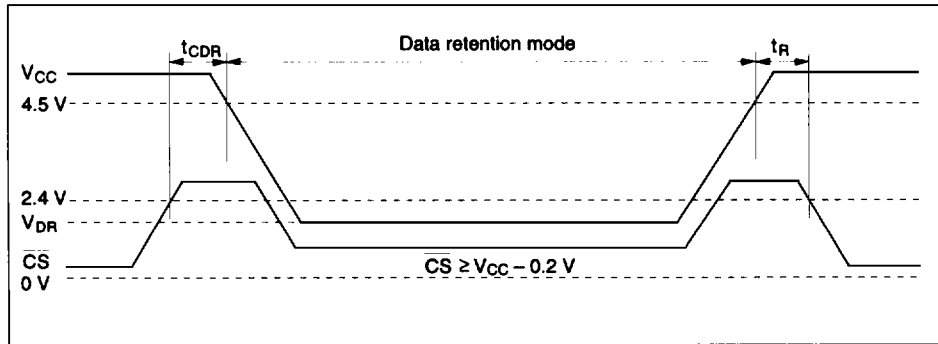
- Notes:
1. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  2.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.
  3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  4.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.
  5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
  6. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.
  7.  $D_{out}$  is the same phase of the write data of this write cycle.
  8.  $D_{out}$  is the read data of next address.
  9. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  10. This parameter is sampled and not 100% tested.
  11.  $t_{WHZ}$  is defined as the time at which the outputs achieve the open circuit conditions and is not referred to output voltage levels.
  12. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW \min} + t_{WHZ \max}$

**Low  $V_{CC}$  Data Retention Characteristics** ( $T_a = -40$  to  $+85^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*2
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq 0$ V
Data retention current	$I_{CCDR}$	—	1*3	50*1	$\mu\text{A}$	$V_{CC} = 3.0$ V, $V_{in} \geq 0$ V $\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

**Low  $V_{CC}$  Data Retention Timing Waveform ( $\overline{CS}$  Controlled)**



- Notes:
1. For L-version and  $20 \mu\text{A}$  (max.) at  $T_a = 0$  to  $40^\circ\text{C}$ .
  2.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. In data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
  3. Typical value is at  $V_{CC} = 3.0$  V,  $T_a = 25^\circ\text{C}$  and specified loading, and not guaranteed.