

OBJECTIVE SPECIFICATIONS

Features

- *Function, pin-out, speed and drive compatibility with 54/74ALS logic family*
- *Low power consumption characteristic of CMOS*
- *High-Drive-Current outputs:*
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- *Inputs and outputs interface directly with TTL, NMOS and CMOS devices*
- *Wide operating voltage range: 4.5V to 5.5V*
- *Characterized for operation over industrial and military temperature ranges:*
74AHCT: -40°C to +85°C
54AHCT: -55°C to +125°C

Dual AND-OR-Invert Gates and Dual AND-OR Gates

Description

The '51 performs the following Boolean functions:

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$

The '58 performs:

$$1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

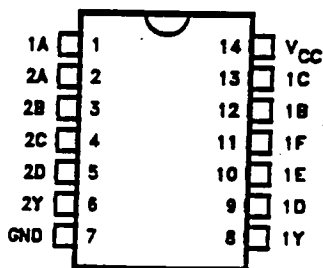
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Function Table

Inputs						Output 1Y	
1A	1B	1C	1D	1E	1F	'51	'58
H	H	H	X	X	X	L	H
X	X	X	H	H	H	L	H
Any Other Combination						H	L

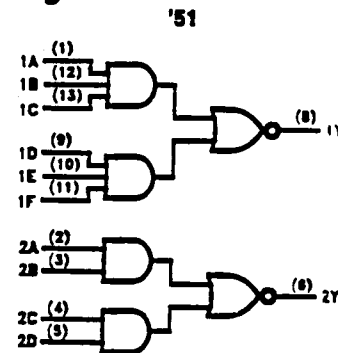
Inputs				Output 2Y	
2A	2B	2C	2D	'51	'58
H	H	X	X	L	H
X	X	H	H	L	H
Any Other Combination				H	L

Pin Configuration

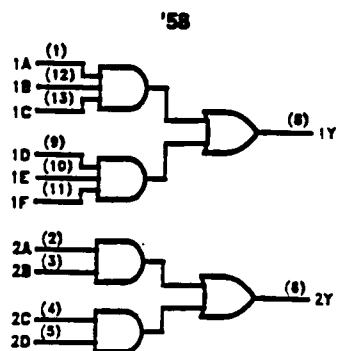


0014-1

Logic Diagrams



0014-2



0014-3

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{STG} -65°C to $+150^\circ\text{C}$
 Power Dissipation Per Package, P_D * 500 mW

*Power Dissipation temperature derating:
 Plastic Package (N): $-12\text{mW}/^\circ\text{C}$ from 65°C to 85°C
 Ceramic Package (J): $-12\text{mW}/^\circ\text{C}$ from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature

Range 74AHCT: -40°C to $+85^\circ\text{C}$
 54AHCT: -55°C to $+125^\circ\text{C}$

Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Sym	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			74AHCT	54AHCT	Unit
			Typ	Guaranteed Limits		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V	
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V	
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu\text{A}$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V	
		$I_O = -4 \text{ mA}$	4.2	3.98	3.84	3.7		
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu\text{A}$ $I_O = 4 \text{ mA}$ $I_O = 8 \text{ mA}$	0	0.1	0.1	0.1	V	
				0.26	0.33	0.4		
				0.39	0.5			
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$		2.0	20.0	40.0	μA	

AC Electrical Characteristics (Input $t_r, t_f \leq 2$ ns), AHCT51, AHCT58

Sym	Parameter	Conditions •	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	74AHCT $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	54AHCT $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay	$C_L = 50$ pF	9	15	18	ns
t_{PHL}			9	15	18	
C_{IN}	Maximum Input Capacitance		5			pF
C_{PD}	Power Dissipation Capacitance*	(per gate)	15			pF

* C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$
 •For AC switching test circuits and timing waveforms see section 2.