BURR-BROWN®

DAC7700 DIE

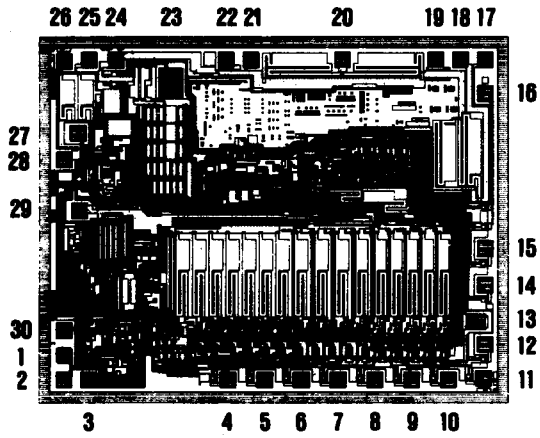
Current Output 16-BIT DIGITAL-TO-ANALOG CONVERTER DIE

DESCRIPTION

The DAC7700KD is complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to −2mA and ±1mA are available.

DIE TOPOGRAPHY



Pad	Function	Pad	Function
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} − 10kΩ
4	Bit 4 Input	19	No Connection
5	Bit 5 Input	20	R_{FB} − 10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	−15V Supply	28	Reference Output
14	Bit 13 Input	29	−15V Supply
15	Bit 14 Input	30	Zener test point. Do not use.

Die size: 153 × 120 mils

Bonding pad size: 4 × 4 mils

Backside Contact: Gold (Must be connected to $-V_{CC}$)

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Tel: (602) 746-111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-611

SPECIFICATIONS

ELECTRICAL PROBE LIMITS [1]

At T_A = +25°C and $\pm V_{CC}$ = 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC7700KD			
PARAMETER	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs				
V_{IH}	+2.4		$+V_{CC}$	V
V_{IL}	−1.0		+0.8	V
I_{IH}, V_I = +2.7V			+40	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Linearity Error[3]		±0.0015	±0.003	% of FSR[4]
Differential Linearity Error[3]		±0.003	±0.006	% of FSR
Gain Error[5]		±0.07	±0.15	%
Zero Error[5] [6]		+1	+2	µA
Monotonicity	14	15		Bits
OUTPUT				
Unipolar (CSB Code)[8]		0 to −2		mA
Output Impedance[8]		4		kΩ
Bipolar (COB Code)[8]		±1		mA
Output Impedance[8]		2.45		kΩ
Compliance Voltage		±2.5		V
REFERENCE VOLTAGE				
Voltage	+6.0	+6.3	+6.6	V
Source Current Available for External Loads		+2.5		mA
POWER SUPPLY REQUIREMENTS				
Voltage:				
$+V_{CC}$	11.4	15	16.5	V
$-V_{CC}$	11.4	15	16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current (no load)				
$+V_{CC}$		+10	+25	mA
$-V_{CC}$		−13	−25	mA
V_{DD}			+8	mA
Power Dissipation (V_{DD} = +5.0V)[9]		365	790	mW
TEMPERATURE RANGE				
Specification:	0		70	°C

PERFORMANCE CHARACTERISTICS

Parameters included are for design information and are not guaranteed or subject to test.

PARAMETER	MIN	TYP	MAX	UNITS
DRIFT(over specification temperature range)				
Total Error Over Temperature Range (all models)[10]		±.08	±0.15	% of FSR
Total Full Scale Drift:				
Unipolar models		±10	±30	ppm of FSR/°C
Bipolar models		±10	±25	ppm of FSR/°C
Gain Drift (all models)		±10	±25	ppm/°C
Zero Drift:				
Unipolar models		±2.5	±5	ppm of FSR/°C
Bipolar models		±5	±12	ppm of FSR/°C
Differential Linearity Over Temp.[3]			+0.009, −0.006	% of FSR
Linearity Error Over Temp.[3]			±0.006	% of FSR

PERFORMANCE CHARACTERISTICS (CONT)

PARAMETER	MIN	TYP	MAX	UNITS
Reference Temperature Coefficient			25	ppm/°C
SETTLING TIME (to ±0.003% of FSR)[7]				
Full Scale Step (2mA), 10 to 100Ω load		350	1000	nsec
1kΩ load		1	3	µsec

NOTES: (1) All dice are 100% probe tested and guaranteed to meet the above probe limits. Due to possible wafer saw and assembly shifts, probe parameters are not guaranteed for assembled units. (2) DAC7700KD is specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) ±0.0015% of full-scale range is equivalent to 1LSB in 16-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 14-bit resolution. (4) FSR means full-scale range and is 20V for the ±10V range, 10V for the 0 to +10V range. FSR is 2mA for the ±1mA range and the 0 to +2mA range. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for CSB operation, $7FFF_H$ for COB operation. (7) Maximum represents the 3σ limit. Not 100% tested for this parameter. (8) Tolerance on output impedance and output current is ±30%. (9) Power dissipation is an additional 40mW when V_{DD} is operated at +15V. (10) With gain and zero errors adjusted to zero at +25°C.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to R_F	±18V
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGING

DAC7700 dice are visually inspected to MIL-STD-883, Method 2010, Test Condition B, and are shipped in sealed carriers.

ORDERING INFORMATION

DAC7700 K D

Basic Model Number

Grade/Temperature Range
K = 0°C to +70°C

Package Code
D = Die

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor may be needed from Gain Adjust to Common to reduce noise pickup. Refer to Figures 2 and 3 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram, Figure 4, for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

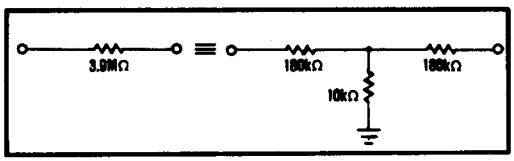

FIGURE 1. Equivalent Resistances.

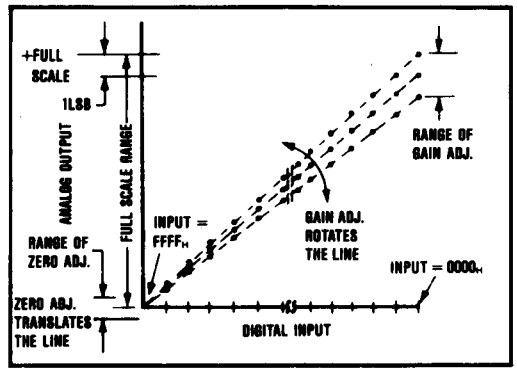

FIGURE 2. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters.

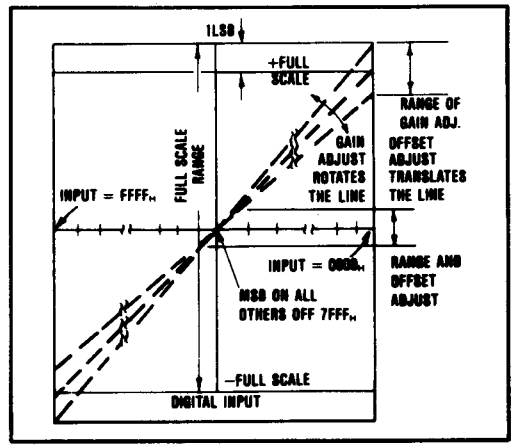

FIGURE 3. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters.

TABLE I. Digital Input and Analog Output Relationships.

CURRENT OUTPUT MODES							
	Analog Output						
	Unipolar, 0 to −2mA			Bipolar, ±1mA			
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	Units
One LSB	0.031	0.061	0.122	0.031	0.061	0.122	μA
0000$_H$	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988	mA
FFFF$_H$	0	0	0	+1.00000	+1.00000	+1.00000	mA
7FFF$_H$	−1.00000	−1.00000	−1.00000	0	0	0	mA

VOLTAGE OUTPUT MODES (WITH EXTERNAL OP-AMP)										
	Analog Output									
	Unipolar, 0 to +10V			Bipolar, ±10V			Bipolar, ±5V			
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit	Units
One LSB	153	305	610	305	610	1224	153	305	610	μV
0000$_H$	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878	+4.99985	+4.99969	+4.99939	V
FFFF$_H$	0	0	0	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V
7FFF$_H$	+5.00000	+5.00000	+5.00000	0	0	0	0	0	0	V

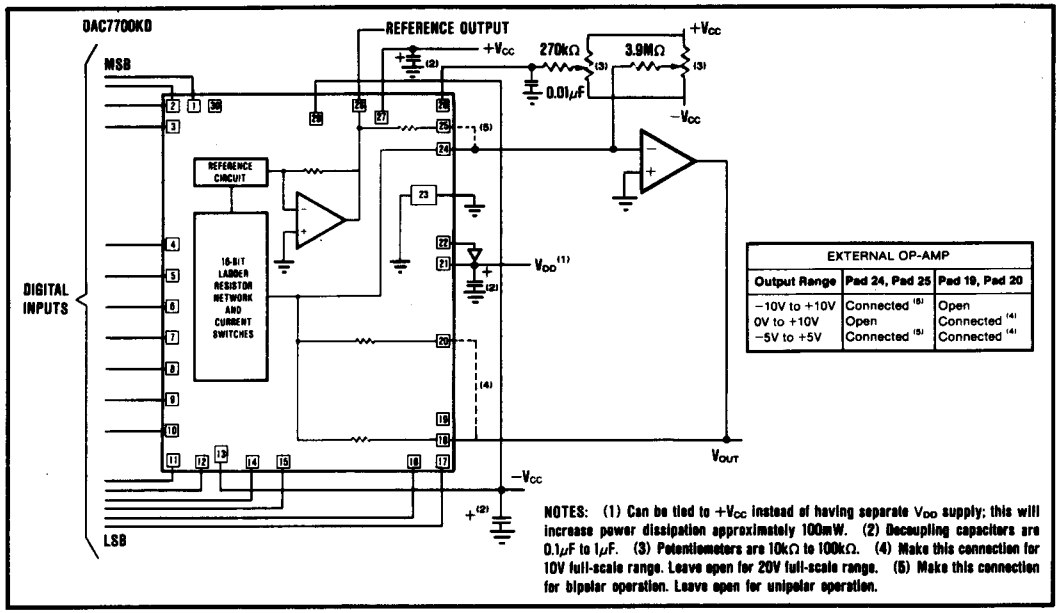

FIGURE 4. Connection Diagram.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and Figure 4 for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter connected for a +10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 5 and 6, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located

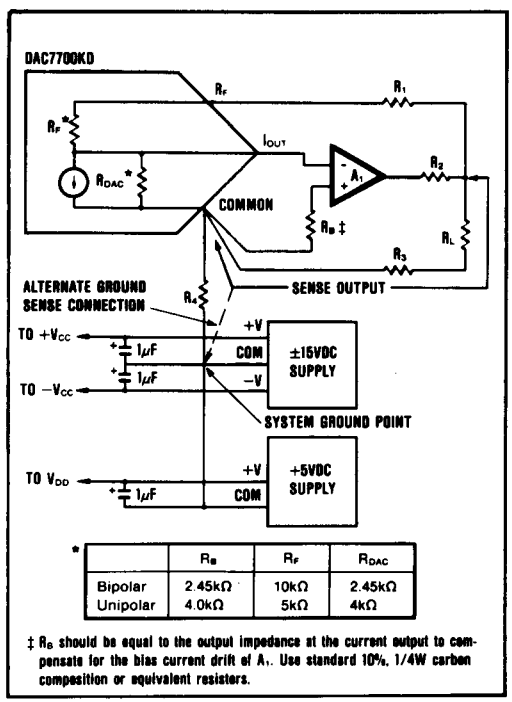

FIGURE 5. Preferred External Op Amp Configuration.

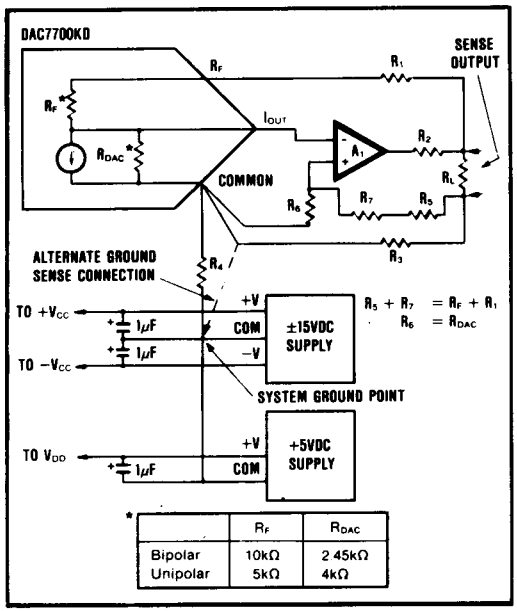

FIGURE 6. Differential Sensing Output Op Amp Configuration.

as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the common pad. Sensing the output voltage at the system ground point is permissible with the DAC7700 because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5 and 6.

Figures 5 and 6 show two methods of connecting the current output model DAC7700 with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 6 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 6 can be reduced to the one shown in Figure 5. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.