SDLS166 OCTOBER 1976 - REVISED MARCH 1988

### Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

#### description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

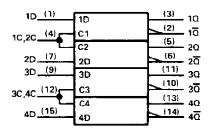
All inputs are diode-clamped to minimize transmissionline effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of - 55°C to 125°C; SN74LS375 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE** (EACH LATCH) INPUTS OUTPUTS D G Q ā I ī Ħ Н н H L  $\underline{\sigma}^{\vec{0}}$  $\sigma^{0}$ L

H = high lever, L = low level, X = irrelevant

 $Q_{\overline{Q}}$  = the level of Q before the high-to low transition of C.

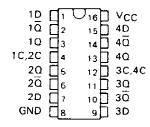
# logic symbol<sup>†</sup>



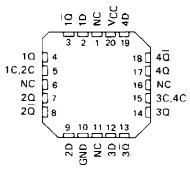
<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and JEC Publication 617-12

Pin numbers shown are for D, J, N, and W packages.

#### SN54LS375 . . . J OR W PACKAGE SN74LS375 . . . D OR N PACKAGE (TOP VIEW)

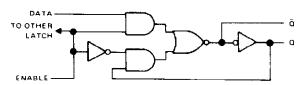


#### SN54LS375 . . . FK PACKAGE (TOP VIEW)

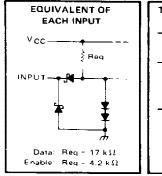


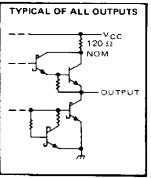
NC - No internal connection

## logic diagram (each latch)



#### schematics of inputs and outputs





PRODUCTION DATA documents contain information current as of publication data. Products conform to specifications per the torms of Taxes instruments standard warranty. Production processing does not necessarily include testing of all perameters.



# SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

lute maximum ratings over operating free-ai		2111	P (51	ull	4,6	, ai	.90	. , u	 	Ψŧ	 	JC	 100	• •			
Supply voltage, VCC (see Note 1)																-	
Input voltage																	
Operating free-air temperature range: SN54LS375	5														-55	S°C 1	io 12
SN74LS379	5															0°C	to 7
Storage temperature range															-65	°C ·	to 15

### recommended operating conditions

			SN54LS375			SN74LS375			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4,75	5	5.25	V	
VIH	High-lever input voltage	2			2			$\overline{}$	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level autput current			~ 0.4		_	- 0.4	mA	
<sup>I</sup> OL	Low-level output current			4			8	mΑ	
t <sub>w</sub>	Width of enabling pulse	20		W	20			ns	
:setup	Setup time	20			20	-		ns	
thold	Hold time	0			- 0			пѕ	
TA	Operating free-air temperature	- 55		125	0		70	°C	

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DARAMETER	TEST COND		SN54LS	375					
PARAMETER	[ES] COND	MIN	TYP ‡	MAX	MIN	TYP‡	MAX	UNIT	
ViK	V <sub>CC</sub> = MIN, 1 <sub>1</sub> = -18 mA				-1.5			- 1.5	V
Vон	$V_{CC} = MIN, V_{IH} = 2 V,$ $I_{OH} = -0.4 \text{ mA}$	VIL = MAX	2.5	3.5	•	2.7	3.5		٧
V	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,	IOL = 4 mA		0.25	0.4		0.25		V
VOL	VIL = MAX	IOL = 8 mA					0.35	0.5	1 *
	V <sub>CC</sub> = MAX. V <sub>i</sub> = 7 V	D input			0.1			0.1	mA
14	VCC = IVIAX. V) = 7V	Cinput			0.4			0.4	1 "
,	V <sub>CC</sub> = MAX V <sub>I</sub> = 2.7 V	D input			20			20	
IН	VCC - WIAX V - 2.7 V	C input			80			80	Α.,
,	V MANY 17 - DAY	D input			- 0.4			- 0.4	mA
1 <sub>1</sub> E	$V_{CC} = MAX$ , $V_{\parallel} = 0.4 V$	Cinput			- 16			- 1.6	1 ""^
1 <sub>Q5</sub> ;	V <sub>CC</sub> = MAX		-20		- 100	-20		- 100	mΑ
¹CC	VCC = MAX. See Note 2			6.3	12		6.3	12	mΑ

 $<sup>\</sup>dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP	MAX	UNIT
<sup>1</sup> PL H	D	0		15	27	D.
1PHL .	IL ,			9	17	ns
tpLH	D	ā	$R_L = 2 k \Omega$ , $C_L = 15 pF$	12	20	200
tPHL			7 L 2 K42. CL - 13 B1	7	15	ns
†PLH				15	27	
<sup>†</sup> PHL				14	25	ns
1PLH	C	ā		16	30	
<sup>†</sup> PHL				7	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



<sup>\$</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 \text{ C}$ .

\$ Not more than one output should be shorted at a time.

NOTE 2  $^{-1}CC$  is tested with all inputs grounded and all outputs open

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PRODUCT SUPPORT: TRAINING

## SN74LS375, Quad bistable latches

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54LS375	SN74LS375
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	4	4
th (ns)		0
tpd max (ns)		27
tsu (ns)		20

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Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

▲Back to Top DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Full datasheet in Acrobat PDF: sn74ls375.pdf (147 KB) (Updated: 03/01/1988)

#### APPLICATION NOTES

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View Application Notes for <u>Digital Logic</u>

- Designing With Logic (Rev. C) (SDYA009C Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 Updated: 10/01/1996)
- Live Insertion (SDYA012 Updated: 10/01/1996)

#### RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB Updated: 04/22/2002)

# PRICING/AVAILABILITY/PKG

DEVICE INFOR	VAILABILITY, RMATION	FRG						INVENTORY STAT :00 PM GMT, 26 S			D DISTRIBUTOR IN B:00 PM GMT, 26 Se	
ORDERABLE DEVICE	<u>STATUS</u>	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY   \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS375D	ACTIVE	SOP   16	0 TO 70	View Contents	1KU   0.38	40	<u>N/A*</u>	5694   03 Oct	4 WKS			
								>10k   10 Oct				
								>10k   17 Oct				
								>10k   07 Nov				
								>10k   15 Nov				
SN74LS375DR	ACTIVE	SOP   16	0 TO 70	View Contents	1KU   0.41	2500	<u>N/A*</u>	1114   03 Oct	4 WKS			
								>10k   10 Oct				
								>10k   17 Oct				
								>10k   07 Nov				
								>10k   15 Nov				
SN74LS375J	OBSOLETE	<u>CDIP</u>   16	0 TO 70	View Contents	1KU		<u>N/A*</u>		Not Available			
SN74LS375N	ACTIVE	PDIP   16	0 TO 70	View Contents	1KU   0.32	25	<u>N/A*</u>	>10k   02 Oct	4 WKS			
								4748   04 Oct				
1												

								>10k   09 Oct			
								200   11 Oct			
								>10k   16 Oct			
SN74LS375N3	OBSOLETE	PDIP   16	0 TO 70	View Contents	1KU		<u>N/A*</u>		Not Available		
SN74LS375NSR	ACTIVE	SOP   16		View Contents	1KU   0.32	2000	<u>N/A*</u>	1327   23 Sep	4 WKS		
								4724   04 Oct			
								2302   11 Oct			
								>10k   18 Oct			
								>10k   08 Nov			

Table Data Updated on: 9/26/2002

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