Integrated Device Technology, Inc.

CMOS HIGH-SPEED STATIC RAM 72K (8K x 9-BIT) With Address Latches

PRELIMINARY INFORMATION
IDT71569

FEATURES:

- 8192-words x 9-bits organization
- Address Latch
- Fast access time:
  - — Commercial: 20/25ns
  - — Military: 25/35ns
- Battery backup operation – 2V data retention voltage (L-version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL compatible
- Military product available compliant to MIL-STD-883, Class B
- JEDEC standard 28-pin DIP and SOJ plastic packages

DESCRIPTION:

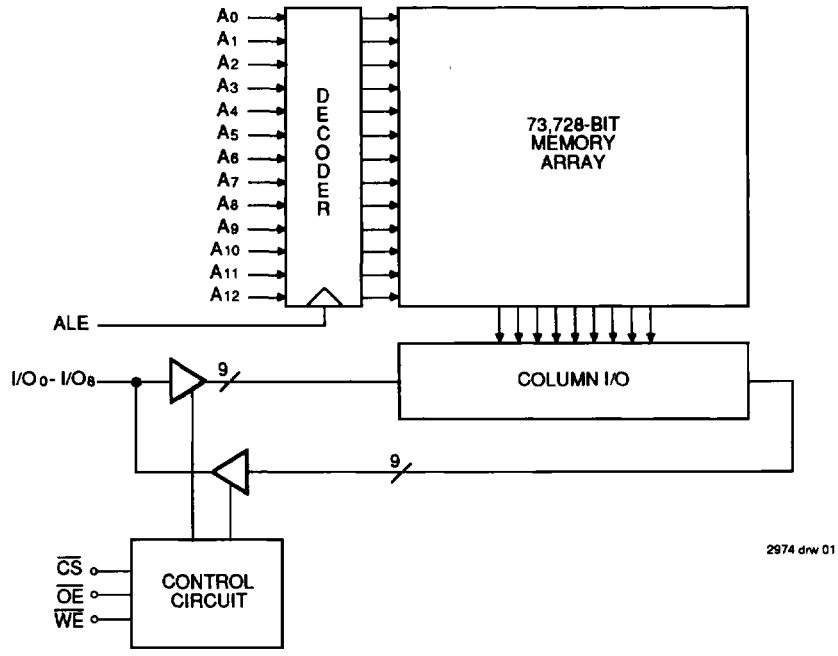
The IDT71569 is a 73,728-bit high-speed static RAM, organized as 8K x 9, with address latches. It is fabricated using IDT's high-performance, high-reliability CEMOS technology.

The IDT71569 offers address access times as fast as 10ns. The ninth bit is optimal for systems using parity. This device is ideally suited for cache memory applications.

All inputs and outputs of the IDT71569 are TTL-compatible. The IDT71569 is packaged in an industry standard 300-mil 28-pin DIP and SOJ plastic packages.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally

FUNCTIONAL BLOCK DIAGRAM



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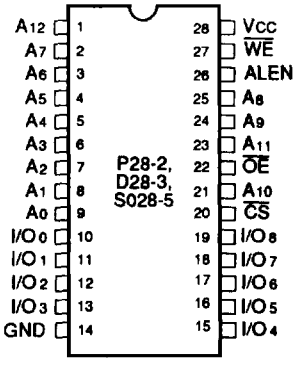
PIN CONFIGURATION



2974 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE[1]

ALE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
H	X	X	X	X	Address Latch Transparent
L	X	X	X	X	Address Latch Closed
H	L	L	H	DOUT	Read From Current Address
L	L	L	H	DOUT	Read From Latched Address
H	L	X	L	DIN	Write to Current Address
L	L	X	L	DIN	Write to Latched Address
X	L	H	H	Hi-Z	Outputs Disabled

NOTE:
1. H = VIH, L = VIL, X = Don't Care.

2974 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:

2974 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:

2974 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2974 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:

2974 tbl 05

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71569S20[3] 71569L20[3] Com'l.	Mil.	71569S25 71569L25 Com'l.	Mil.	71569S35[4] 71569L35[4] Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current	S	90	—	90	100	—	100	mA
	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	L	80	—	80	90	—	90	
I_{CC2}	Dynamic Operating Current	S	180	—	170	190	—	160	mA
	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	L	160	—	150	170	—	140	
I_{SB}	Standby Power Supply Current (TTL Level)	S	20	—	20	20	—	20	mA
	$\overline{CS}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	L	3	—	3	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	S	15	—	15	20	—	20	mA
	$\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{HC}, f = 0[2]	L	0.2	—	0.2	1.0	—	1.0	

2974 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
3. 0° to +70° C. temperature range only.
4. -55° to +125° C. temperature range only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2974 tbl 07

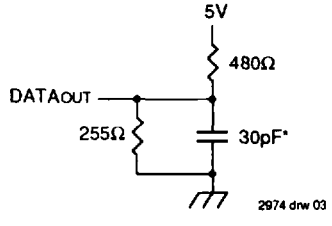


Figure 1. Output Load

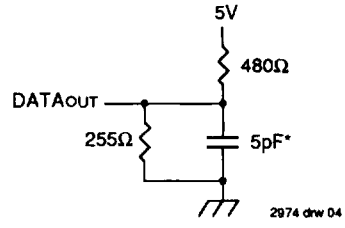


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7169S Min.	IDT7169S Max.	IDT7169L Min.	IDT7169L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2974 tbl 08

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

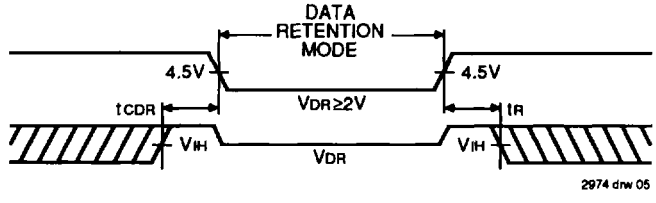
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typical[1] Vcc @ 2.0v	Typical[1] Vcc @ 3.0V	Maximum Vcc @ 2.0V	Maximum Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current	—		—	—	—	2	2	µA

2974 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2974 drw 05

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

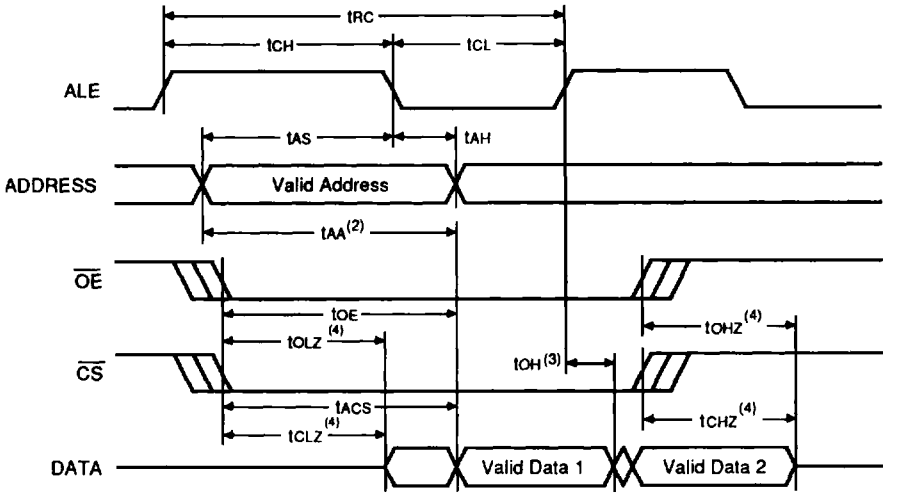
Symbol	Parameter	71569S20[1] 71569L20[1] Min.	Max.	71569S25 71569L25 Min.	Max.	71569S35[4] 71569L35[4] Min.	Max.	Unit
Read Cycle								
tRC	Read Cycle Time	20	—	25	—	35	—	ns
tAA	Address Access Time[3]	—	19	—	25	—	35	ns
tALA	Address Latch Access Time	—	20	—	25	—	35	ns
tACS	Chip Select Access Time	—	20	—	25	—	35	ns
tCLZ	Chip Select to Output in Low Z[2]	3	—	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	8	—	12	—	18	ns
tOLZ	Output Enable to Output in Low Z[2]	3	—	3	—	3	—	ns
tCHZ	ChipSelect to Output High Z[2]	—	13	—	15	—	25	ns
tOHZ	Output Disable to Output in High Z[2]	—	10	—	15	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
tCH	ALEN High Time	10	—	10	—	10	—	ns
tCL	ALEN Low Time	10	—	10	—	10	—	ns
tAS	Address Set-up Time to Address Latch Enable	5	—	5	—	5	—	ns
tAH	Address Hold Time to Address Latch Enable	3	—	5	—	7	—	ns
Write Cycle								
tWC	Write Cycle Time	20	—	25	—	35	—	ns
tAW	Address Valid to End of Write[3]	15	—	18	—	25	—	ns
tCW	Chip Select to End of Write	15	—	18	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	21	—	25	—	ns
tWR	Write Recovery Time[3]	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[2]	—	8	—	10	—	14	ns
tDW	Data Valid to End of Write	10	—	13	—	15	—	ns
tDH	Data Hold Time from Write	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[2]	5	—	5	—	5	—	ns
tCH	ALEN High Time	10	—	10	—	10	—	ns
tCL	ALEN Low Time	10	—	10	—	10	—	ns
tAS	Address Set-up Time to Address Latch Enable	5	—	5	—	5	—	ns
tAH	Address Hold Time to Address Latch Enable	5	—	5	—	5	—	ns

NOTES:

2974 tbl 10

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed, but not tested.
3. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.
4. -55°to +125° C. temperature range only.

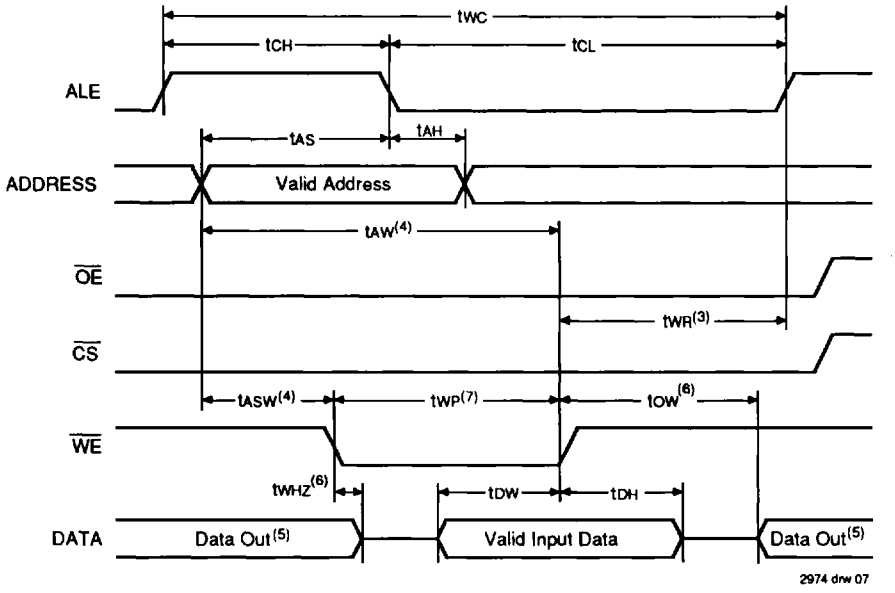
TIMING WAVEFORM OF READ CYCLE (1)



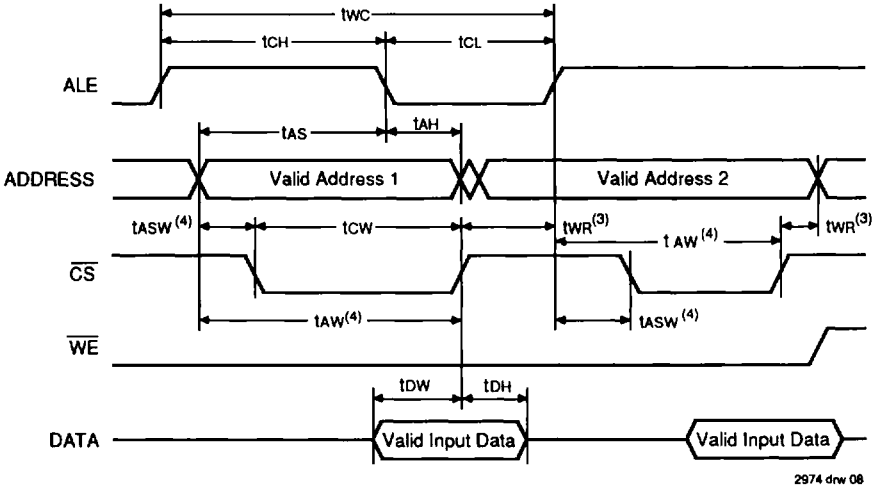
NOTES:

1. $\overline{WE}$ is high throughout a read cycle.
2. The parameter t_{AA} is measured either from the first low to high transition of ALEN after the read address has become valid, or from the stabilization of the read address during the period when ALEN is high, which ever occurs last.
3. The parameter t_{OH} is measured either from the first low to high transition of ALEN after an address change, or from an address change during the period when ALEN is high, whichever occurs first.
4. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1,2)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,2)



NOTES:

1. $\overline{WE}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs last.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALEN after an address change has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.
5. During this period, the I/O pins are in the output state so that the input signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION