Spectrum Spread Clock Generator

Approved Product

PRODUCT FEATURES

- Reduces Clock-related EMI up to 20 dB
- Replicates and modulates externally applied signals
- 3.0V to 5.5V operating supply range
- Operating range of from 14 to 30 Mhz.
- Output is center spread around reference frequency.
- Will accept input frequencies between 14 and 30 Mhz.
- TTL or CMOS compatible outputs with 6mA drive capability
- 16 pin SOIC packages
- Frequency spreading with Fout center frequency.
- Compliant with all major CISC, RISC, and DSP processors
- Low, short-term jitter
- Locks to externally applied signal

BLOCK DIAGRAM

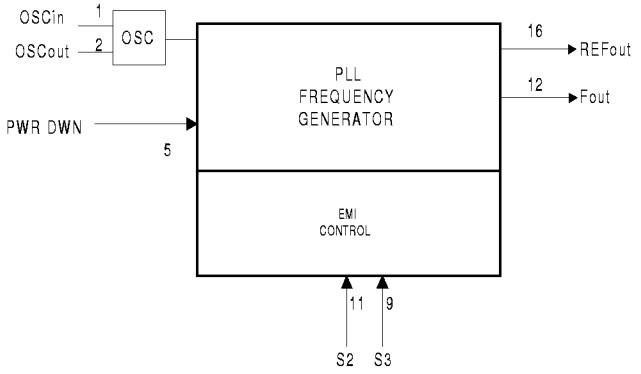

Figure 1.

PRODUCT DESCRIPTION

The IMISG533 is a spectrum spread clock modulator designed for personal computers, modems, laser printers and other digital systems. The IMISG533 uses a patented concept to broadband clock frequencies to reduce measured electromagnetic emissions from system clocks and their associated harmonics. This reduction can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The IMISG533 is extremely flexible in that the amount of spread of the broadbanded clock is selectable. The power-down mode adds the flexibility to operate the device in a completely static mode to reduce standby currents and simplify system board tests.

SOIC CONNECTION DIAGRAM

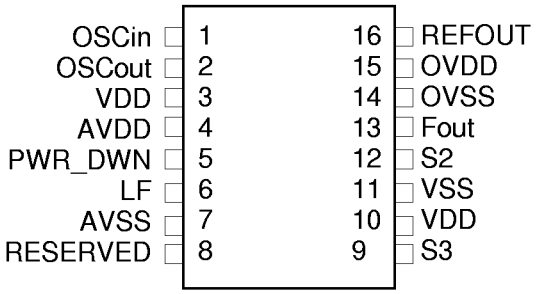

Figure 2.

APPLICATIONS

The IMISG533 applied to existing clock frequencies will modulate that frequency centering on the input frequency. It can be used with input frequencies between 14 Mhz and 30 Mhz. See page 3 for 3-volt supply information.

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PIN DESCRIPTION

OSCin, OSCout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. OSCin may also serve as an input for an externally generated CMOS level or AC coupled reference signal.

Fout - Modulated clock output that is symetrically center spread around the input reference frequency.

LF - This is a phase detector output for the clock signal. It is a single-ended, tri-state output for use as a loop error signal. See Figure 3.

PWR_DWN - Power down selection. When equal to 1, the SM533 is in the normal operating mode. When equal to 0, the SM533 is in the power down mode and the output state is defined by the S2 and S3 settings..

S2, S3 - Control pins for setting amount of modulation. See Table 2 for settings. S2 has internal pull-up; S3 has internal pull-down. When in power down mode, S2 and S3 determine the state of Fout. See table 1 for power down settings.

Reserved - This pin is reserved for IMI test purposes. Do not connect this pin to any external circuitry.

AVDD - Analog circuit positive power supply.

AVSS - Analog circuit ground.

VDD - Digital circuit positive power supply.

VSS - Digital circuit ground.

OVDD - Oscillator circuit power supply.

OVSS - Oscillator circuit ground.

Note - OVDD and OVSS may be common to VDD and VSS respectively.

RECOMMENDED LOOP FILTER

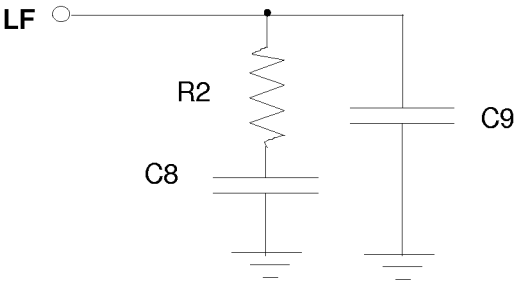

Figure 3.

Recommended Loop Filter Values

14.318 Mhz:	R2 = 2 K ohms
	C8 = 5600 pf.
	C9 = 560 pf.
15 - 30 Mhz:	R2 = 2 K ohms
	C8 = 2000 pf.
	C9 = 300 pf.

Figure 4.

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POWER DOWN SELECTION TABLE			
PWR_DWN	S3	S2	Fout State
1	See Table 2	See Table 2	Modulated Clock
0	0	0	0
0	0	1	1
0	1	0	Reserved for IMI testing
0	1	1	Hi-Z

Table 1

When Power-down address is selected, the VCO is turned off and the modulation is in the standby mode. The phase detector is in the tri-state mode.

* Note: When operating in 3-volt applications, the input frequency is restricted to no more than 66% of the maximum frequency of the applicable Fin range.

SPECTRUM SPREAD CLOCK MODULATOR MODULATION SELECTION TABLE				
EMI Reductuion	Modulation Settings		Bandwidth Limit Frequencies as a % Value of Fout	
	S3	S2	Low	High
Minimum EMI Control	0	0	99.375%	100.625%
Suggested Setting	0	1	98.75%	101.25%
Alternate Setting	1	0	97.5%	102.5%
Maximum EMI Reduction	1	1	95%	105%

Table 2

In systems less tolerant of clock frequency changes, S2 and S3 set to 0 is recommended. See Figures 5, 6, and 7.

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 6V
Voltage Relative to VD:	0.3V
Storage Temperature:	0°C to + 125°C
Operating Temperature:	0°C to + 70°C
Recommended Operating Range:	3.OV - 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however; precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (Vin \text{ or } Vout) < VDD$$

All inputs are tied high or low internally.

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ELECTRICAL CHARACTERISTICS					
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Input Low Voltage	VIL	-	-	0.8	Vdc
Input High Voltage	VIH	2.0	-	-	Vdc
Input Low Current	IIL	-	-	100	µA
Input High Current	IIH	-	-	100	µA
Output Low Voltage IOL= 6mA	VOL	-	-	0.4	Vdc
Output High Voltage IOH = 6mA	VOH	2.5	-	-	Vdc
Tri-State Leakage Current	IOZ	-	-	10	µA
Static Supply Current	IDD	-	-	250	µA
Dynamic Supply Current	ICC	-	25	30	mA
Short Circuit Current	ISC	25	-	-	mA
VDD = 5V ±10%, TA = 0°C to 70°C					

SWITCHING CHARACTERISTICS					
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Output Rise Time Measured at 10% - 90% of VDD	tTLH	3.4	3.8	4.2	ns
Output Fall Time Measured at 10% - 90% of VDD	tTHL	2.2	2.5	2.8	ns
Output Rise Time Measured at 0.8V - 2.0V	tTLH	.8	.95	1.2	ns
Output Fall Time Measured at 0.8V - 2.0V	tTHL	.75	.95	1.0	ns
Output Duty Cycles	TsymF1	45	50	55	%
Peak-to Peak Jitter One Sigma (SSON = 1)	tj1s		-	500	ps
VDD = 5V ± 10%, TA = 0°C to 70°C, CL = 15pF, Fout = 44.2 Mhz.					

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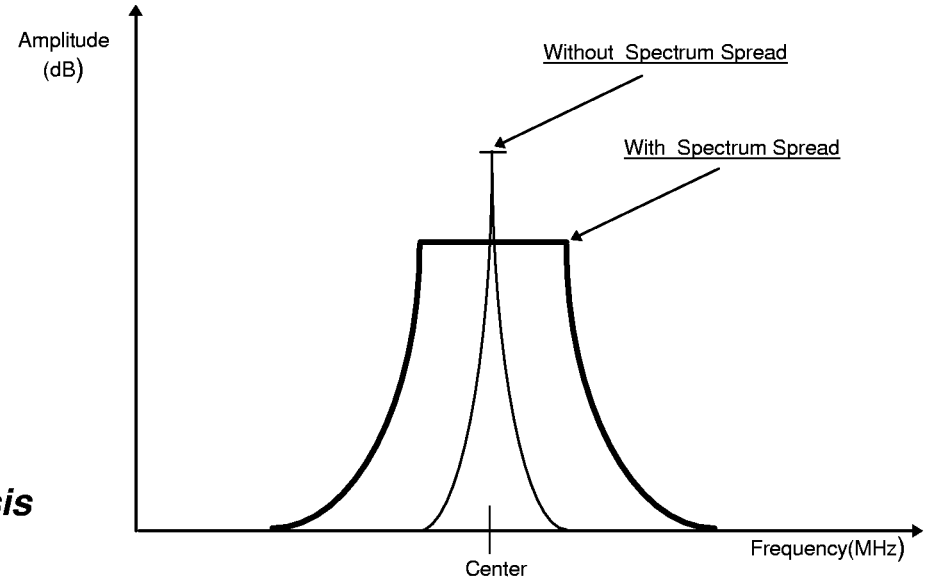
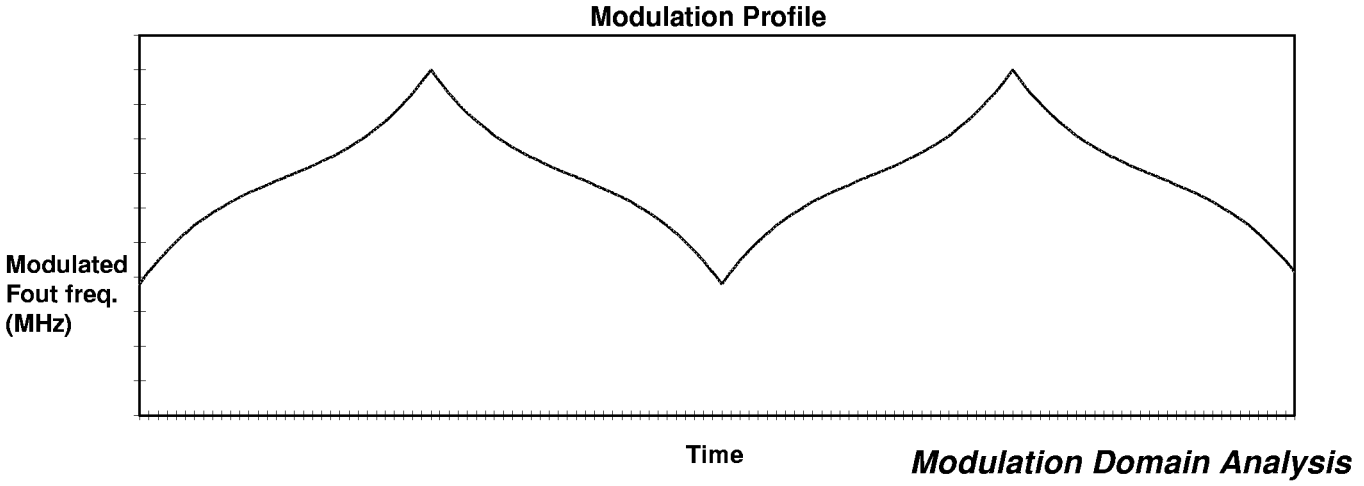
SPECTRUM SPREAD



Spectrum Analysis

Figure 5.



Modulation Domain Analysis

Note : The modulation rate, *fr*, is dependent on the Input frequency (Xin).

Figure 6.

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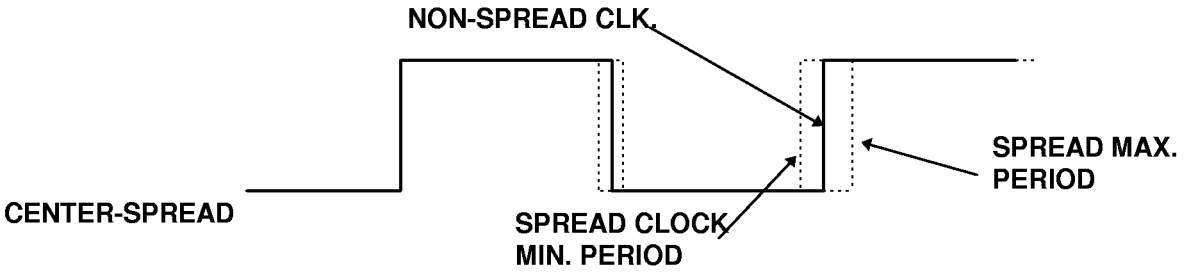

Modulation Period

Figure 7.

APPLICATION SUGGESTION

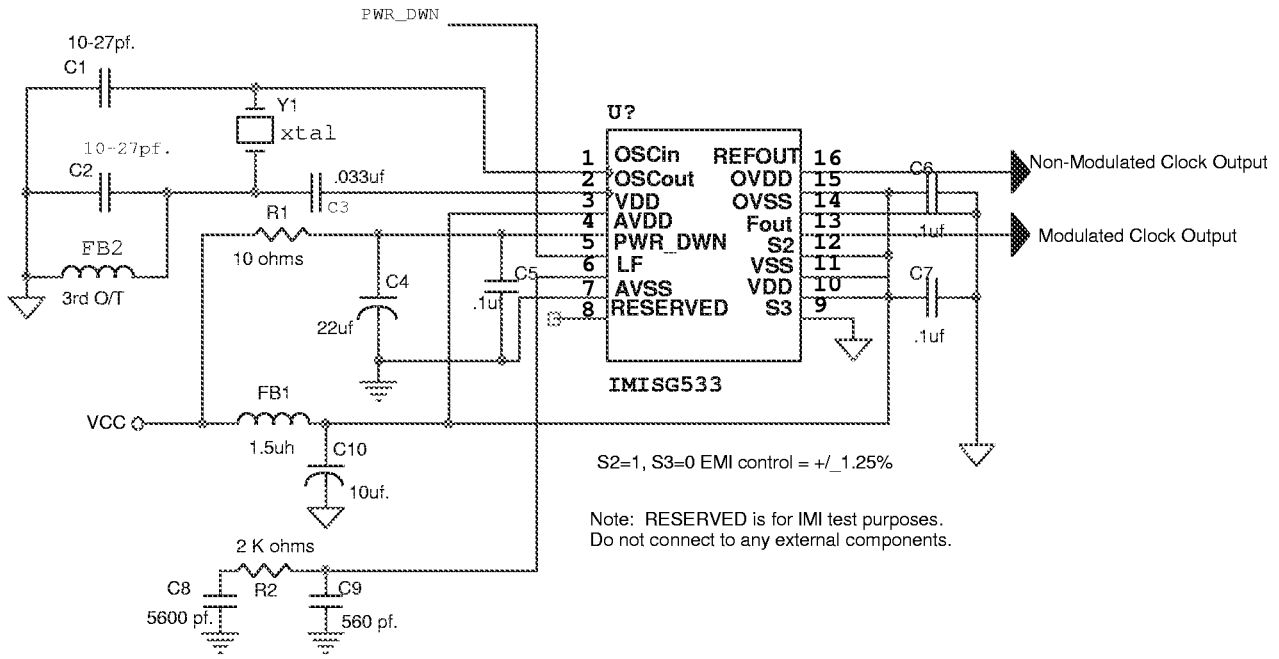

Figure 8.

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PACKAGE DRAWING AND DIMENSIONS

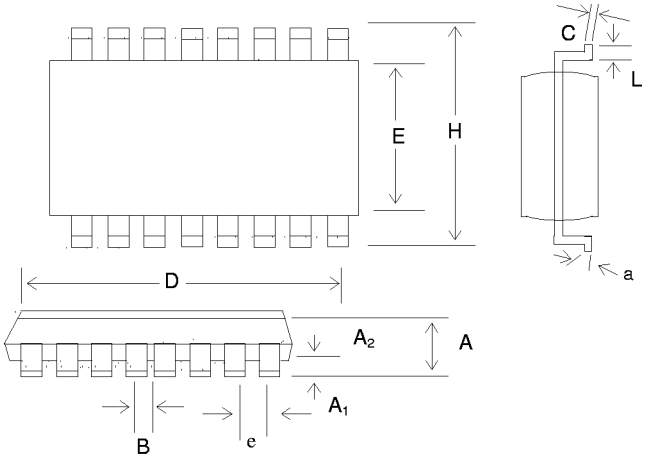

Figure 8.

16 PIN SOIC OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.0020	0.009	0.0015	0.060	0.22	0.38
A2	0.090	0.092	0.111	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	.399	.407	.412	10.13	10.34	10.46
E	0.285	0.296	0.299	7.24	7.52	7.59
e	0.050 BSC			1.27 BSC		
H	0.400	0.406	0.40	10.16	10.31	10.41
a	0°	5°	10°	0°	5°	10°
L	0.24	0.032	0.040	0.61	0.81	1.02

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG533AXB	16 Pin SOIC	Commercial, 0°C to + 70°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG533AXB
Date Code, Lot#

IMISG533AXB

Flow
B = Commercial, 0°C to + 70°C
Package
X = SOIC
Revisions

IMI Device Number